19-0282; Rev 0; 7/94

EVALUATION KIT AVAILABLE

250Msps, 8-Bit ADC with Track/Hold

MAX100

General Description

The MAX100 ECL-compatible, 250Msps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 125MHz (Nyquist frequency). Designed with Maxim's proprietary advanced bipolar processes, the MAX100 contains a high-performance track/hold (T/H) amplifier and a quantizer in a single ceramic strip-line package.

The innovative design of the internal T/H assures an exceptionally wide input bandwidth of 1.2GHz and aperture delay uncertainty of less than 2ps, resulting in a high 6.8 effective bits performance. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes occurring due to metastable states is reduced to less than 1 error per 10^{15} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX100 keeps the magnitude to less than 1LSB.

The analog input is designed for either differential or single-ended use with a ±270mV range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric use. Midpoint tap for the reference string is available for applications that need to modify the output coding for a user-defined bilinear response. Use of separate high-current and low-current ground pins provides better noise immunity and highest device accuracy.

Dual output data paths provide several data output modes for easy interfacing. These modes can be configured as either one or two identical latched ECL outputs. An 8:16 demultiplexer mode that reduces the output data rates to one-half the clock rate is also available.

For applications that require faster data rates, refer to Maxim's MAX101, which allows conversion rates up to 500Msps.

Features

- **250Msps Conversion Rate**
- **6.8 Effective Bits at 125MHz**
- **Less than ±1/2LSB INL**
- **50Ω Differential or Single-Ended Inputs**
- **±270mV Input Signal Range**
- **Reference Sense Inputs**
- **Ratiometric Reference Inputs**
- **Configurable Dual-Output Data Paths**
- **Latched, ECL-Compatible Outputs**
- **Low Error Rate, Less than 10^{-15} Metastable States**
- **Selectable On-Chip 8:16 Demultiplexer**
- **84-Pin Ceramic Flat Pack**

Applications

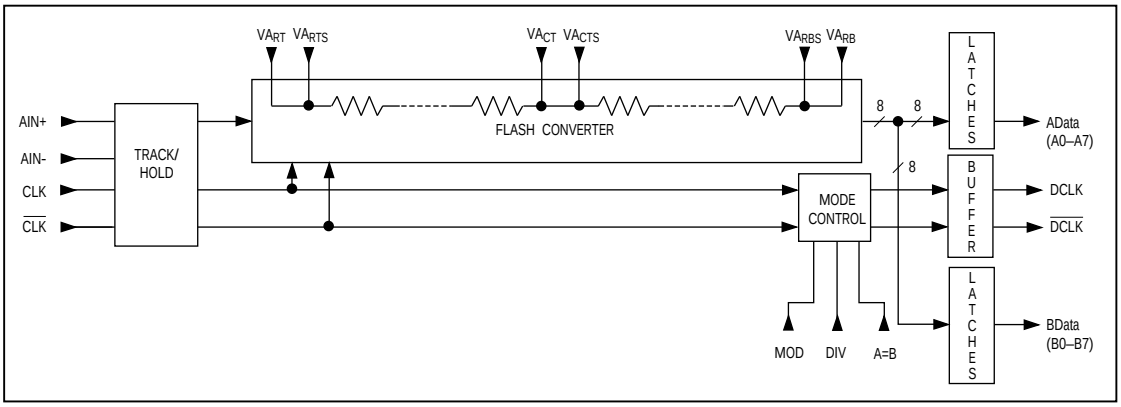
High-Speed Digital Instrumentation
High-Speed Signal Processing
Medical Systems
Radar/Sonar
High-Energy Physics
Communications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX100CFR*	0°C to +70°C	84 Ceramic Flat Pack (with heatsink)

**Contact factory for 84-Pin Ceramic Flat Pack without heatsink.*

Functional Diagram



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
V_{CC} .....0V to +7V
V_{EE} .....-7V to 0V
V_{CC} - V_{EE}.....+12V
Analog Input Voltage .....±2V
Digital Input Voltage .....-2.3V to +0V
Reference Voltage (VA_{RT}) .....-0.3V to +1.5V
Reference Voltage (VA_{RB}).....-1.5V to +0.3V
Data Output Current .....-33mA
DCLK Output Current .....-43mA
Operating Temperature Range.....0°C to +70°C
Operating Junction Temperature (Note 2).....0°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+250°C

Note 1: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in conductive foam or shunt the terminals together. Discharge the conductive foam to the destination socket before insertion.

Note 2: Typical thermal resistance, junction-to-case $R_{\theta JC}$ = 5°C/W and thermal resistance, junction to ambient (MAX100CA) $R_{\theta JA}$ = 12°C/W, providing 200 lineal ft/min airflow with heatsink. See *Package Information.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 50Ω to -2V, VA_{RT} = 1.02V, VA_{RB} = -1.02V, T_{MIN} to T_{MAX} = 0°C to +70°C, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Integral Nonlinearity (Note 4)	INL	AData, BData	T_A = +25°C			±0.5	LSB
			T_A = T_{MIN} to T_{MAX}			±0.6	
Differential Nonlinearity	DNL	AData, BData, no missing codes	T_A = +25°C			±0.75	LSB
			T_A = T_{MIN} to T_{MAX}			±0.85	
DYNAMIC SPECIFICATIONS							
Effective Bits	ENOB	f_{CLK} = 250MHz, V_{IN} = 95% full scale (Note 5)	f_{AIN} = 10MHz		7.4		Bits
			f_{AIN} = 50MHz		7.1		
			f_{AIN} = 125MHz	6.8			
Signal-to-Noise Ratio	SNR	f_{AIN} = 50MHz, f_{CLK} = 250MHz, V_{IN} = 95% full scale (Note 6)			44.5		dB
Maximum Conversion Rate	f_{CLK}	(Note 7)		250			Msps
Analog Input Bandwidth	BW_{3dB}				1.2		GHz
Aperture Width	t_{AW}	Figure 5			270		ps
Aperture Jitter	t_{AJ}	Figure 5			2		ps
ANALOG INPUT							
Input Voltage Range	V_{IN}	AIN+ to AIN-, Table 2, T_A = T_{MIN} to T_{MAX}	Full scale	230		315	mV
			Zero scale	-305		-215	
Input Offset Voltage	V_{IO}	AIN+, AIN-, T_A = T_{MIN} to T_{MAX}		-17		+32	mV
Least-Significant-Bit Size	LSB	T_A = T_{MIN} to T_{MAX}		1.8		2.5	mV
Input Resistance	R_I	AIN+ and AIN- with respect to GND		49		51	Ω
Input Resistance Temperature Coefficient					0.008		Ω/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 50Ω to -2V, VA_{RT} = 1.02V, VA_{RB} = -1.02V, T_{MIN} to T_{MAX} = 0°C to +70°C, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Reference String Resistance	R_{REF}	VA_{RT} to VA_{RB}		116		175	Ω
Reference String Resistance Temperature Coefficient					0.02		Ω/°C
LOGIC INPUTS							
Digital Input Low Voltage (Note 8)	V_{IL}	DIV, MOD, A=B, CLK, $\overline{CLK}$, T_A = T_{MIN} to T_{MAX}				-1.5	V
Digital Input High Voltage (Note 8)	V_{IH}	DIV, MOD, A=B, CLK, $\overline{CLK}$, T_A = T_{MIN} to T_{MAX}		-1.07			V
Digital Input Low Current	I_{IL}	DIV, MOD, A=B = -1.8V, T_A = T_{MIN} to T_{MAX}		-5		20	µA
		CLK, $\overline{CLK}$, V_{IL} = -1.8V (no termination), T_A = T_{MIN} to T_{MAX}		0		80	
Digital Input High Current	I_{IH}	DIV, MOD, A=B = -0.8V, T_A = T_{MIN} to T_{MAX}		-5		20	µA
		CLK, $\overline{CLK}$, V_{IH} = -0.8V (no termination), T_A = T_{MIN} to T_{MAX}		0		80	
LOGIC OUTPUTS (Note 9)							
Digital Output Low Voltage	V_{OL}	AData, $\overline{AData}$, BData, $\overline{BData}$, DCLK, $\overline{DCLK}$	T_A = +25°C	-1.95		-1.60	V
			T_A = T_{MIN} to T_{MAX}	-1.95		-1.50	
Digital Output High Voltage	V_{OH}	AData, $\overline{AData}$, BData, $\overline{BData}$, DCLK, $\overline{DCLK}$	T_A = +25°C	-1.02		-0.70	V
			T_A = T_{MIN} to T_{MAX}	-1.10		-0.70	
POWER REQUIREMENTS							
Positive Supply Current	I_{CC}	V_{CC} = 5.0V	T_A = +25°C		464	670	mA
			T_A = T_{MIN} to T_{MAX}			710	
Negative Supply Current	I_{EE}	V_{EE} = -5.2V	T_A = +25°C	-750	-560		mA
			T_A = T_{MIN} to T_{MAX}	-780			
Common-Mode Rejection Ratio	CMRR	V_{INCM} = ±0.5V	T_A = T_{MIN} to T_{MAX}	35			dB
Power-Supply Rejection Ratio	PSRR	T_A = T_{MIN} to T_{MAX}	V_{CC}(nom) = ±0.25V	40			dB
			V_{EE}(nom) = ±0.25V	40			

TIMING CHARACTERISTICS

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 50Ω to -2V, VA_{RT} = 1.02V, VA_{RB} = -1.02V, T_A = +25°C, unless otherwise noted.)

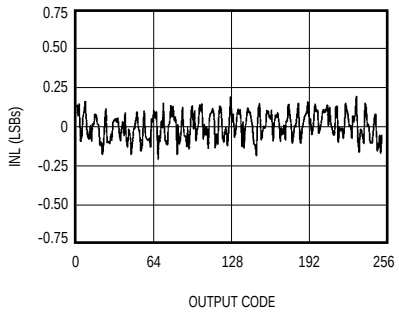
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Clock Pulse Width Low	t_{PWL}	CLK, $\overline{CLK}$, Figures 1 and 2			1.9		5.0	ns
Clock Pulse Width High	t_{PWH}	CLK, $\overline{CLK}$, Figures 1 and 2			1.9			ns
CLK to DCLK Propagation Delay	t_{PD1}	DIV = 0, Figure 1			0.8		2.4	ns
		DIV = 1, Figure 2			1.9		5.7	
DCLK to A/BData Propagation Delay	t_{PD2}	DIV = 0, Figure 1			0.5		2.2	ns
		DIV = 1, Figure 2			-1.4		-0.1	
Rise Time	t_R	20% to 80%	DCLK			500		ps
			DATA			700		
Fall Time	t_F	20% to 80%	DCLK			600		ps
			DATA			550		
Pipeline Delay (Latency)	t_{NPD}	See Figures 3 and 4 and Table 1 (delay depends on output mode)	Divide-by-1 mode		7 1/2		7 1/2	Clock Cycles
			Divide-by-2 mode	AData	7 1/2		7 1/2	
				BData	8 1/2		8 1/2	

Note 3: All devices are 100% production tested at +25°C and are guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} as specified.
Note 4: Deviation from best-fit straight line. See *Integral Nonlinearity* section.
Note 5: See the *Signal-to-Noise Ratio and Effective Bits* section in the *Definitions of Specifications.*
Note 6: SNR calculated from effective bits performance using the following equation: SNR (dB) = 1.76 + (6.02) (effective bits).
Note 7: Clock pulse width minimum requirements t_{PWL} and t_{PWH} must be observed to achieve stated performance.
Note 8: Functionality guaranteed for $-1.07 \le V_{IH} \le -0.7$ and $-2.0 \le V_{IL} \le -1.5$.
Note 9: Outputs terminated through 50Ω to -2.0V.

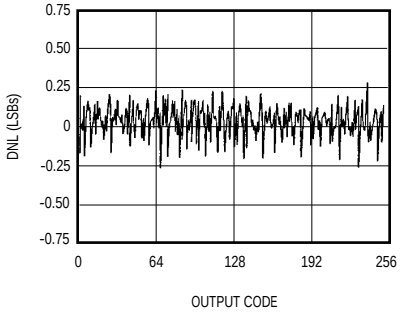
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

INTEGRAL NONLINEARITY vs. OUTPUT CODE



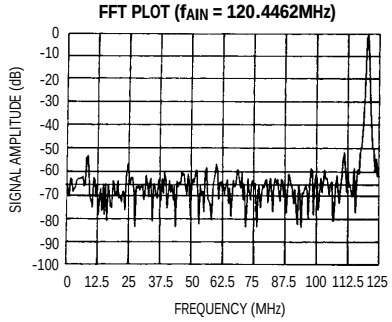
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



Typical Operating Characteristics (continued)

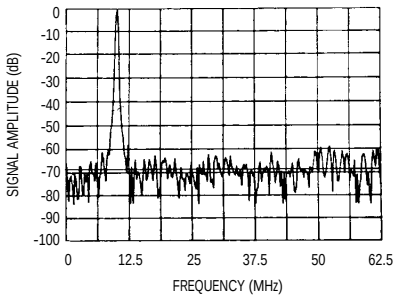
(T_A = +25°C, unless otherwise noted.)

FFT PLOT (f_{AIN} = 120.4462MHz)



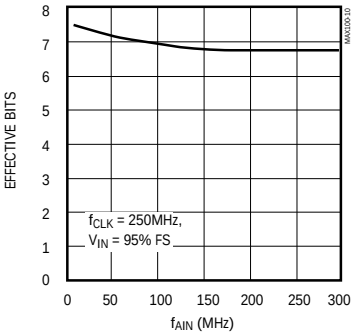
f_{CLK} = 250MHz, f_{AIN} = 120.4462MHz
SER = -42.3dB, NOISE FLOOR = -65.4dB

FFT PLOT (f_{AIN} = 10.4462MHz)

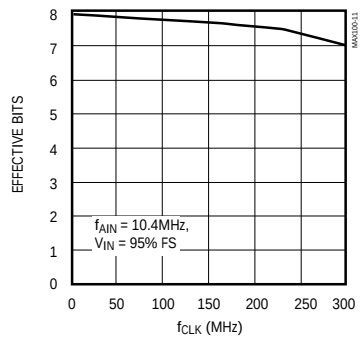


f_{CLK} = 250MHz, f_{AIN} = 10.4462MHz
SER = -45.87dB, NOISE FLOOR = -68.5dB

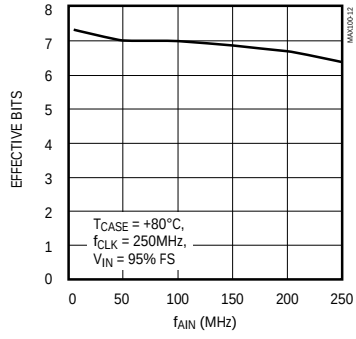
EFFECTIVE BITS vs. ANALOG INPUT FREQUENCY



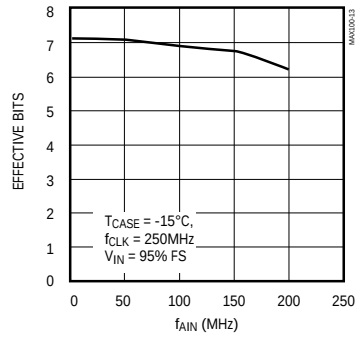
EFFECTIVE BITS vs. CLOCK FREQUENCY



EFFECTIVE BITS vs. ANALOG INPUT FREQUENCY



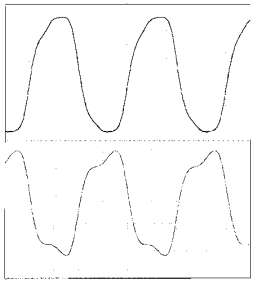
EFFECTIVE BITS vs. ANALOG INPUT FREQUENCY



Typical Operating Characteristics (continued)

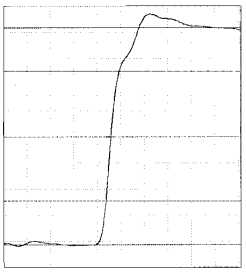
(T_A = +25°C, unless otherwise noted.)

CLOCK RELATIONSHIP (DIVIDE-BY-1 MODE)



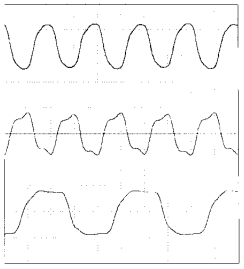
A = CLK, 200mV/div
B = DCLK, 200mV/div
TIMEBASE = 1ns/div,
f_{CLK} = 250MHz

DIGITAL CLOCK (POSITIVE EDGE)



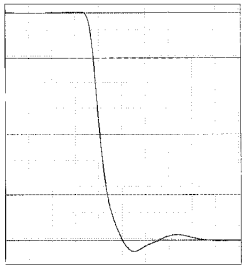
TIMEBASE = 1ns/div, t_r = 580ps

CLOCK/DATA (DIVIDE-BY-1 MODE)



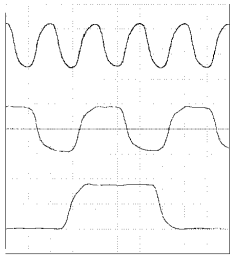
A = CLK, 500mV/div
B = DCLK, 500mV/div
C = AData, 500mV/div
TIMEBASE = 2ns/div,
f_{CLK} = 250MHz

DATA OUTPUT (NEGATIVE EDGE)



TIMEBASE = 1ns/div, t_f = 596ps

CLOCK/DATA (DIVIDE-BY-2 MODE)



A = CLK, 500mV/div
B = DCLK, 500mV/div
C = AData, 500mV/div
TIMEBASE = 2ns/div,
f_{CLK} = 250MHz

CLOCK/DATA DETAIL (DIVIDE-BY-5 MODE)

A = DCLK, 200mV/div
B = AData, 200mV/div
TIMEBASE = 5ns/div,
f_{CLK} = 250MHz

Pin Description

PIN	NAME	FUNCTION
1	PAD	Internal connection, leave open.
2, 62	CLK	Complementary Differential Clock Inputs. Can be driven from standard 10K ECL with the following considerations: Internally, pins 2 & 62 and 3 & 61 are the ends of a 50Ω transmission line. Either end can be driven, with the other end terminated with 50Ω to -2V. See *Typical Operating Circuit.*
3, 61	$\overline{CLK}$	
4, 7, 15, 49, 57, 60, 64, 67, 70, 71, 74, 77, 78, 79, 82, 84	GND	Power-Supply Ground. Connect GND and DGND pins (Note 10).
5, 6, 9, 10, 31, 33, 35, 48, 58, 59, 63, 81, 83	N.C.	No Connect—there is no internal connection to these pins.
8, 21, 43, 56	VCC	Positive power supply, +5V ±5% nominal
11	DIV	Divide Enable Input. DIV and MOD select the output modes. See Table 1.
12	MOD	Modulus. MOD and DIV select the output modes. See Table 1.
13	$\overline{DCLK}$	Complementary Differential Clock Outputs. Used to synchronize following circuitry: AData and BData outputs are valid t_{PD2} after the rising edge of DCLK. See Figures 1–4.
14	DCLK	
16	A=B	Sets AData equal to BData when asserted (A=B = 1). See Table 1.
17, 20, 23, 26, 36, 39, 42, 45	A7–A0	AData and BData Outputs. A0 and B0 are the LSBs, and A7 and B7 are the MSBs. AData and BData outputs conform to standard 10K ECL logic swings and drive 50Ω transmission lines. Terminate with 50Ω to -2V. See Figures 1–4.
19, 22, 25, 28, 38, 41, 44, 47	B7–B0	
18, 24, 27, 30, 34, 37, 40, 46	DGND	Power-Supply Ground. Connect all ground (GND, DGND) pins together, as described in Note 10.
29	SUB	Circuit Substrate Contact. This pin **must** be connected to VEE.
32, 69, 80	VEE	Negative Power Supply, -5.2V ±5% nominal
50	VA_{RT}	Positive Reference Voltage Input (Note 11)
51	VA_{RTS}	Positive Reference Voltage Sense (Note 11)

Pin Description (continued)

PIN	NAME	FUNCTION
52	VA_{CTS}	Reference Bias Resistor Center-Tap Sense (Note 12)
53	VA_{CT}	Reference Bias Resistor Center Tap (Note 12)
54	VA_{RBS}	Negative Reference Voltage Sense (Note 11)
55	VA_{RB}	Negative Reference Voltage Input (Note 11)
65	TP3	Internal node. Do not connect.
66	TP2	Internal node. Do not connect.
68	TP1	Internal connection. This pin **must** be connected to GND.
72, 73	AIN+	Analog Inputs, internally terminated with 50Ω to ground. Full-scale linear input range is approximately ±270mV. Drive AIN+ and AIN- differentially for best high-frequency performance.
75, 76	AIN-	

Note 10: Use a multilayer board with a separate layer dedicated to ground. Connect GND and DGND in separate areas in the ground plane (separated by at least 1/4 inch) and at only one location on the board (see *Typical Operating Circuit*).

Note 11: Reference bias supply. Use a separate high-quality supply for these pins. Carefully bypassing these pins to achieve noise-free operation of the reference supplies contributes directly to high ADC accuracy.

Note 12: The center-tap connection of the MAX100 is normally left open. It can be driven with a bias voltage, but should be bypassed carefully (refer to Note 11).

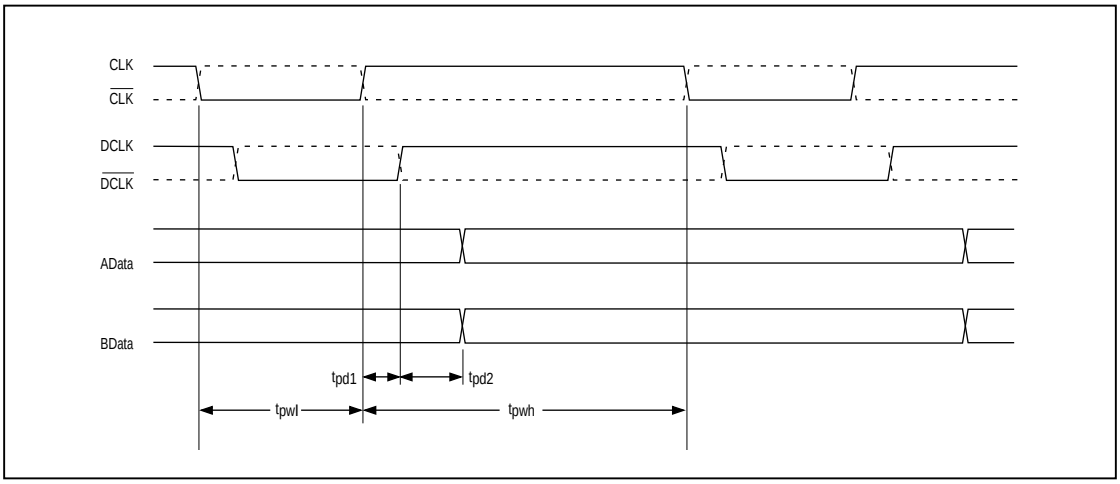


Figure 1. Output Timing: Divide-by-1 Mode (DIV = 0)

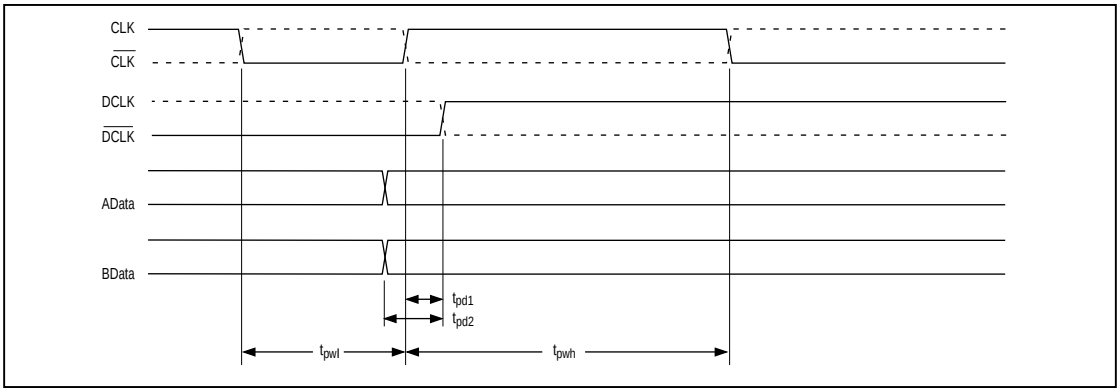


Figure 2. Output Timing: Divide-by-2 or Divide-by-5 Mode (DIV = 1)

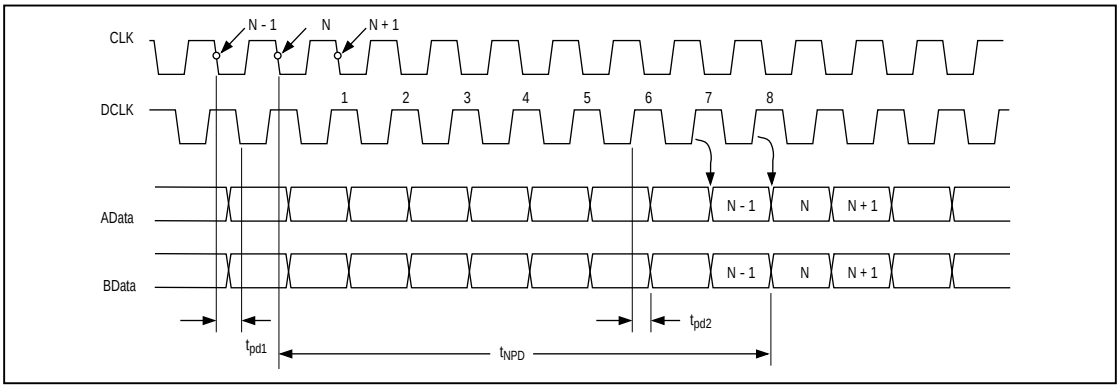


Figure 3. Output Timing: Clock to Data, Divide-by-1 Mode (fast mode, DIV = 0)

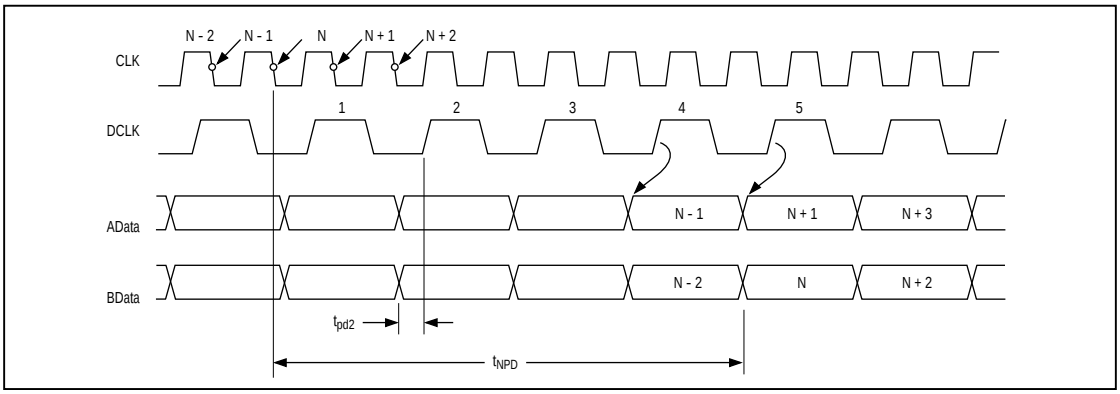


Figure 4. Output Timing: Divide-by-2 Mode (DIV = 1)

Definitions of Specifications

Signal-to-Noise Ratio and Effective Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other analog-to-digital (A/D) output signals. The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of effective bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB. The FFT plots in the *Typical Operating Characteristics* show the output level in various spectral bands.

Effective bits is calculated from a digital record taken from the ADC under test. The quantization error of the ideal converter equals the total error of the device. In addition to ideal quantization error, other sources of error include all DC and AC nonlinearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

The ADC's input is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase, and amplitudes of the mathematical model are adjusted until a best-fit sine wave is found. After subtracting this sine wave from the digital record, the residual error remains. The rms value of the error is applied in the following equation to yield the ADC's effective bits.

$$\text{Effective bits} = N - \log_2 \left(\frac{\text{measured rms error}}{\text{ideal rms error}} \right)$$

where N is the resolution of the converter. In this case, N = 8.

The worst-case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (1/2 the input clock rate).

Aperture Width and Jitter

Aperture width is the time the T/H circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in hold mode). Aperture jitter is the sample-to-sample variation in aperture delay (Figure 5).

Error Rates

Errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for many typical converters can be incorrect, including false full- or zero-scale output. The MAX100's unique design reduces the magnitude of this type of error to 1LSB, and reduces the probability of the error occurring to less than one in every 10^{15} clock cycles. If the MAX100 were operated at 250MHz, 24 hours a day, this would translate to less than one metastable-state error every 46 days.

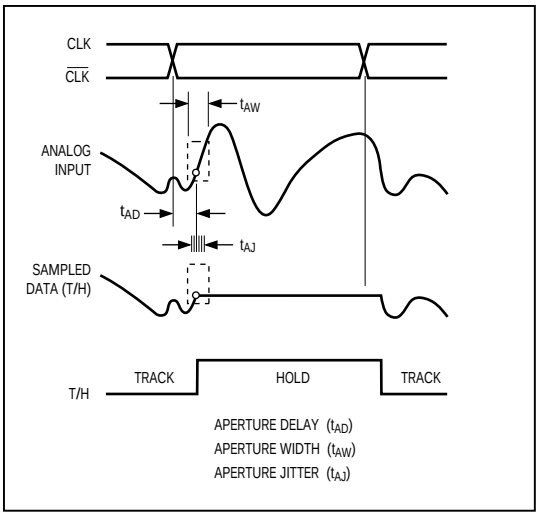


Figure 5. T/H Aperture Timing

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1LSB using a "best straight line" determined by a least square curve fit.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DNL is expressed in LSBs and is calculated using the following equation:

$$\text{DNL(LSB)} = \frac{[V_{MEAS} - (V_{MEAS-1})] - \text{LSB}}{\text{LSB}}$$

where V_{MEAS-1} is the measured value of the previous code.

A DNL specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Detailed Description

Converter Operation

The parallel or "flash" architecture used by the MAX100 provides the fastest multibit conversion of all common integrated ADC designs. The basic element of a flash (as with all other ADC architectures) is the comparator, which has a positive input, a negative input, and an output. If the voltage at the positive input is higher than the negative input (connected to a reference), the output will be high. If the positive input voltage is lower than the reference, the output will be low. A typical n-bit flash consists of 2^n-1 comparators with negative inputs evenly spaced at 1LSB increments from the bottom to the top of the reference ladder. For n = 8, there will be 255 comparators.

For any input voltage, all the comparators with negative inputs connected to the reference ladder below the input voltage will have outputs of 1, and all comparators with negative inputs above the input voltage will have outputs of 0. Decode logic is provided to convert this information into a parallel n-bit digital word (the output) corresponding to the number of LSBs (minus 1) that the input voltage is above the level set at the bottom of the ladder.

Finally, the comparators contain latch circuitry and are clocked. This allows the comparators to function as described above when, for example, clock is low. When clock goes high (samples) the comparator will latch and hold its state until the clock goes low again.

Track/Hold

As with all ADCs, if the input waveform is changing rapidly during the conversion the effective bits and SNR will decrease. The MAX100 has an internal track/hold (T/H) that increases attainable effective-bits performance and allows more accurate capture of analog data at high conversion rates.

The internal T/H circuit provides two important circuit functions for the MAX100:

1) Its nominal voltage gain of 4 reduces the input driving signal to ±270mV differential (assuming a ±1.02V reference).
2) It provides a differential 50Ω input that allows easy interface to the MAX100.

Data Flow

The MAX100 contains an internal T/H amplifier that stores the analog input voltage for the ADC to convert. The differential inputs AIN+ and AIN- are tracked continuously between data samples. When a negative CLK edge is applied, the T/H enters hold mode (Figure 5). When CLK goes low, the most recent sample is presented to the ADC's input comparators. Internal processing of the sampled data is delayed for several clock cycles before it is available at outputs AData or BData. All output data is timed with respect to DCLK and $\overline{\text{DCLK}}$ (Figures 1–4).

Applications Information

Analog Input Ranges

Although the normal operating range is ±270mV, the MAX100 can be operated with up to ±500mV on each input with respect to ground. This extended input level includes the analog signal and any DC common-mode voltage.

To obtain a full-scale digital output with differential input drive, a nominal +270mV must be applied between AIN+ and AIN-. That is, AIN+ = +135mV and AIN- = -135mV (with no DC offset). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential -270mV drive, occurs when AIN+ = -135mV and AIN- = +135mV. Table 2 shows how the output of the converter stays at all ones (full scale) when over ranged or all zeros (zero scale) when under ranged.

For single-ended operation:

1) Apply a DC offset to one of the analog inputs, or leave one input open. (Both AIN+ and AIN- are terminated internally with 50Ω to analog ground.)
2) Drive the other input with a ±270mV + offset to obtain either full- or zero-scale digital output. If a DC common-mode offset is used, the total voltage swing allowed is ±500mV (analog signal plus offset with respect to ground).

Table 1. Input Voltage Range

INPUT	AIN+** (mV)	AIN-** (mV)	OUTPUT CODE	MSB to LSB
Differential	+135	-135	11111111	full scale
	0	0	10000000	mid scale
	-135	+135	00000000	zero scale
Single Ended	+270	0	11111111	full scale
	0	0	10000000	mid scale
	-270	0	00000000	zero scale

**An offset V_{IO}, as specified in the DC electrical parameters, may be present at the input. Compensate for this offset by either adjusting the reference voltage (VA_{RT} or VA_{RB}), or introducing an offset voltage in one of the input terminals AIN + or AIN-.

Table 2. Output Mode Control

DIV	MOD	A=B	DCLK* (MHz)	MODE	DESCRIPTION
0	X	0	250	Divide by 1	Data appears on AData only, BData port inactive (Figure 3).
0	X	1	250	Divide by 1	AData identical to BData (Figure 3).
1	0	0	125	Divide by 2	8:16 demultiplexer mode. AData and BData ports are active. BData carries older sample and AData carries most recent sample (Figure 4).
1	0	1	125	Divide by 2	AData and BData ports are active, both carry identical sampled data. Alternate samples are taken but discarded.
1	1	0	50	Divide by 5	AData port updates data on 5th input CLK. BData port inactive. Other 4 sampled data points are discarded.
1	1	1	50	Divide by 5	AData and BData ports are both active with identical data. Data is updated on output ports every 5th input clock (CLK). The other 4 samples are discarded.

*Input clocks (CLK, $\overline{CLK}$) = 250MHz for all above combinations. In divide-by-2 or divide-by-5 mode the output clock DCLK will always be a 50% duty-cycle signal. In divide-by-1 mode DCLK will have the same duty cycle as CLK.

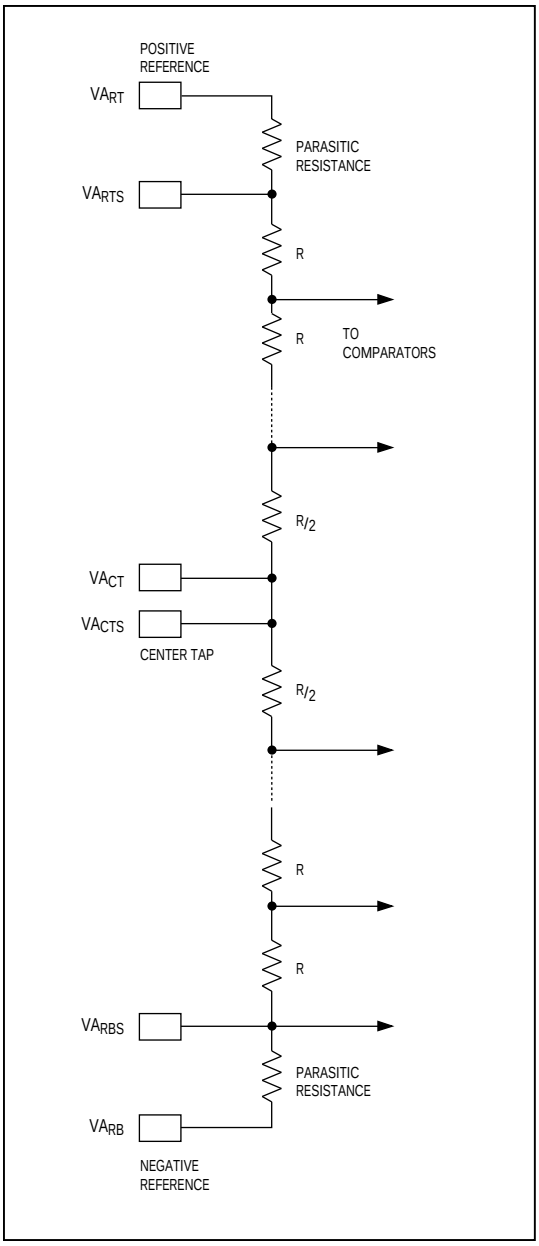


Figure 6. Reference Ladder String

Reference

The ADC's reference resistor is a Kelvin-sensed, center-tapped resistor string that sets the ADC's LSB size and dynamic operating range. Normally, the top and bottom of this string are driven with an op amp, and the center tap is left open. However, driving the center tap is an effective way to modify the output coding to provide a user-defined bilinear response. The buffer amplifier used to drive the top and bottom inputs will need to supply approximately 18mA due to the resistor string impedance of 116Ω minimum. A reference voltage of ±1.02V is normally applied to inputs VA_{RT} and VA_{RB}. This reference voltage can be adjusted up to ±1.4V to accommodate extended input requirements (accuracy specifications are guaranteed with ±1.02V references). The reference input VA_{RTS}, VA_{RBS}, and VA_{CTS} allow Kelvin sensing of the applied voltages to increase precision.

An RC network at the ADC's reference terminals is needed for best performance. This network consists of a 33Ω resistor connected in series with the op amp output that drives the reference. A 0.47µF capacitor must be connected near the resistor at the op amp's output (see *Typical Operating Circuit*). This resistor and capacitor combination should be located within 0.5 inches of the MAX100 package. Any noise on these pins will directly affect the code uncertainty and degrade the ADC's effective-bits performance.

CLK and DCLK

All input and output clock signals are differential. The input clocks, CLK and $\overline{CLK}$, are the primary timing signals for the MAX100. CLK and $\overline{CLK}$ are fed to the internal circuitry from pins 2 & 3 or pins 62 & 61 through an internal 50Ω transmission line. One pair of CLK/$\overline{CLK}$ inputs should be driven and the other pair terminated by 50Ω to -2V. Either pair can be used as the driven inputs (input lines are balanced) for easy circuit connection. A minimum pulse width (t_{PWL}) is required for CLK and $\overline{CLK}$ (Figures 1–4).

For best performance and consistent results, use a low phase-jitter clock source for CLK and $\overline{CLK}$. Phase jitter larger than 2ps from the input clock source reduces the converter's effective-bits performance and causes inconsistent results.

DCLK and $\overline{DCLK}$ are output clock signals derived from the input clocks and are used for external timing of the AData and BData outputs. The MAX100 is characterized to work with maximum input clock frequencies of 250MHz (Table 1). See *Typical Operating Circuit.*

Output Mode Control

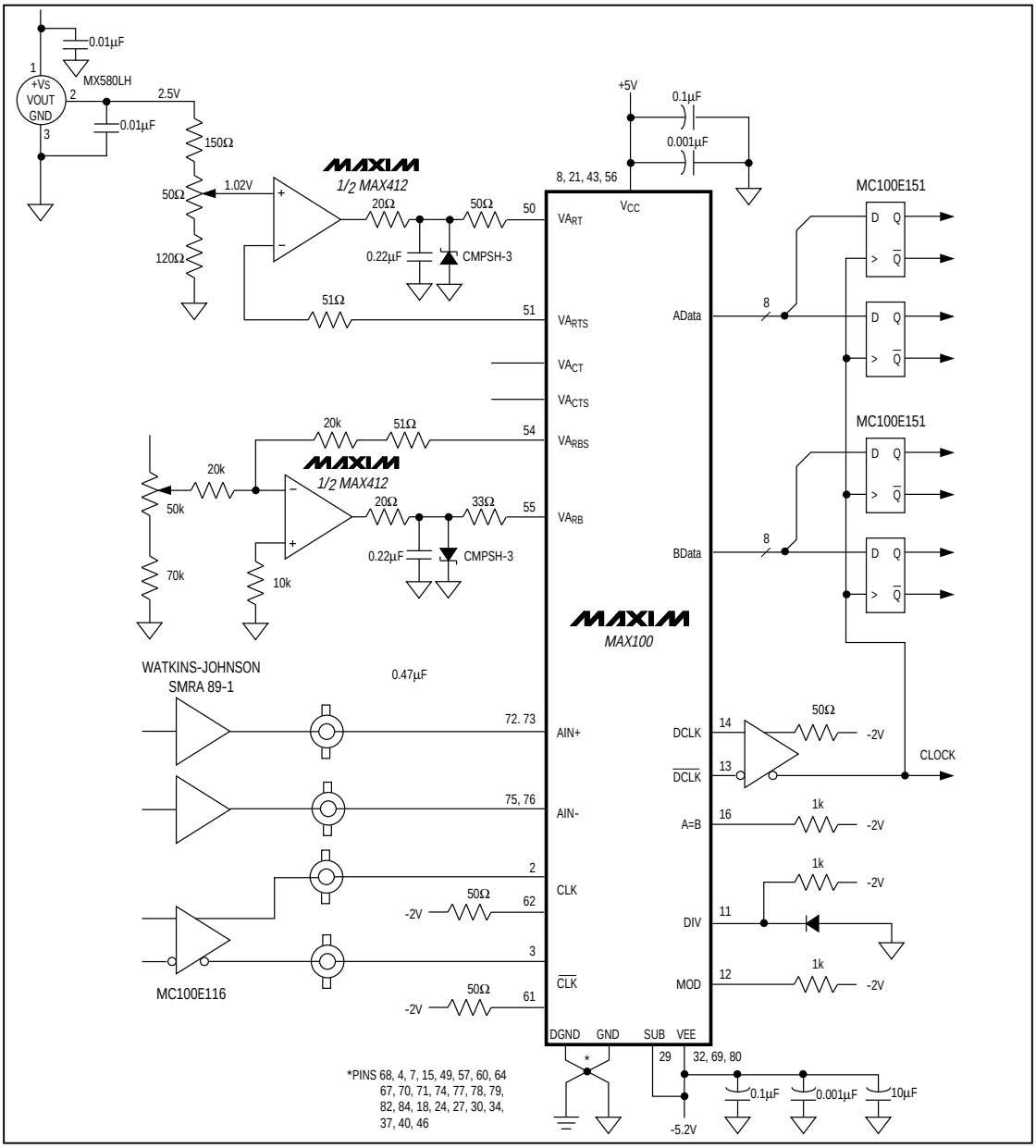
DIV, MOD, and A=B are input pins that determine the operating mode of the two output data paths. Six options are available (Table 1). A typical operating configuration (8:16 demultiplexer mode) is set by 1 on DIV, 0 on MOD, and 0 on A=B. This will give the most recent sample at AData with the older data on BData. Both outputs are synchronous and are at half the input clock rate. To terminate the control inputs, use a resistor to -2V or the equivalent circuit resistor combination from DGND to -5.2V up to 1kΩ. When using a diode pull-up to tie an input high, bias the diode "on" with a pull-down resistor to avoid input voltage excursions close to ground. The control inputs are compatible with standard ECL 10K logic levels over temperature.

Layout, Grounding, and Power Supplies

The MAX100 is designed with separate analog and digital ground connections to isolate high-current digital noise spikes. The high-current digital ground, DGND, is connected to the collectors of the output emitter follower transistors. The low-current ground connection is GND, which is a combination of the analog ground and the ground of the low-current digital decode section. The DGND and GND connections should be at the same DC level, and should be connected at only one location on the board. This will provide better noise immunity and highest device accuracy. A ground plane is recommended.

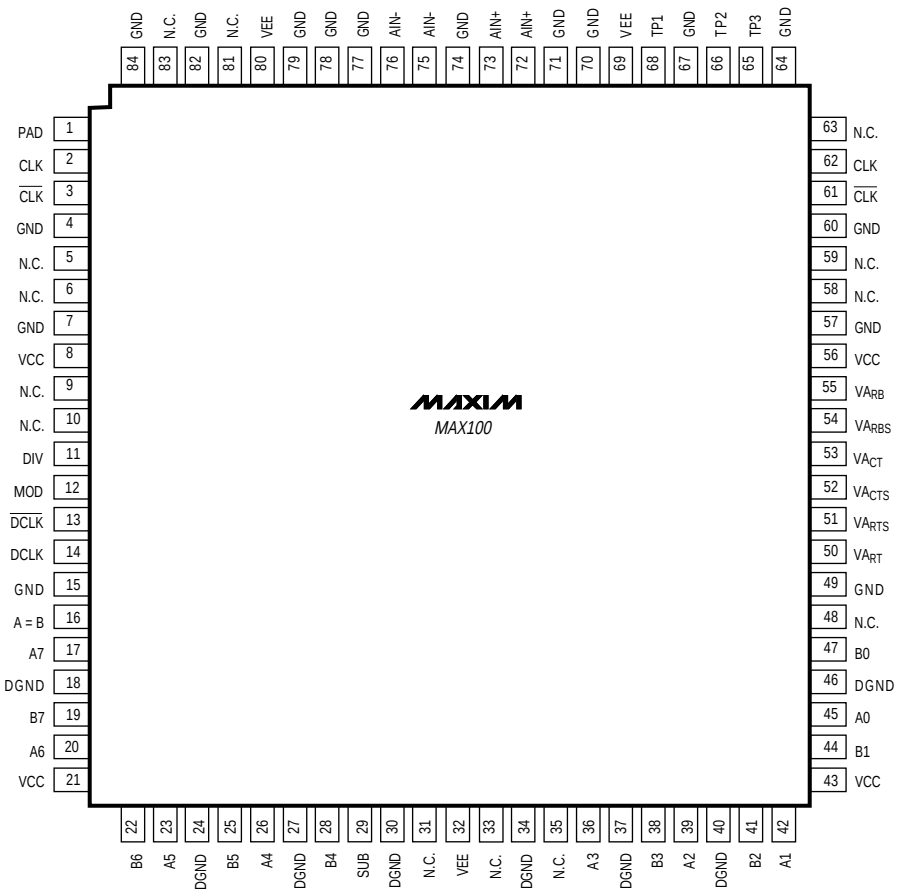
A +5V ±5% supply as well as a -5.2V ±5% supply is needed for proper operation. Bypass the VEE and VCC supply pins to GND with high-quality 0.1µF and 0.001µF ceramic capacitors located as close to the package as possible. An evaluation kit with a suggested layout is available.

Typical Operating Circuit



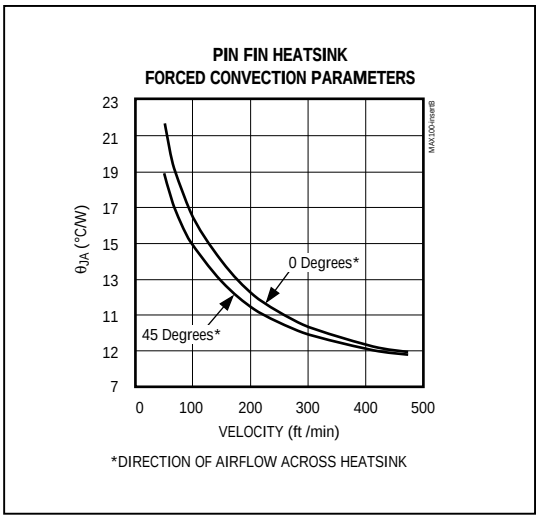
Pin Configuration

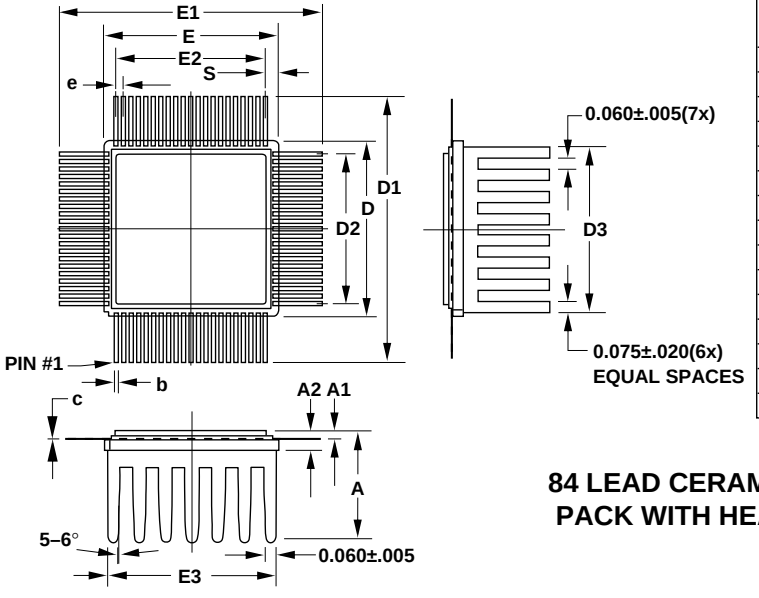
TOP VIEW



Ceramic Flat Pack

Package Information





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.272	18.288	0.680	0.720
A1	1.041	1.270	0.041	0.050
A2	3.048	3.302	0.120	0.130
b	0.406	0.508	0.016	0.020
C	0.228	0.279	0.009	0.011
D	29.184	29.794	1.149	1.173
D1	44.196	44.704	1.740	1.760
D2	25.298	25.502	0.996	1.004
D3	28.448	28.829	1.120	1.135
e	1.270 BSC		0.050 BSC	
E	29.184	29.794	1.149	1.173
E1	44.196	44.704	1.740	1.760
E2	25.298	25.502	0.996	1.004
E3	28.194	28.702	1.110	1.130
S	1.930	2.184	0.076	0.086

84 LEAD CERAMIC FLAT PACK WITH HEAT SINK