**DALLAS MAXIM**
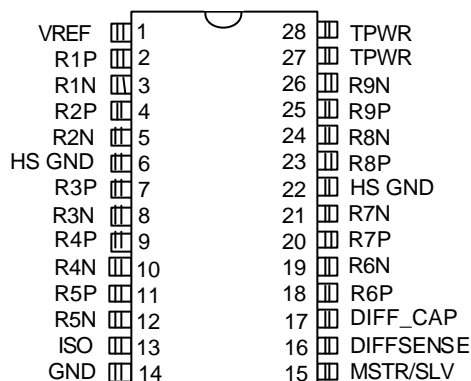
# DS2120
# Ultra3 LVD SCSI Terminator

www.maxim-ic.com

## FEATURES
- Fully compliant with Ultra3, Ultra160, Ultra320, and Ultra2 (LVD only) SCSI
- Provides low-voltage differential (LVD) termination for nine signal line pairs
- Zero-temperature coefficient-termination resistors
- Auto-select of LVD termination
- 5% tolerance on LVD termination resistance
- Low power-down capacitance of 3pF
- Built-in mode change filter/delay
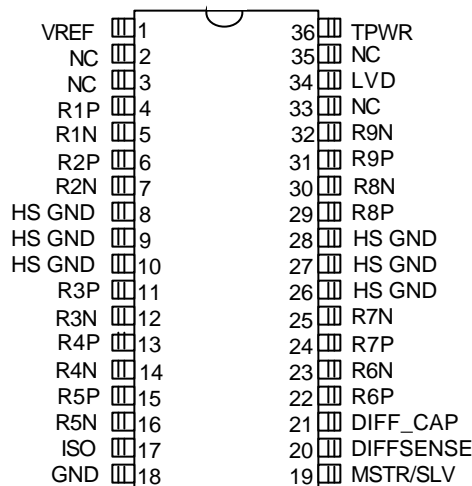- On-board thermal-shutdown circuitry
- SCSI bus hot-plug compatible

## APPLICATIONS
- Raid Systems
- SCSI Host Bus Adapter Cards (HBA)
- Servers
- SCSI Cables
- Network Attached Storage (NAS)
- Storage Area Networks (SANs)

## ORDERING INFORMATION
DS2120E     28-Pin TSSOP     0°C to +70°C
DS2120B     36-Pin SSOP     0°C to +70°C

## PIN ASSIGNMENT

```
VREF     1        28  TPWR
R1P      2        27  TPWR
R1N      3        26  R9N
R2P      4        25  R9P
R2N      5        24  R8N
HS GND   6        23  R8P
R3P      7        22  HS GND
R3N      8        21  R7N
R4P      9        20  R7P
R4N     10        19  R6N
R5P     11        18  R6P
R5N     12        17  DIFF_CAP
ISO     13        16  DIFFSENSE
GND     14        15  MSTR/SLV
```
DS2120E 28-Pin TSSOP

```
VREF     1        36  TPWR
NC       2        35  NC
NC       3        34  LVD
R1P      4        33  NC
R1N      5        32  R9N
R2P      6        31  R9P
R2N      7        30  R8N
HS GND   8        29  R8P
HS GND   9        28  HS GND
HS GND  10        27  HS GND
R3P     11        26  HS GND
R3N     12        25  R7N
R4P     13        24  R7P
R4N     14        23  R6N
R5P     15        22  R6P
R5N     16        21  DIFF_CAP
ISO     17        20  DIFFSENSE
GND     18        19  MSTR/SLV
```
DS2120B 36-Pin SSOP

## DESCRIPTION
The DS2120 Ultra3 LVD SCSI terminator is a low-voltage differential (LVD) terminator. If the device is connected in an LVD-only bus, the DS2120 uses LVD termination. If any single-ended (SE) or high-voltage differential (HVD) devices are connected to the bus, the DS2120 disconnects from the bus. This is accomplished inside the part automatically by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2120 integrates two current sources with nine precision resistor strings. Three DS2120 terminators are needed for a wide SCSI bus.

---

**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://dbserv.maxim-ic.com/errata.cfm.

## REFERENCE DOCUMENTS

Small Computer Systems Interface (SCSI-3)   SCSI Parallel Interface (SPI)         Project: 0855-M, 1995
Small Computer Systems Interface (SCSI-3)   SCSI Parallel Interface 2 (SPI-2)   Project: 1142-M, 1998
Small Computer Systems Interface (SCSI-3)   SCSI Parallel Interface 3 (SPI-3)   Project: 1302-D, 1999
Small Computer Systems Interface (SCSI-3)   SCSI Parallel Interface 4 (SPI-4)   Project: 1365-D, 200$x$

**Available from:**
American National Standards Institute (ANSI)   Phone: 212-642-4900
Global Engineering Documents  15 Inverness Way East; Englewood, CO 80112   Phone: 800-854-7179

## FUNCTIONAL DESCRIPTION

The DS2120 combines LVD termination with DIFFSENSE sourcing and detection.

LVD termination is provided by a laser-trimmed resistor biased with two current sources and a common-mode voltage source, generated from a bandgap reference of 1.25V. The configuration is a y-type terminator with a 105Ω differential and 150Ω common-mode resistance. A fail-safe bias of 112mV is maintained when no drivers are connected to the SCSI bus. In non-LVD mode, the resistors are isolated from the bus.

The DIFF_CAP pin of DS2120 monitors the DIFFSENS line to determine the proper operating mode of the device. If the voltage on the DIFF_CAP is between 0.7V and 1.9V, the device enters LVD mode after the mode-change delay. If the voltage at the DIFF_CAP later crosses one of the thresholds, the DS2120 again changes modes after the mode-change delay. The mode-change delay is the same when changing in or out of LVD mode. A new mode change can start anytime after a previous mode change has been detected. These modes are the following:

**LVD Mode:** LVD termination is provided by a precision laser-trimmed resistor string with two current sources. This configuration yields a 105Ω differential and 150Ω common-mode impedance. A fail-safe bias of 112mV is maintained when no drivers are connected to the SCSI bus.

**SE Isolation Mode:** The DS2120 identifies that there is a SE (single-ended) device on the SCSI bus and isolates the termination pins from the bus.

**HVD Isolation Mode:** The DS2120 identifies that there is an HVD device on the SCSI bus and isolates the termination pins from the bus.

When ISO is pulled high, the termination pins are isolated from the SCSI bus and VREF remains active. The mode-change delay/filter is still active and the LVD pin continues to indicate the correct bus mode. During thermal shutdown, the termination pins are isolated from the SCSI bus and VREF becomes high impedance. The DIFFSENS driver is shut down during either of these two events. The DIFF_CAP receiver is disabled and the LVD goes low, indicating a non-LVD condition.

To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and $V_{DD}$ lines should be bypassed locally. A 2.2µF capacitor and a 0.01µF high-frequency capacitor are recommended between TPWR and ground and placed as close as possible to the DS2120. The DS2120 should be placed as close as possible to the SCSI connector to minimize signal and power trace length, thereby lessening input capacitance and reflections that can degrade the bus signals.

To maintain the specified regulation, a 4.7µF capacitor is required between the VREF pin and ground of each DS2120. A high-frequency cap (0.1µF ceramic recommended) can also be placed on the VREF pin in applications that use fast rise/fall-time drivers. A typical SCSI bus configuration is shown in Figure 2.

**DIFFSENS Noise Filtering:** The DS2120 incorporates a digital filter to remove high-frequency transients on the DIFFSENS control line, thereby eliminating erroneous switching between modes. This filter eliminates the need for the external capacitor and resistor, which previously performed this function. The external filter can be used in addition to the digital filter if the DS2120 and DS2118M or DS2119M are to be used interchangeably.

## NOTES:
1) DIFFSENS: Refers to the SCSI bus signal.
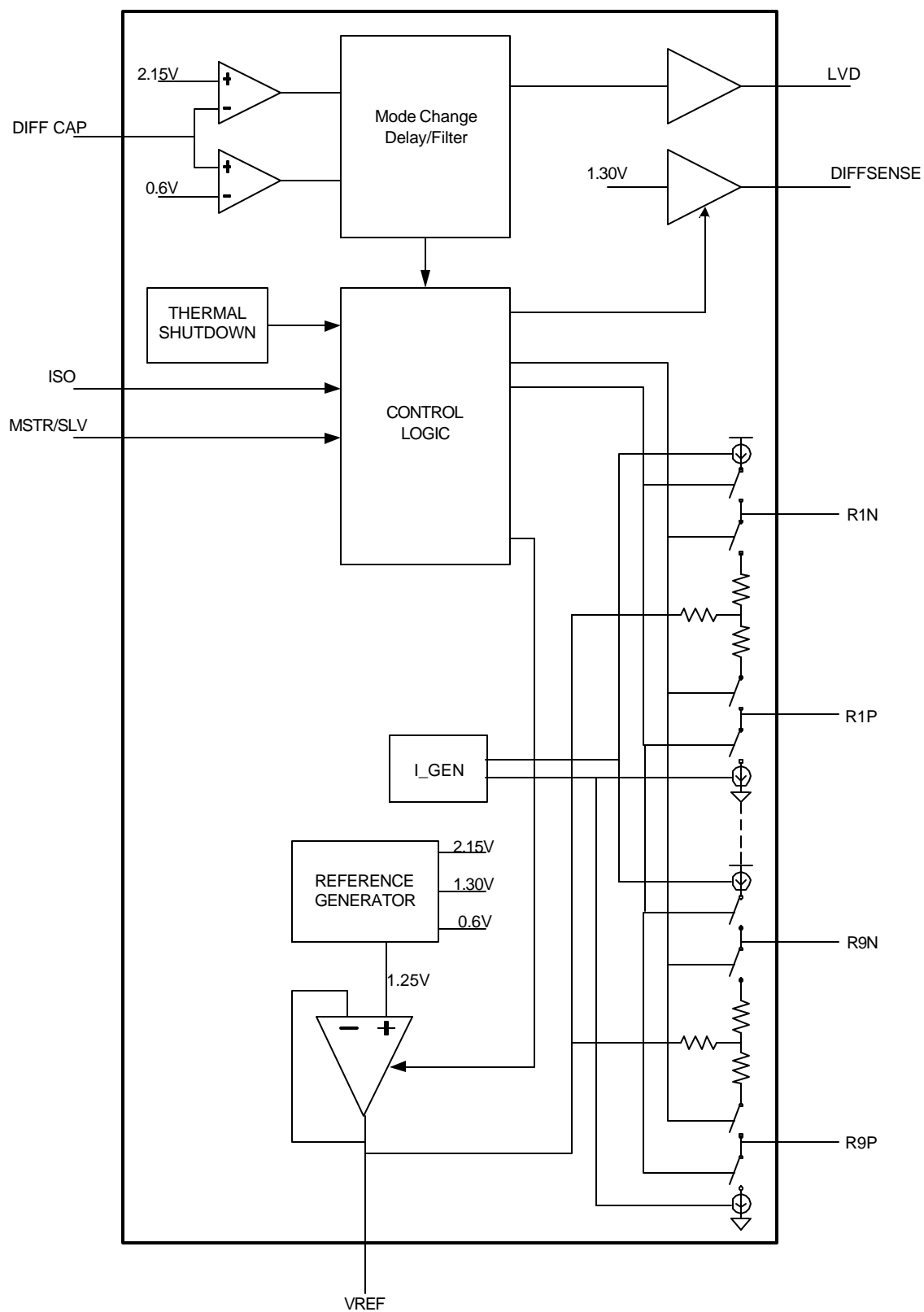2) DIFFSENSE: Refers to the Dallas Semiconductor pin name and internal circuitry relating to differential sensing.

# Figure 1. **BLOCK DIAGRAM**
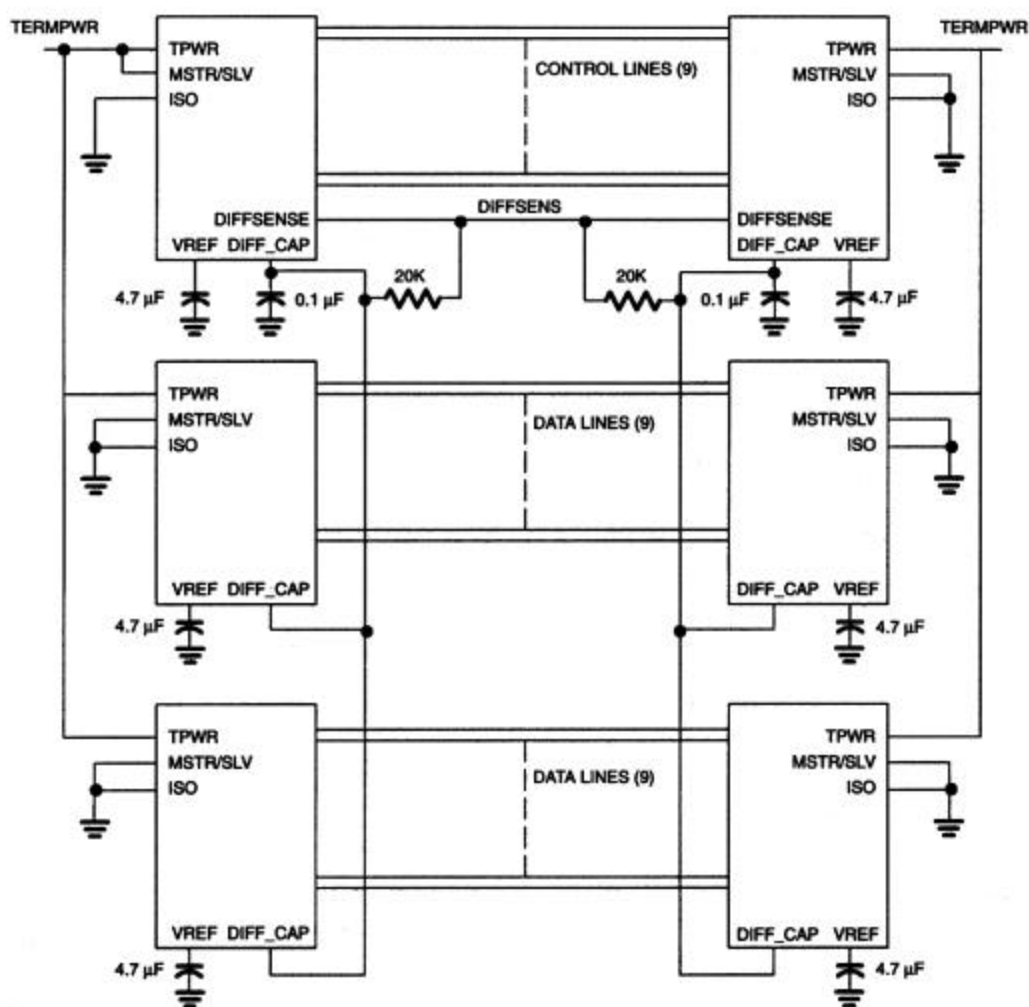
# Figure 2. **SCSI BUS CONFIGURATION**

# Table 1. **PIN DESCRIPTION**

### DS2120E 28-Pin TSSOP

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | VREF | **Regulator Output Voltage.** 1.25V reference in LVD mode; must be decoupled with a 4.7µF cap. |
| 2–5, 7–12, 18–21, 23–26 | RxP, RxN | **Signal Termination.** Connect to SCSI bus signal lines. |
| 6, 22 | HS_GND | **Heat Sink Ground.** Internally connected to the mounting pad. Should be connected to ground. |
| 13 | ISO | **Isolation.** When pulled high, terminating resistors and biasing current sources are isolated from the SCSI bus. |
| 14 | GND | **Signal Ground.** |
| 15 | MSTR/SLV | **Master/Slave.** Mode select for the noncontrolling terminator. When pulled high (MSTR), the DIFFSENS driver is enabled. |
| 16 | DIFFSENSE | **DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line. |
| 17 | DIFF_CAP | **DIFFSENSE Capacitor.** Connect a 0.1µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus. |
| 27, 28 | TPWR | **Termination Power.** Connect to the SCSI TERMPWR line and decouple with 2.2µF capacitor. |

### DS2120B 36-Pin SSOP

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | VREF | **Regulator Output Voltage.** 1.25V reference in LVD mode; must be decoupled with a 4.7µF cap. |
| 2, 3, 33, 35 | NC | **No Connect.** Do not connect pins. |
| 4–7, 11–16, 22–25, 29–32 | RxP, RxN | **Signal Termination.** Connect to SCSI bus signal lines. |
| 8–10, 26–28 | HS_GND | **Heat Sink Ground.** Internally connected to the mounting pad. Should be connected to ground. |
| 17 | ISO | **Isolation.** When pulled high, terminating resistors and biasing current sources are isolated from the SCSI bus. |
| 18 | GND | **Signal Ground.** |
| 19 | MSTR/SLV | **Master/Slave.** Mode select for the noncontrolling terminator. When pulled high (MSTR), the DIFFSENS driver is enabled. |
| 20 | DIFFSENSE | **DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line. |
| 21 | DIFF_CAP | **DIFFSENSE Capacitor.** Connect a 0.1µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single ended) on the SCSI bus. |
| 34 | LVD | **Low-Voltage Differential.** Output of DIFFSENSE receiver; output high indicates LVD bus operation . |
| 36 | TPWR | **Termination Power.** Connect to the SCSI TERMPWR line and decouple with 2.2µF capacitor. |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Termpower Voltage, LVD Mode | $V_{TPWR}$ (LVD) | 2.7 | | 5.5 | V | |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 13 |
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{tpwr} + 0.3$ | V | 13 |
| Operating Temperature | $V_{AMB}$ | 0 | | 70 | °C | |

## LOW-VOLTAGE DIFFERENTIAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Differential Mode Termination Resistance | $R_{DM}$ | 100 | | 110 | ? | |
| Common Mode Termination Resistance | $R_{CM}$ | 110 | | 190 | ? | |
| Differential Mode Bias | $V_{DM}$ | 100 | | 125 | mV | 2 |
| Common Mode Bias | $V_{CM}$ | 1.125 | | 1.375 | V | |
| Output Capacitance | $C_{OUT}$ | | | 3 | pF | 1 |
| Mode-Change Delay | $M_{CD}$ | 0.66 | 1.25 | 2 | ms | 1, 12 |

## DC CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Termpower Current | $I_{TPMR}$ | | 12 | 30 | mA | 2, 3 |
| Input Leakage High | $I_{IH}$ | -1.0 | | | µA | 14, 15 |
| Input Leakage Low | $I_{IL}$ | | | 1.0 | µA | 14, 15 |
| Output Current High | $I_{OH}$ | | | -1.0 | mA | 4, 6 |
| Output Current Low | $I_{OL}$ | 4.0 | | | mA | 5, 6 |
| DIFF_CAP LVD Operating Range | $V_{LVDOR}$ | 0.7 | | 1.9 | V | |
| DIFFSENSE Driver Output Voltage | $V_{DSO}$ | 1.2 | | 1.4 | V | 7, 8 |
| DIFFSENSE Driver Source Current | $I_{DSH}$ | 5 | | 15 | mA | 7, 9, 11 |
| DIFFSENSE Driver Sink Current | $I_{DSL}$ | 20 | | 200 | µA | 7, 10, 11 |
| MSTR/SLV Input Leakage | $I_{MSTRSLV}$ | -6.5 | | +125 | µA | |
| ISO Input Leakage | $I_{ISO}$ | -125 | | +6.5 | µA | |
| Thermal Shutdown | | | 150 | | °C | |

## REGULATOR CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| VREF Line Regulation | $LI_{REG}$ | | 1.0 | 2.0 | % | |
| VREF Load Regulation | $LO_{REG}$ | | 1.3 | 3.5 | % | |
| VREF Current Limit | $I_{LIM}$ | | | 200 | mA | |
| VREF Sink Current | $I_{SINK}$ | | | 200 | mA | |

## NOTES:

1) Guaranteed by design.
2) All lines open.
3) ISO = 1
4) $V_{OUT}$ = 2.4V
5) $V_{OUT}$ = 0.4V
6) LVD pin only.
7) MSTR/SLV = 1
8) $I_{DS}$ = 0 to 5mA
9) $V_{DSO}$ = 0.0V
10) $V_{DSO}$ = 2.75V
11) TPWR = 5.5V
12) $M_{CD}$ is extended by the RC time constant formed by the resistor connected from DIFFSENSE to DIFF_CAP and the capacitor connected from DIFF_CAP to ground.
13) MSTR/SLV and ISO pins.
14) Terminator pins only.
15) DIFFCAP pin only.

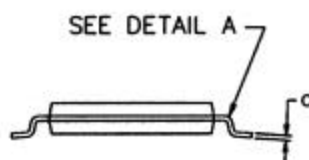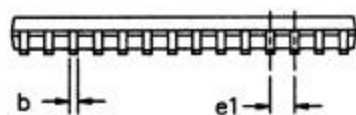## DS2120E 28-PIN TSSOP PACKAGE
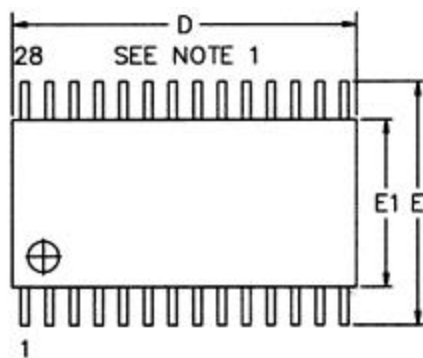


**NOTES:**

1) Dimension D does not include mold mismatch, flash, or protrusions. Mold mismatch, flash, and protrusions shall not exceed 0.15 per side.

2) Dimension B does not include dambar protrusion. Dambar protrusion shall not be located on the lower radius of the foot.
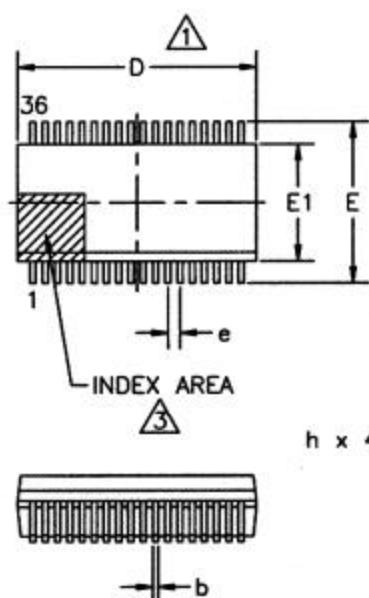




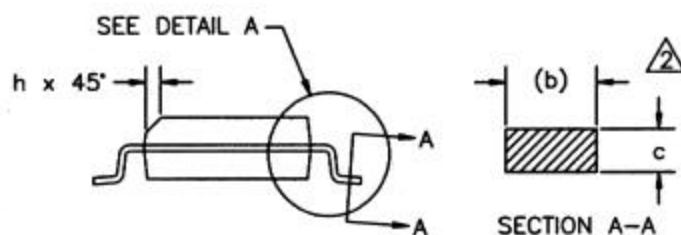| DIM | MIN | MAX |
|-----|-----|-----|
| A | - | 1.10 |
| A1 | 0.05 | - |
| A2 | 0.75 | 1.05 |
| c | 0.09 | 0.20 |
| L | 0.50 | 0.75 |
| e1 | 0.65 BSC | |
| b | 0.18 | 0.30 |
| D | 9.60 | 9.80 |
| E1 | 4.40 BSC | |
| E | 6.20 | 6.60 |

DETAIL A
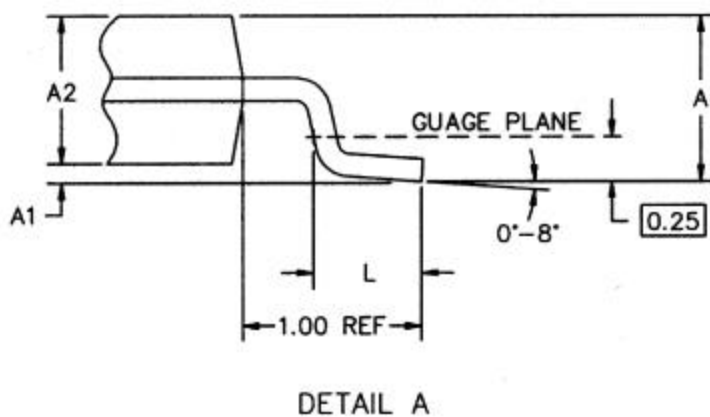
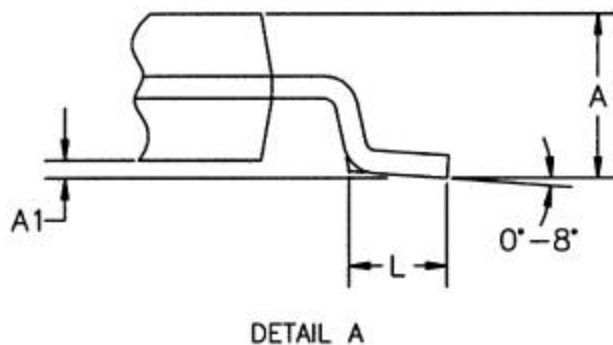Dimensions are in millimeters (mm).

## DS2120B 36-PIN SSOP PACKAGE

### NOTES:

1) Dimensions D and E1 include mold mismatch, but do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.254mm per side.
2) Section A-A dimensions apply to the flat section of the lead between 0.13mm to 0.25mm from the lead tip.
3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.

| DIM | MIN | MAX |
|-----|-----|-----|
| A | 2.44 | 2.64 |
| A1 | 0.12 | - |
| b | 0.29 | 0.43 |
| c | 0.23 | 0.32 |
| D | 15.20 | 15.54 |
| E | 10.11 | 10.52 |
| E1 | 7.40 | 7.60 |
| e | 0.80 BSC | |
| h | 0.25 | 0.71 |
| L | 0.51 | 1.02 |

Dimensions are in millimeters (mm).