



## HYS 64/72V32300GU SDRAM-Modules

### 3.3 V 32M x 64/72-Bit, 256MByte SDRAM Modules 168-pin Unbuffered DIMM Modules

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications using 256Mbit technology.
- PC100-222, PC133-333 and PC133-222 versions
- One bank 32M x 64 and 32M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- Programmed Latencies:
- Single + 3.3 V ( $\pm 0.3$  V) power supply
- Programmable  $\overline{\text{CAS}}$  Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Uses Infineon 256 Mbit SDRAM components in 32M x 8 organization and TSOPII-54 packages
- Gold contact pads, card size: 133.35 mm x 31.75 mm x 3.00 mm (JEDEC MO-161-BA)

| Product Speed |       | CL | $t_{\text{RCD}}$ | $t_{\text{RP}}$ |
|---------------|-------|----|------------------|-----------------|
| -7            | PC133 | 2  | 2                | 2               |
| -7.5          | PC133 | 3  | 3                | 3               |
| -8            | PC100 | 2  | 2                | 2               |

- SDRAM Performance:

|                 |                        | -7 / -7.5 | -8    | Unit |
|-----------------|------------------------|-----------|-------|------|
|                 |                        | PC133     | PC100 |      |
| $f_{\text{CK}}$ | Clock Frequency (max.) | 133       | 100   | MHz  |
| $t_{\text{AC}}$ | Clock Access Time      | 5.4       | 6     | ns   |

#### Description

The HYS 64V32300GU and HYS 72V32300GU are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 32M x 64 and 32M x 72 in 1 memory bank high speed memory arrays designed with 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -7 speed sorted 32M x 8 SDRAM devices in TSOP54 packages to meet the PC133-222 requirement, -7.5 components for PC133-333 and -8 components for the standard PC100 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's module specification. The DIMMs have a serial presence detect, implemented with a serial E<sup>2</sup>PROM using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25" (31.75 mm) height.

**Ordering Information**

| Type                                          | Code          | Package      | Descriptions                           | Module Height |
|-----------------------------------------------|---------------|--------------|----------------------------------------|---------------|
| HYS 64V32300GU-7-D                            | PC133-222-520 | L-DIM-168-33 | PC133 32M × 64 1 bank SDRAM module     | 1.25"         |
| HYS 72V32300GU-7-D                            | PC133-222-520 | L-DIM-168-33 | PC133 32M × 72 1 bank ECC-SDRAM module | 1.25"         |
| HYS 64V32300GU-7.5-C2<br>HYS 64V32300GU-7.5-D | PC133-333-520 | L-DIM-168-33 | PC133 32M × 64 1 bank SDRAM module     | 1.25"         |
| HYS 72V32300GU-7.5-C2<br>HYS 72V32300GU-7.5-D | PC133-333-520 | L-DIM-168-33 | PC133 32M × 72 1 bank ECC-SDRAM module | 1.25"         |
| HYS 64V32300GU-8-C2                           | PC100-222-620 | L-DIM-168-33 | PC100 32M × 64 1 bank SDRAM module     | 1.25"         |
| HYS 72V32300GU-8-C2                           | PC100-222-620 | L-DIM-168-33 | PC100 32M × 72 1 bank ECC-SDRAM module | 1.25"         |

*Note: All part numbers end with a place code designating the die revision. Consult factory for current revision. Example: HYS 64V32300GU-8-C2, indicating Rev. C2 dies are used for SDRAM components.*

**Pin Definitions and Functions**

|                  |                                    |                                     |                                     |
|------------------|------------------------------------|-------------------------------------|-------------------------------------|
| A0 - A12         | Address Inputs                     | CLK0 - CLK3                         | Clock Input                         |
| BA0, BA1         | Bank Selects                       | DQMB0 - DQMB7                       | Data Mask                           |
| DQ0 - DQ63       | Data Input/Output                  | $\overline{CS0}$ , $\overline{CS2}$ | Chip Select                         |
| CB0 - CB7        | Check Bits (x72 organisation only) | $V_{DD}$                            | Power (+ 3.3 V)                     |
| $\overline{RAS}$ | Row Address Strobe                 | $V_{SS}$                            | Ground                              |
| $\overline{CAS}$ | Column Address Strobe              | SCL                                 | Clock for Presence Detect           |
| $\overline{WE}$  | Read/Write Input                   | SDA                                 | Serial Data Out for Presence Detect |
| CKE0             | Clock Enable                       | N.C./DU                             | No Connection                       |

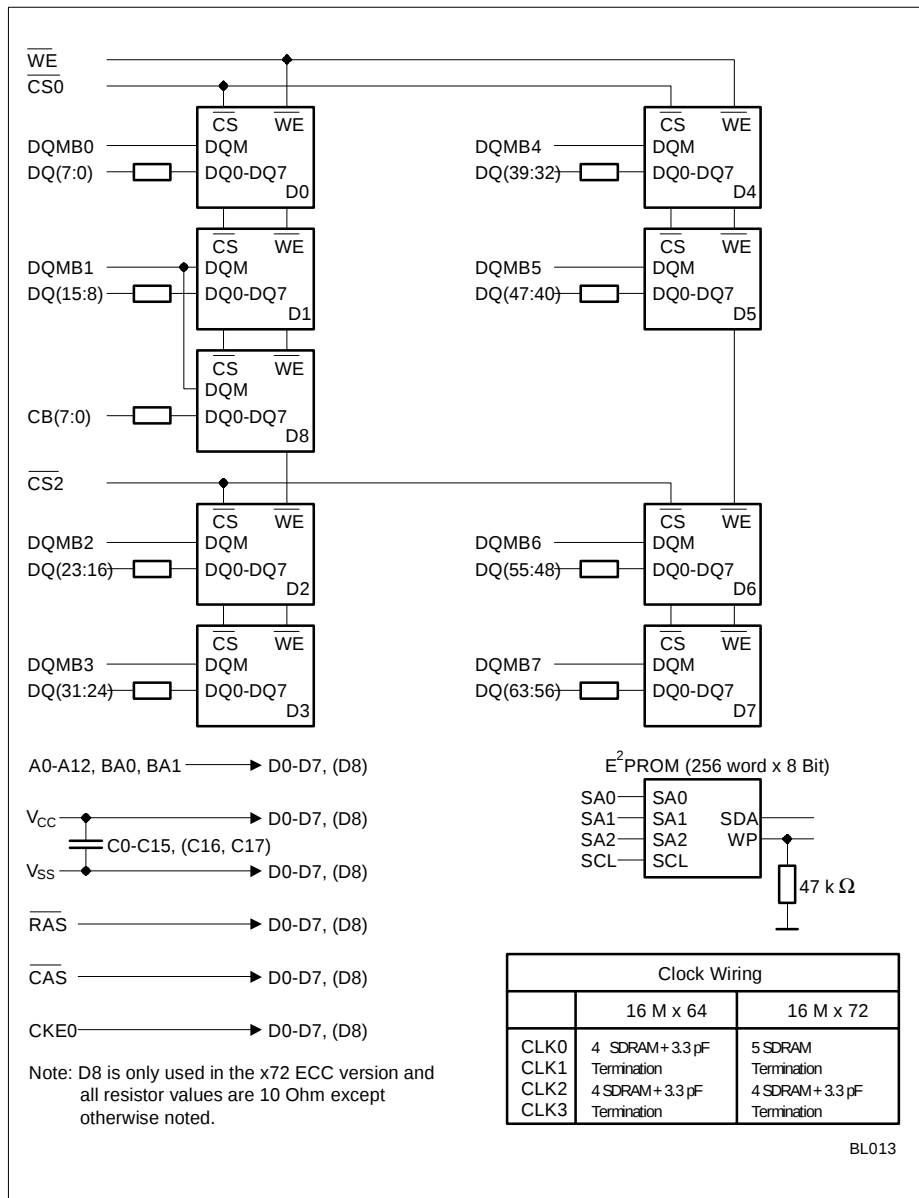
**Address Format**

|             | Part Number      | Rows | Columns | Bank Select | Refresh | Period | Interval    |
|-------------|------------------|------|---------|-------------|---------|--------|-------------|
| 32M × 64/72 | HYS64/72V32300GU | 13   | 10      | 2           | 8k      | 64 ms  | 7.8 $\mu$ s |

**Pin Configuration**

| PIN# | Symbol          | PIN# | Symbol          | PIN# | Symbol          | PIN# | Symbol          |
|------|-----------------|------|-----------------|------|-----------------|------|-----------------|
| 1    | V <sub>SS</sub> | 43   | V <sub>SS</sub> | 85   | V <sub>SS</sub> | 127  | V <sub>SS</sub> |
| 2    | DQ0             | 44   | DU              | 86   | DQ32            | 128  | CKE0            |
| 3    | DQ1             | 45   | CS2             | 87   | DQ33            | 129  | N.C.            |
| 4    | DQ2             | 46   | DQMB2           | 88   | DQ34            | 130  | DQMB6           |
| 5    | DQ3             | 47   | DQMB3           | 89   | DQ35            | 131  | DQMB7           |
| 6    | V <sub>DD</sub> | 48   | DU              | 90   | V <sub>DD</sub> | 132  | N.C.            |
| 7    | DQ4             | 49   | V <sub>DD</sub> | 91   | DQ36            | 133  | V <sub>DD</sub> |
| 8    | DQ5             | 50   | N.C.            | 92   | DQ37            | 134  | N.C.            |
| 9    | DQ6             | 51   | N.C.            | 93   | DQ38            | 135  | N.C.            |
| 10   | DQ7             | 52   | N.C. (CB2)      | 94   | DQ39            | 136  | CB6             |
| 11   | DQ8             | 53   | N.C. (CB3)      | 95   | DQ40            | 137  | CB7             |
| 12   | V <sub>SS</sub> | 54   | V <sub>SS</sub> | 96   | V <sub>SS</sub> | 138  | V <sub>SS</sub> |
| 13   | DQ9             | 55   | DQ16            | 97   | DQ41            | 139  | DQ48            |
| 14   | DQ10            | 56   | DQ17            | 98   | DQ42            | 140  | DQ49            |
| 15   | DQ11            | 57   | DQ18            | 99   | DQ43            | 141  | DQ50            |
| 16   | DQ12            | 58   | DQ19            | 100  | DQ44            | 142  | DQ51            |
| 17   | DQ13            | 59   | V <sub>DD</sub> | 101  | DQ45            | 143  | V <sub>DD</sub> |
| 18   | V <sub>DD</sub> | 60   | DQ20            | 102  | V <sub>DD</sub> | 144  | DQ52            |
| 19   | DQ14            | 61   | N.C.            | 103  | DQ46            | 145  | N.C.            |
| 20   | DQ15            | 62   | DU              | 104  | DQ47            | 146  | DU              |
| 21   | N.C. (CB0)      | 63   | N.C.            | 105  | N.C. (CB4)      | 147  | N.C.            |
| 22   | N.C. (CB1)      | 64   | V <sub>SS</sub> | 106  | N.C. (CB5)      | 148  | V <sub>SS</sub> |
| 23   | V <sub>SS</sub> | 65   | DQ21            | 107  | V <sub>SS</sub> | 149  | DQ53            |
| 24   | N.C.            | 66   | DQ22            | 108  | N.C.            | 150  | DQ54            |
| 25   | N.C.            | 67   | DQ23            | 109  | N.C.            | 151  | DQ55            |
| 26   | V <sub>DD</sub> | 68   | V <sub>SS</sub> | 110  | V <sub>DD</sub> | 152  | V <sub>SS</sub> |
| 27   | WE              | 69   | DQ24            | 111  | CAS             | 153  | DQ56            |
| 28   | DQMB0           | 70   | DQ25            | 112  | DQMB4           | 154  | DQ57            |
| 29   | DQMB1           | 71   | DQ26            | 113  | DQMB5           | 155  | DQ58            |
| 30   | CS0             | 72   | DQ27            | 114  | N.C.            | 156  | DQ59            |
| 31   | DU              | 73   | V <sub>DD</sub> | 115  | RAS             | 157  | V <sub>DD</sub> |
| 32   | V <sub>SS</sub> | 74   | DQ28            | 116  | V <sub>SS</sub> | 158  | DQ60            |
| 33   | A0              | 75   | DQ29            | 117  | A1              | 159  | DQ61            |
| 34   | A2              | 76   | DQ30            | 118  | A3              | 160  | DQ62            |
| 35   | A4              | 77   | DQ31            | 119  | A5              | 161  | DQ63            |
| 36   | A6              | 78   | V <sub>SS</sub> | 120  | A7              | 162  | V <sub>SS</sub> |
| 37   | A8              | 79   | CLK2            | 121  | A9              | 163  | CLK3            |
| 38   | A10             | 80   | N.C.            | 122  | BA0             | 164  | N.C.            |
| 39   | BA1             | 81   | WP              | 123  | A11             | 165  | SA0             |
| 40   | V <sub>DD</sub> | 82   | SDA             | 124  | V <sub>DD</sub> | 166  | SA1             |
| 41   | V <sub>DD</sub> | 83   | SCL             | 125  | CLK1            | 167  | SA2             |
| 42   | CLK0            | 84   | V <sub>DD</sub> | 126  | A12             | 168  | V <sub>DD</sub> |

Note: Pin names in parantheses are for the x72 ECC versions; example: Pin 106 = (CB5)



**Block Diagram: 32M x 64/72 One Bank SDRAM DIMM Modules**

**Absolute Maximum Ratings**

| Parameter                                   | Symbol            | Limit Values |      | Unit |
|---------------------------------------------|-------------------|--------------|------|------|
|                                             |                   | min.         | max. |      |
| Input / Output voltage relative to $V_{SS}$ | $V_{IN}, V_{OUT}$ | -1.0         | 4.6  | V    |
| Power supply voltage on $V_{DD}$            | $V_{DD}$          | -1.0         | 4.6  | V    |
| Storage temperature range                   | $T_{STG}$         | -55          | +150 | °C   |
| Power dissipation per SDRAM component       | $P_D$             | -            | 1    | W    |
| Data out current (short circuit)            | $I_{OS}$          | -            | 50   | mA   |

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.  
Functional operation should be restricted to recommended operation conditions.  
Exposure to higher than recommended voltage for extended periods of time affect device reliability

**DC Characteristics**

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{DD} = 3.3$  V  $\pm$  0.3 V

| Parameter                                                                               | Symbol     | Limit Values |                | Unit |
|-----------------------------------------------------------------------------------------|------------|--------------|----------------|------|
|                                                                                         |            | min.         | max.           |      |
| Input High Voltage                                                                      | $V_{IH}$   | 2.0          | $V_{DD} + 0.3$ | V    |
| Input Low Voltage                                                                       | $V_{IL}$   | -0.5         | 0.8            | V    |
| Output High Voltage ( $I_{OUT} = -4.0$ mA)                                              | $V_{OH}$   | 2.4          | -              | V    |
| Output Low Voltage ( $I_{OUT} = 4.0$ mA)                                                | $V_{OL}$   | -            | 0.4            | V    |
| Input Leakage Current, any input<br>( $0$ V < $V_{IN}$ < 3.6 V, all other inputs = 0 V) | $I_{I(L)}$ | -40          | 40             | μA   |
| Output Leakage Current<br>(DQ is disabled, $0$ V < $V_{OUT}$ < $V_{DD}$ )               | $I_{O(L)}$ | -40          | 40             | μA   |

**Capacitance**

$T_A = 0$  to  $70$  °C;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

| Parameter                                                                                          | Symbol    | Limit Values     |                  | Unit |
|----------------------------------------------------------------------------------------------------|-----------|------------------|------------------|------|
|                                                                                                    |           | max.<br>32M x 64 | max.<br>32M x 72 |      |
| Input Capacitance<br>(A0 to A11, BA0, BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) | $C_{I1}$  | 65               | 72               | pF   |
| Input Capacitance ( $\overline{CS0} - \overline{CS3}$ )                                            | $C_{I2}$  | 32               | 40               | pF   |
| Input Capacitance (CLK0 - CLK3)                                                                    | $C_{ICL}$ | 38               | 40               | pF   |
| Input Capacitance (CKE0)                                                                           | $C_{I3}$  | 65               | 72               | pF   |
| Input Capacitance (DQMB0 - DQMB7)                                                                  | $C_{I4}$  | 13               | 16               | pF   |
| Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)                                                   | $C_{IO}$  | 10               | 10               | pF   |
| Input Capacitance (SCL, SA0-2)                                                                     | $C_{SC}$  | 8                | 8                | pF   |
| Input/Output Capacitance                                                                           | $C_{SD}$  | 8                | 8                | pF   |

**Operating Currents per SDRAM Component <sup>1)</sup>**
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 

| Parameter                                                                                                                                                                                                                             | Test Condition          | Symbol     | -7.5 | -8  | Unit | Note              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------------|------|-----|------|-------------------|
|                                                                                                                                                                                                                                       |                         |            | max. |     |      |                   |
| Operating current<br><br>$t_{RC} = t_{RCMIN.}$ , $t_{CK} = t_{CKMIN.}$<br>Outputs open, Burst Length = 4, CL = 3<br>All banks operated in random access,<br>all banks operated in ping-pong manner<br>to maximize gapless data access | –                       | $I_{CC1}$  | 230  | 170 | mA   | <sup>2)</sup>     |
| Precharge stand-by current<br>in Power Down Mode<br><br>$\overline{CS} = V_{IH(MIN.)}$ , $CKE \leq V_{IL(MAX.)}$                                                                                                                      | $t_{CK} = \text{min.}$  | $I_{CC2P}$ | 2    | 2   | mA   | <sup>2)</sup>     |
| Precharge Stand-by Current<br>in Non-Power Down Mode<br><br>$\overline{CS} = V_{IH(MIN.)}$ , $CKE \geq V_{IH(MIN.)}$                                                                                                                  | $t_{CK} = \text{min.}$  | $I_{CC2N}$ | 40   | 30  | mA   | <sup>2)</sup>     |
| No operating current<br><br>$t_{CK} = \text{min.}$ , $\overline{CS} = V_{IH(MIN.)}$ ,<br>active state (max. 4 banks)                                                                                                                  | $CKE \geq V_{IH(MIN.)}$ | $I_{CC3N}$ | 50   | 45  | mA   | <sup>2)</sup>     |
|                                                                                                                                                                                                                                       | $CKE \leq V_{IL(MAX.)}$ | $I_{CC3P}$ | 10   | 10  | mA   | <sup>2)</sup>     |
| Burst operating current<br>$t_{CK} = \text{min.}$ ,<br>Read command cycling                                                                                                                                                           | –                       | $I_{CC4}$  | 150  | 100 | mA   | <sup>2), 3)</sup> |
| Auto refresh current<br>$t_{CK} = \text{min.}$ ,<br>Auto Refresh command cycling                                                                                                                                                      | –                       | $I_{CC5}$  | 240  | 220 | mA   | <sup>2)</sup>     |
| Self refresh current<br>Self Refresh Mode, $CKE = 0.2 \text{ V}$                                                                                                                                                                      |                         | $I_{CC6}$  | 3    | 3   | mA   | <sup>2)</sup>     |

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 133 MHz operation frequency for -7 & -7.5 and at 100 MHz for -8 modules.  
Input signals are changed once during  $t_{CK}$ , excepts for  $I_{CC6}$  and for stand-by currents when  $t_{CK} = \text{infinity}$ .
3. These parameters are measured with continuous data stream during read access and all DQ toggling.  
CL = 3 and BL = 4 are assumed and the data-out current is excluded.

**AC Characteristics** <sup>1), 2)</sup>
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;  $V_{SS} = 0 \text{ V}$ ;  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $t_T = 1 \text{ ns}$ 

| Parameter | Symbol | Limit Values    |     |                   |      |                 |      | Unit | Notes |
|-----------|--------|-----------------|-----|-------------------|------|-----------------|------|------|-------|
|           |        | -7<br>PC133-222 |     | -7.5<br>PC133-333 |      | -8<br>PC100-222 |      |      |       |
|           |        | min.            | max | min.              | max. | min.            | max. |      |       |

**Clock**

|                                                                                                 |          |            |            |           |            |          |            |            |        |
|-------------------------------------------------------------------------------------------------|----------|------------|------------|-----------|------------|----------|------------|------------|--------|
| Clock Cycle Time<br>$\overline{\text{CAS}}$ Latency = 3<br>$\overline{\text{CAS}}$ Latency = 2  | $t_{CK}$ | 7.5<br>7.5 | —<br>—     | 7.5<br>10 | —<br>—     | 10<br>10 | —<br>—     | ns<br>ns   | —      |
| System Frequency<br>$\overline{\text{CAS}}$ Latency = 3<br>$\overline{\text{CAS}}$ Latency = 2  | $f_{CK}$ | —<br>—     | 133<br>133 | —<br>—    | 133<br>100 | —<br>—   | 100<br>100 | MHz<br>MHz | —      |
| Clock Access Time<br>$\overline{\text{CAS}}$ Latency = 3<br>$\overline{\text{CAS}}$ Latency = 2 | $t_{AC}$ | —<br>—     | 5.4<br>5.4 | —<br>—    | 5.4<br>6   | —<br>—   | 6<br>6     | ns<br>ns   | 3), 4) |
| Clock High Pulse Width                                                                          | $t_{CH}$ | 2.5        | —          | 2.5       | —          | 3        | —          | ns         | 4)     |
| Clock Low Pulse Width                                                                           | $t_{CL}$ | 2.5        | —          | 2.5       | —          | 3        | —          | ns         | 4)     |

**Setup and Hold Times**

|                                 |           |     |   |     |   |   |   |     |    |
|---------------------------------|-----------|-----|---|-----|---|---|---|-----|----|
| Input Setup Time                | $t_{CS}$  | 1.5 | — | 1.5 | — | 2 | — | ns  | 5) |
| Input Hold Time                 | $t_{CH}$  | 0.8 | — | 0.8 | — | 1 | — | ns  | 5) |
| Power Down Mode Entry Time      | $t_{SB}$  | —   | 1 | —   | 1 | — | 1 | CLK | 6) |
| Power Down Mode Exit Setup Time | $t_{PDE}$ | 1   | — | 1   | — | 1 | — | CLK | 7) |
| Mode Register Setup Time        | $t_{RSC}$ | 2   | — | 2   | — | 2 | — | CLK |    |
| Transition Time (rise and fall) | $t_T$     | 1   | — | 1   | — | 1 | — | ns  | —  |

**Common Parameters**

|                                                                           |           |    |   |      |      |    |      |     |   |
|---------------------------------------------------------------------------|-----------|----|---|------|------|----|------|-----|---|
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay                  | $t_{RCD}$ | 15 | — | 20   | —    | 20 | —    | ns  | — |
| Precharge Time                                                            | $t_{RP}$  | 15 | — | 20   | —    | 20 | —    | ns  | — |
| Active Command Period                                                     | $t_{RAS}$ | 42 | — | 45   | 100k | 50 | 100k | ns  | — |
| Cycle Time                                                                | $t_{RC}$  | 60 | — | 67.5 | —    | 70 | —    | ns  | — |
| Bank to Bank Delay Time                                                   | $t_{RRD}$ | 14 | — | 15   | —    | 16 | —    | ns  | — |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (same bank) | $t_{CCD}$ | 1  | — | 1    | —    | 1  | —    | CLK | — |

**AC Characteristics (cont'd)** <sup>1), 2)</sup>
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}; t_T = 1 \text{ ns}$ 

| Parameter | Symbol | Limit Values    |     |                   |      |                 |      | Unit | Note |
|-----------|--------|-----------------|-----|-------------------|------|-----------------|------|------|------|
|           |        | -7<br>PC133-222 |     | -7.5<br>PC133-333 |      | -8<br>PC100-222 |      |      |      |
|           |        | min.            | max | min.              | max. | min.            | max. |      |      |

**Refresh Cycle**

|                              |            |    |   |   |    |   |    |     |               |
|------------------------------|------------|----|---|---|----|---|----|-----|---------------|
| Refresh Period (8192 cycles) | $t_{REF}$  | 64 | — | — | 64 | — | 64 | ms  | <sup>6)</sup> |
| Self Refresh Exit Time       | $t_{SREX}$ | —  | 1 | 1 | —  | 1 | —  | CLK | <sup>8)</sup> |

**Read Cycle**

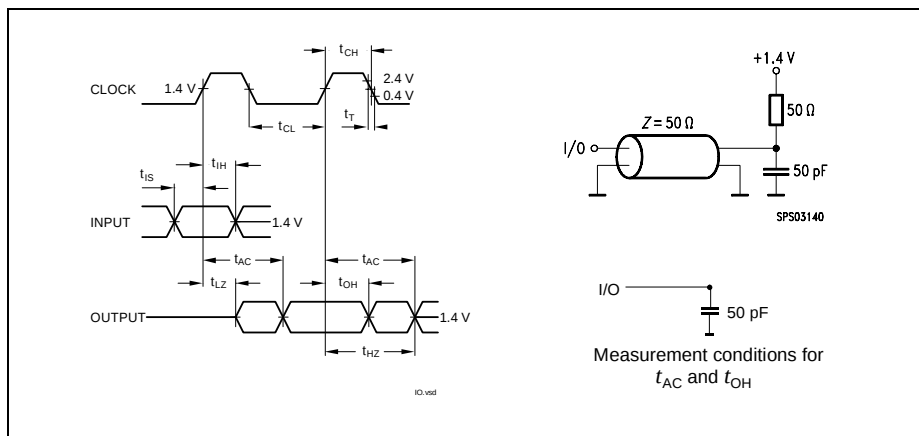
|                              |           |   |   |   |   |   |   |     |               |
|------------------------------|-----------|---|---|---|---|---|---|-----|---------------|
| Data Out Hold Time           | $t_{OH}$  | 3 | — | 3 | — | 3 | — | ns  | <sup>2)</sup> |
| Data Out to Low Impedance    | $t_{LZ}$  | 0 | — | 0 | — | 0 | — | ns  | —             |
| Data Out to High Impedance   | $t_{HZ}$  | 3 | 7 | 3 | 7 | 3 | 8 | ns  | <sup>9)</sup> |
| DQM Data Out Disable Latency | $t_{DQZ}$ | — | 2 | — | 2 | — | 2 | CLK | —             |

**Write Cycle**

|                                             |           |   |   |   |   |   |   |     |   |
|---------------------------------------------|-----------|---|---|---|---|---|---|-----|---|
| Data Input to Precharge<br>(write recovery) | $t_{WR}$  | 2 | — | 2 | — | 2 | — | CLK | — |
| DQM Write Mask Latency                      | $t_{DQW}$ | 0 | — | 0 | — | 0 | — | CLK | — |

### Notes

1. All AC characteristics are shown for the SDRAM components.  
An initial pause of 100  $\mu$ s is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have  $V_{IL} = 0.4$  V and  $V_{IH} = 2.4$  V with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{IH}$  and  $V_{IL}$ . All AC measurements assume  $t_T = 1$  ns with the AC output load circuit shown in Figure below. Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V/ns edge rate between 0.8 V and 2.0 V.
3. If clock rising time is longer than 1 ns, a time  $(t_T/2 - 0.5)$  ns must be added to this parameter.
4. Rated at 1.4 V.
5. If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)$  ns must be added to this parameter.
6. Whenever the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
7. Timing is asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
8. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied after the Self Refresh Exit command is registered.
9. This is referenced to the time at which the output achieved the open circuit condition, not to output voltage levels.



### Serial Presence Detect

A serial presence detect storage device - E<sup>2</sup>PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E<sup>2</sup>PROM device during module production using a serial presence detect protocol (I<sup>2</sup>C synchronous 2-wire bus).

**SPD-Table for 32M x 64 (256MByte non-ECC) Modules HYS64V32300GU**

| Byte# | Description                                                | SPD Entry Value              | Hex      |      |    |
|-------|------------------------------------------------------------|------------------------------|----------|------|----|
|       |                                                            |                              | 32M x 64 |      |    |
|       |                                                            |                              | -7       | -7.5 | -8 |
| 0     | Number of SPD Bytes                                        | 128                          | 80       |      |    |
| 1     | Total Bytes in Serial PD                                   | 256                          | 08       |      |    |
| 2     | Memory Type                                                | SDRAM                        | 04       |      |    |
| 3     | Number of Row Addresses                                    | 13                           | 0D       |      |    |
| 4     | Number of Column Addresses                                 | 10                           | 0A       |      |    |
| 5     | Number of DIMM Banks                                       | 1                            | 01       |      |    |
| 6     | Module Data Width                                          | 64                           | 40       |      |    |
| 7     | Module Data Width (cont'd)                                 | 0                            | 00       |      |    |
| 8     | Module Interface Levels                                    | LVTTTL                       | 01       |      |    |
| 9     | SDRAM Cycle Time at CL = 3                                 | 7.5 / 10 ns                  | 75       | 75   | A0 |
| 10    | SDRAM Access Time at CL = 3                                | 5.4 / 6 ns                   | 54       | 54   | 60 |
| 11    | DIMM Config                                                | non-ECC                      | 00       |      |    |
| 12    | Refresh Rate/Type                                          | Self-Refresh,<br>7.8 $\mu$ s | 82       |      |    |
| 13    | SDRAM Width, Primary                                       | x8                           | 08       |      |    |
| 14    | Error Checking SDRAM Data Width                            | na                           | 00       |      |    |
| 15    | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD} = 1$ CLK            | 01       |      |    |
| 16    | Burst Length Supported                                     | 1, 2, 4 & 8                  | 0F       |      |    |
| 17    | Number of SDRAM Banks                                      | 4                            | 04       |      |    |
| 18    | Supported CAS Latencies                                    | CL = 2 & 3                   | 06       |      |    |
| 19    | CS Latencies                                               | CS latency = 0               | 01       |      |    |
| 20    | WE Latencies                                               | Write latency = 0            | 01       |      |    |
| 21    | SDRAM DIMM Module Attributes                               | unbuffered                   | 00       |      |    |
| 22    | SDRAM Device Attributes: General                           | $V_{DD}$ tol +/- 10%         | 0E       |      |    |
| 23    | SDRAM Cycle Time at CL = 2                                 | 7.5 / 10.0 ns                | 75       | A0   | A0 |
| 24    | SDRAM Access Time at CL = 2                                | 5.4 / 6.0 ns                 | 54       | 60   | 60 |
| 25    | SDRAM Cycle Time at CL = 1                                 | not supported                | 00       | FF   | FF |
| 26    | SDRAM Access Time at CL = 1                                | not supported                | 00       | FF   | FF |
| 27    | Minimum Row Precharge Time                                 | 15 / 20 ns                   | 0F       | 14   | 14 |
| 28    | Min. Row to Row Active Delay $t_{RRD}$                     | 14 / 15 / 16 ns              | 0E       | 0F   | 10 |
| 29    | Minimum RAS to CAS Delay $t_{RCD}$                         | 15 / 20 ns                   | 0F       | 14   | 14 |
| 30    | Minimum RAS Pulse Width $t_{RAS}$                          | 42 / 45 / 50 ns              | 2A       | 2D   | 32 |
| 31    | Module Bank Density (per bank)                             | 256 MByte                    | 40       |      |    |
| 32    | SDRAM Input Setup Time                                     | 1.5 / 2.0 ns                 | 15       | 15   | 20 |
| 33    | SDRAM Input Hold Time                                      | 0.8 / 1.0 ns                 | 08       | 08   | 10 |
| 34    | SDRAM Data Input Hold Time                                 | 1.5 / 2.0 ns                 | 15       | 15   | 20 |
| 35    | SDRAM Data Input Setup Time                                | 0.8 / 1.0 ns                 | 08       | 08   | 10 |

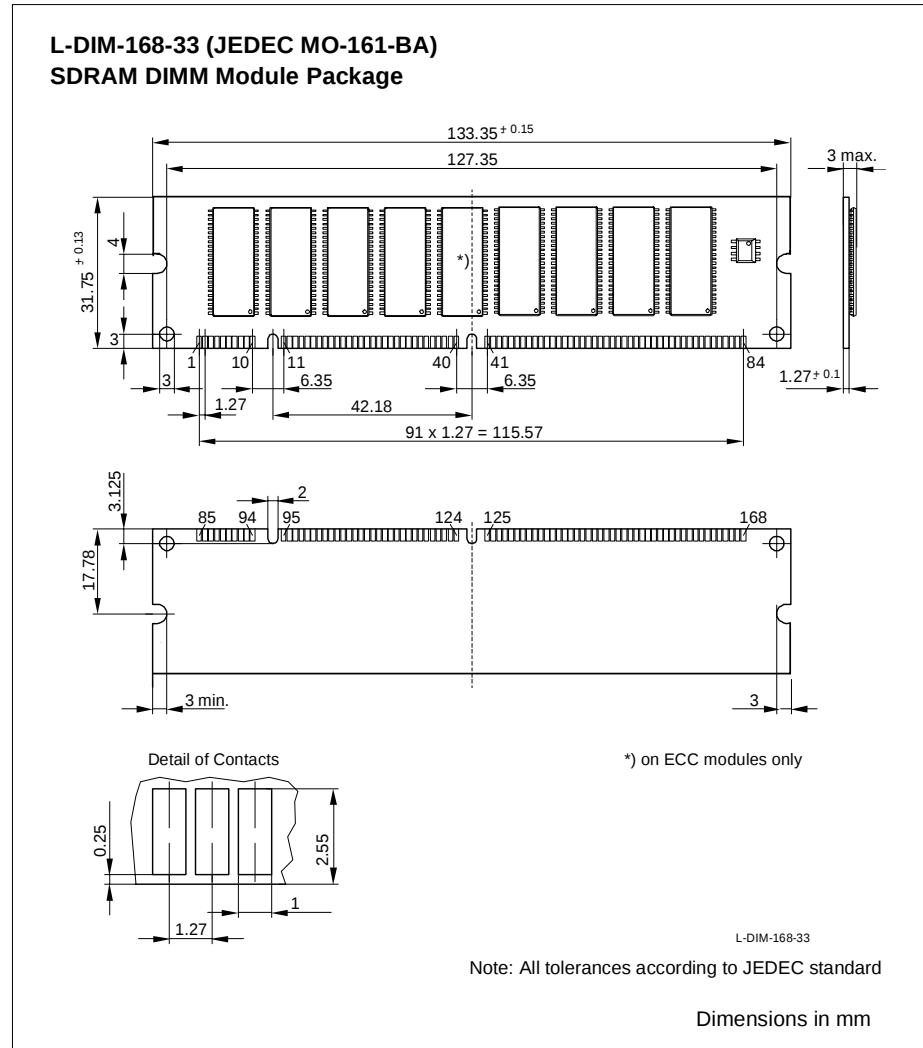
| Byte#  | Description                 | SPD Entry Value | Hex        |      |    |
|--------|-----------------------------|-----------------|------------|------|----|
|        |                             |                 | 32M x 64   |      |    |
|        |                             |                 | -7         | -7.5 | -8 |
| 36-61  | Superset Information        | –               | FF         | FF   | FF |
| 62     | SPD Revision                | Revision 1.2    | 12         | 12   | 12 |
| 63     | Checksum for Bytes 0 - 62   | –               | F3         | 36   | 99 |
| 64     | Manufacturers JEDEC ID Code | –               | C1         |      |    |
| 65-71  | Manufacturer                |                 | INFINEO(N) |      |    |
| 72     | Module Assembly Location    |                 |            |      |    |
| 73-90  | Module Part Number          |                 |            |      |    |
| 91-92  | Module Revision Code        |                 |            |      |    |
| 93-94  | Module Manufacturing Code   |                 |            |      |    |
| 95-98  | Module Serial Number        |                 |            |      |    |
| 99-125 | Superset Information        |                 |            |      |    |
| 126    | Frequency Specification     |                 | 64         | 64   | 64 |
| 127    | 100 MHz Support Details     | –               | AF         | AF   | AF |
| 128+   | Unused Storage Locations    | –               | FF         |      |    |

**SPD-Table for 32M x 72 (256MByte ECC) Modules HYS72V32300GU**

| Byte# | Description                                                | SPD Entry Value              | Hex      |      |    |
|-------|------------------------------------------------------------|------------------------------|----------|------|----|
|       |                                                            |                              | 32M x 72 |      |    |
|       |                                                            |                              | -7       | -7.5 | -8 |
| 0     | Number of SPD Bytes                                        | 128                          | 80       |      |    |
| 1     | Total Bytes in Serial PD                                   | 256                          | 08       |      |    |
| 2     | Memory Type                                                | SDRAM                        | 04       |      |    |
| 3     | Number of Row Addresses                                    | 13                           | 0D       |      |    |
| 4     | Number of Column Addresses                                 | 10                           | 0A       |      |    |
| 5     | Number of DIMM Banks                                       | 1                            | 01       |      |    |
| 6     | Module Data Width                                          | 72                           | 48       |      |    |
| 7     | Module Data Width (cont'd)                                 | 0                            | 00       |      |    |
| 8     | Module Interface Levels                                    | LVTTTL                       | 01       |      |    |
| 9     | SDRAM Cycle Time at CL = 3                                 | 7.5 / 10 ns                  | 75       | 75   | A0 |
| 10    | SDRAM Access Time at CL = 3                                | 5.4 / 6 ns                   | 54       | 54   | 60 |
| 11    | DIMM Config                                                | ECC                          | 02       |      |    |
| 12    | Refresh Rate/Type                                          | Self-Refresh,<br>7.8 $\mu$ s | 82       |      |    |
| 13    | SDRAM Width, Primary                                       | x8                           | 08       |      |    |
| 14    | Error Checking SDRAM Data Width                            | x8                           | 08       |      |    |
| 15    | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD} = 1$ CLK            | 01       |      |    |
| 16    | Burst Length Supported                                     | 1, 2, 4 & 8                  | 0F       |      |    |
| 17    | Number of SDRAM Banks                                      | 4                            | 04       |      |    |
| 18    | Supported CAS Latencies                                    | CL = 2 & 3                   | 06       |      |    |
| 19    | CS Latencies                                               | CS latency = 0               | 01       |      |    |
| 20    | WE Latencies                                               | Write latency = 0            | 01       |      |    |
| 21    | SDRAM DIMM Module Attributes                               | unbuffered                   | 00       |      |    |
| 22    | SDRAM Device Attributes: General                           | $V_{DD}$ tol +/- 10%         | 0E       |      |    |
| 23    | SDRAM Cycle Time at CL = 2                                 | 7.5 / 10.0 ns                | 75       | A0   | A0 |
| 24    | SDRAM Access Time at CL = 2                                | 5.4 / 6.0 ns                 | 54       | 60   | 60 |
| 25    | SDRAM Cycle Time at CL = 1                                 | not supported                | 00       | FF   | FF |
| 26    | SDRAM Access Time at CL = 1                                | not supported                | 00       | FF   | FF |
| 27    | Minimum Row Precharge Time                                 | 15 / 20 ns                   | 0F       | 14   | 14 |
| 28    | Min. Row to Row Active Delay $t_{RRD}$                     | 14 / 15 / 16 ns              | 0E       | 0F   | 10 |
| 29    | Minimum RAS to CAS Delay $t_{RCD}$                         | 15 / 20 ns                   | 0F       | 14   | 14 |
| 30    | Minimum RAS Pulse Width $t_{RAS}$                          | 42 / 45 / 50 ns              | 2A       | 2D   | 32 |
| 31    | Module Bank Density (per bank)                             | 256 MByte                    | 40       |      |    |
| 32    | SDRAM Input Setup Time                                     | 1.5 / 2.0 ns                 | 15       | 15   | 20 |
| 33    | SDRAM Input Hold Time                                      | 0.8 / 1.0 ns                 | 08       | 08   | 10 |
| 34    | SDRAM Data Input Hold Time                                 | 1.5 / 2.0 ns                 | 15       | 15   | 20 |
| 35    | SDRAM Data Input Setup Time                                | 0.8 / 1.0 ns                 | 08       | 08   | 10 |

| Byte#  | Description                 | SPD Entry Value | Hex        |      |    |
|--------|-----------------------------|-----------------|------------|------|----|
|        |                             |                 | 32M x 72   |      |    |
|        |                             |                 | -7         | -7.5 | -8 |
| 36-61  | Superset Information        | –               | FF         | FF   | FF |
| 62     | SPD Revision                | Revision 1.2    | 12         | 12   | 12 |
| 63     | Checksum for Bytes 0 - 62   | –               | 05         | 48   | AB |
| 64     | Manufacturers JEDEC ID Code | –               | C1         |      |    |
| 65-71  | Manufacturer                |                 | INFINEO(N) |      |    |
| 72     | Module Assembly Location    |                 |            |      |    |
| 73-90  | Module Part Number          |                 |            |      |    |
| 91-92  | Module Revision Code        |                 |            |      |    |
| 93-94  | Module Manufacturing Code   |                 |            |      |    |
| 95-98  | Module Serial Number        |                 |            |      |    |
| 99-125 | Superset Information        |                 |            |      |    |
| 126    | Frequency Specification     |                 | 64         | 64   | 64 |
| 127    | 100 MHz Support Details     | –               | AF         | AF   | AF |
| 128+   | Unused Storage Locations    | –               | FF         |      |    |

**Package Outlines**





## **HYS 64/72V32300GU SDRAM-Modules**

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**Change List:**

|            |                                                                                                                                                                                                                                                                                                      |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14.1.1999  | Input capacitances adjusted                                                                                                                                                                                                                                                                          |
| 18.4.1999  | -8A speed sort added<br>Infineon logo added<br>SPD codes updated according to new 256M speedsorts                                                                                                                                                                                                    |
| 12.5.99    | Some ICC current values changed due to new inputs                                                                                                                                                                                                                                                    |
| 21.7.99    | HYS64/72V32200GU changed to HYS64/72V32300GU due to the use of L-DIM168-33 instead of L-DIM168-30                                                                                                                                                                                                    |
| 23.8.99    | Byte 126 changed to 64h for PC133 modules                                                                                                                                                                                                                                                            |
| 6.9.99     | Template from R&L                                                                                                                                                                                                                                                                                    |
| 29.9.99    | Some minor errors corrected                                                                                                                                                                                                                                                                          |
| 20.10.99   | CL=2 max. frequency for -7.5 modules changes to 83 MHz                                                                                                                                                                                                                                               |
| 2.12.99    | Some timing parameters according to INTEL'S PC133 specification                                                                                                                                                                                                                                      |
| 20.1.2000  | Capacitance values for x72 adjusted (new measurements)<br>-8B version removed                                                                                                                                                                                                                        |
| 10.3.2000  | Implemented differences between 256Mbit S20 and S17 PC133 modules<br>256Mbit S20 based PC133 modules are backward compatible to PC100 3-2-2<br>256Mbit S17 based modules are backwards compatible to PC100-2-2-2<br>leading to changes in SPD code of bytes 23, 63 (checksum) and 126<br>TPCR issued |
| 10.5.2000  | Reference to JEDEC MO-161-BA added                                                                                                                                                                                                                                                                   |
| 14.02.2001 | -8A speedsort removed<br>for 256M S17 and later only                                                                                                                                                                                                                                                 |
| 25.07.2001 | 256M S14 based modules including -7 added                                                                                                                                                                                                                                                            |
| 06.09.2001 | SCR : Absolute Maximum Ratings table added                                                                                                                                                                                                                                                           |