LINEAR TECHNOLOGY

DESIGN NOTES

Multiple Power Supplies Track During Power Up

Design Note 272

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Many modern circuits require multiple power supplies that must turn on in a certain order to avoid damaging sensitive components. In many cases, forcing the supplies to ramp up together is the preferred solution. Unfortunately, this can be difficult when the supplies are generated from multiple sources, each with its own power-up timing and transient response. However, there is a simple solution for up to five supplies ramping up simultaneously.

The circuit shown in Figure 1 solves this problem by placing an N-channel MOSFET between the output of each power supply and the load. When power is first applied to the circuit, the MOSFETs are turned off and each power supply is allowed to power up at its own rate. Once each power supply has settled, the common gates of the MOSFETs are ramped up, forcing the outputs to ramp up simultaneously as shown in Figure 2.

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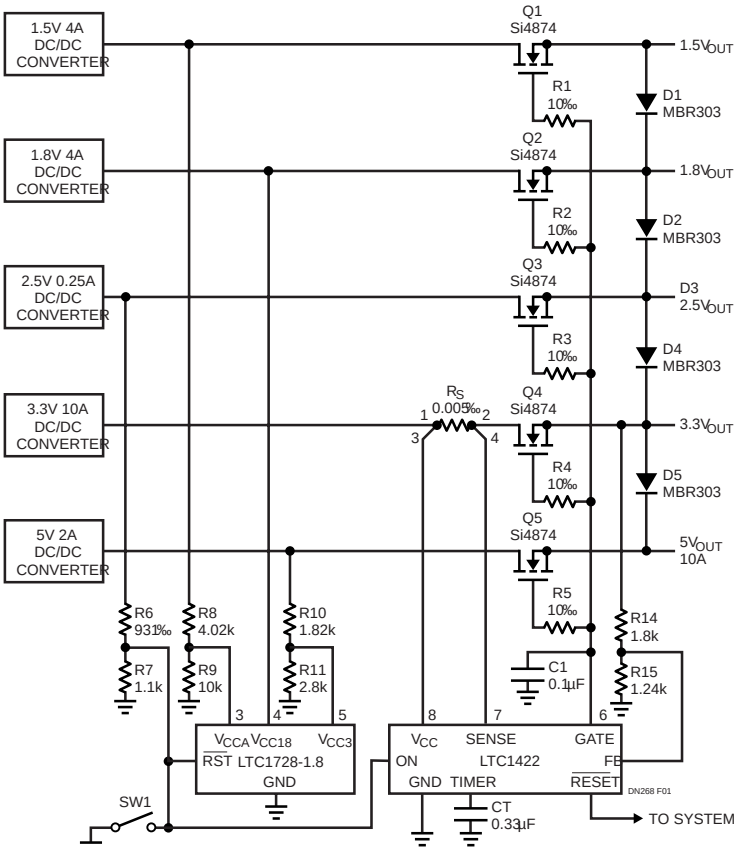
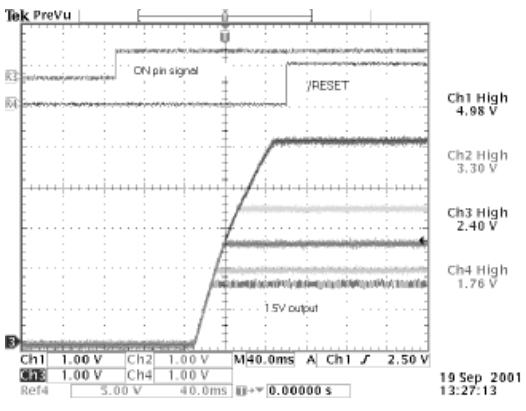
The key components of the circuit in Figure 1 are the LTC1728-1.8 triple supply monitor and the LTC1422 single Hot Swap™ controller. The LTC1728-1.8 directly monitors three supply outputs: 5V, 1.8V and 1.5V. The outputs of the 3.3V and 2.5V supplies are monitored by





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the LTC1422. Short-circuit protection for the 3.3V supply is provided by the LTC1422 using sense resistor R_S, but all other voltages rely on their individual power supplies' current limit.

When all three supplies monitored by the LTC1728-1.8 are in compliance, the open-drain pull-down on the $\overline{RST}$ pin turns off after a 200ms delay. The 2.5V resistor divider monitor connected to the LTC1422 ON pin is then enabled. When the 2.5V supply is within tolerance as measured by the ON pin, and the 3.3V supply exceeds the LTC1422 undervoltage lockout threshold, the LTC1422 turns on.

After one timing cycle (set by C2 at the TIMER pin), the voltage at the GATE pin begins to ramp up, turning on transistors Q1 to Q5. The slope of the voltage rise is set by the total capacitance at the GATE pin (C_G) and 0.1µA GATE pull-up current:

$$\frac{dV_{GATE}}{dt} = \frac{I_{GATE}}{C_G}$$

Capacitance C_G is equal to the sum of capacitor C1 and the total MOSFET gate capacitance. Because each MOSFET is connected as a source follower, the inrush current into each load capacitance is limited according to:

$$I_{INRUSH} = \frac{C_{LOAD} \bullet I_{GATE}}{C_G}$$

Once the 3.3V output is within tolerance as measured by the FB pin, the $\overline{RESET}$ pin open-drain pull-down turns off after a timing cycle. A complete timing diagram is shown in Figure 3.

Power down can be initiated by forcing the ON pin signal low with the switch SW1, or by turning off any of the power supplies. The GATE pin is pulled low immediately, disconnecting the loads from the power supplies, and the loads start to discharge at the rate determined by the load capacitance and load current. Diodes D1 to D5 are included to ensure worst-case differential levels between supplies during power-down and catastrophic fault conditions.

For better performance, use low drop power MOSFETs and adjust the preliminary power supply voltage to account for the voltage drop across the transistor.

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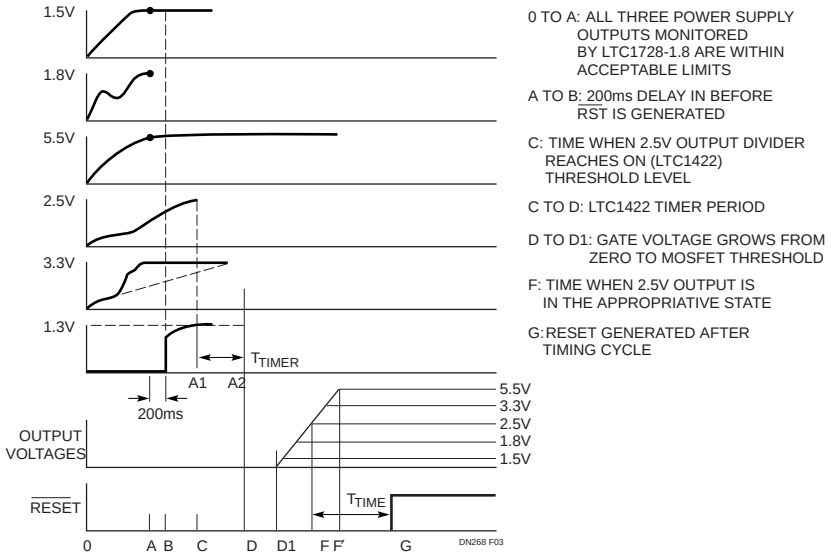
Although the circuit of Figure 1 controls five supplies, it can be easily modified to accommodate fewer supplies. Unused monitor inputs can be tied off to a higher supply voltage and the unused MOSFETs removed. Different supply voltages can be accommodated by selecting the appropriate voltage option of the LTC1728-1.8 and changing resistor values. In sum, with only a handful of components, the circuit solves the tricky problem of controlling the power up of multiple supplies in a complex system.



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http://www.linear.com/go/dnLTC1422

For literature on our Hot Swap Controllers, call ✍✘✎✎✍✔✍✶ For applications help, call (408) 432-1900, Ext. 2453

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