Solve Isolated Control Problems by Up-Shifting Control Frequency with TimerBlox PWM Generator

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Industrial and medical systems often have functions that are completely isolated from the mains power—requiring control signals that must cross the isolation barrier, usually via a small transformer. One cost-effective source of control signals is the I/O pin of embedded controllers. The oscillators and counters already included in controllers can be used to produce digitally programmable PWM signals, which can provide a variable duty cycle square wave, or, if averaged by a simple RC lowpass filter, a linearly variable analog voltage.

For example, if the I/O pin output of an embedded controller produces a varying duty cycle PWM signal that switches between V_{CC} and ground, the average output voltage of the I/O pin is simply V_{CC} • (duty cycle).

The problem with using the PWM output of an embedded controller to produce control signals in an isolated system is that the frequency of these signals is often too low for a small signal transformer to handle.

Figure 1 shows a simple strategy that allows low frequency PWM signals to be properly passed via small signal

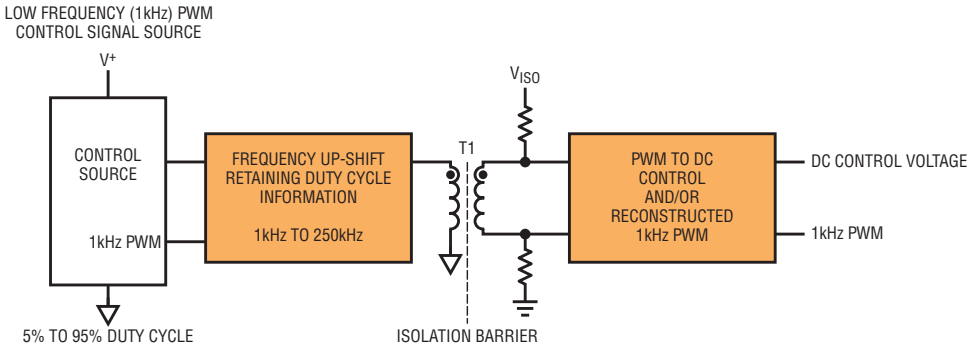

Figure 1. Transferring control information across a small signal isolation transformer requires a higher frequency PWM signal than that produced by most embedded controllers. On the isolated side, the resulting signal can be either converted to a DC control voltage or converted to a replicate of the original PWM signal.

transformers across an isolation barrier. In this solution, the low frequency PWM signal is converted to a higher frequency while retaining the duty cycle control information. Specifically, a 1kHz PWM signal is shifted to 250kHz, coupled across the isolation barrier, then shifted back down to the original 1kHz (or simply converted to a DC voltage control signal). Changes in the source PWM signal duty cycle are duplicated nearly instantly on the isolated side. Accuracy of the isolated control signal is within 1% of the source duty cycle.

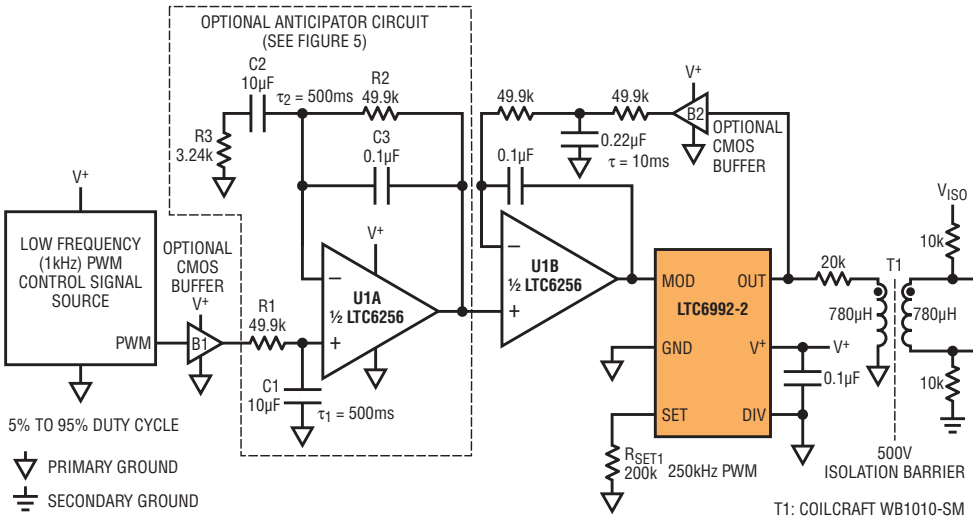

Figure 2. Nonisolated control side. A TimerBlox® PWM circuit generates a 250kHz signal with the same duty cycle as the original low frequency PWM signal. The optional anticipator circuit improves step response by anticipating step changes in the duty cycle of the control PWM (see "Circuit Enhancements" below).

The problem with using the PWM output of an embedded controller to produce control signals in an isolated system is that the frequency of these signals is often too low for a small signal transformer to handle. Here is a simple strategy that allows low frequency PWM signals to be properly passed via small signal transformers across an isolation barrier.

UP-SHIFTING THE PWM CONTROL FREQUENCY

Figure 2 shows a circuit that converts a 1kHz PWM signal to a 250kHz signal with the exact same duty cycle. This 250kHz signal can easily couple across an isolation transformer.

The LTC6992-2 is a voltage-controlled PWM generator. A voltage ranging from 0V to 1V on the MOD input pin linearly varies the duty cycle of the output clock from 5% to 95%. This device is chosen because it keeps its output clocking at all times. The duty cycle never reaches 0% or 100% duty cycle, since a DC signal would not pass through the transformer. The output frequency can range up to 1MHz and is easily programmed using resistors. Resistor R_{SET} fixes an internal master oscillator frequency and the voltage on the DIV pin sets an internal frequency divider ratio.

Amplifier U1B (one half of an LTC6256 low power dual rail-to-rail op amp) is an integrator used to servo the voltage at the MOD pin to force the 250kHz signal duty cycle to match the 1kHz input signal duty cycle. Simple RC lowpass filters convert both PWM clocks to their average DC voltages. To minimize duty cycle jitter, the time constants of these filters should be much longer than the clock period. The 1kHz PWM signal is filtered with a 500ms time constant network while the 250kHz filter is 10ms. The integrator output voltage stops at the MOD pin voltage required to force the average voltages, and therefore the duty cycles, of the two PWM signals to be exactly the same.

For accurate duty cycle control, the amplitudes of the two square waves must be the same so the power supply voltage for the LTC6992-2 is the same supply used for the controller generating the input PWM signal. The LTC6992-2 has 20mA of output current drive and can directly drive the primary winding of the isolation transformer.

The 500ms time constant network on the control source PWM signal makes duty cycle changes occur at a slow rate. Amplifier U1A is an optional circuit function that can speed up the response time of the circuit to duty cycle changes by a factor of 10. This function is described in the section "Circuit Enhancements," below.

CONTROL SIGNALS ON THE ISOLATED SIDE

On the isolated side of the transformer is an LT1719 comparator. This comparator converts the signal across the secondary of the transformer to a 250kHz square wave. This square wave can be filtered and simply buffered with an op amp to provide an isolated DC control voltage that moves proportionally to the duty cycle of the original PWM signal.

If a reconstructed replica of the 1kHz input PWM signal is required on the isolated side, simply add another LTC6992-2 PWM circuit, which is resistor programmed to output a 1kHz PWM signal. An integrator can be used here, in the same fashion as on the nonisolated side, to servo the output duty cycle to match that of

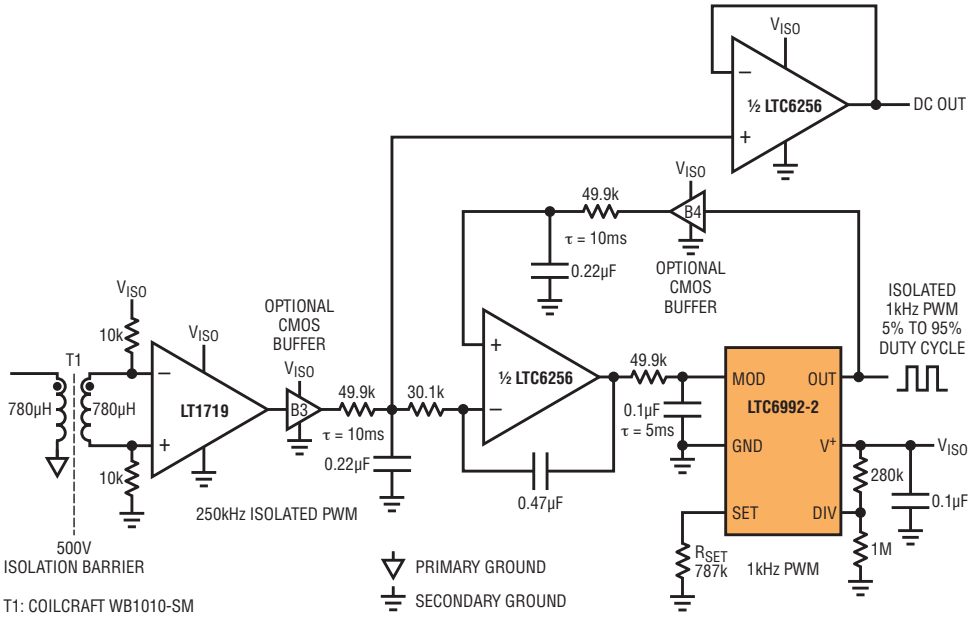

Figure 3. Isolated side. Simply buffering the filtered average of the 250kHz PWM signal on the isolated side provides a DC control signal. A second TimerBlox circuit can be used to reconstruct the original 1kHz PWM signal with the same duty cycle as the control source signal.

A possible drawback to this circuit is the long time constant and resulting slow response time to any changes in the duty cycle of the 1kHz control source PWM signal. The amplifier circuit shown in Figure 5 allows the 250kHz PWM signal to respond nearly instantly to any changes in the 1kHz control PWM despite the slow filter response time.

the 250kHz comparator output square wave. Once again the average voltages, and therefore the duty cycles, of the two square waves are forced to be the same.

CIRCUIT ENHANCEMENTS

Improving Duty Cycle Accuracy

One important requirement for an accurate match of the two duty cycles is that the amplitude of the PWM signals are exactly the same. Lightly loaded CMOS outputs swing virtually all the way between ground and the supply rail.

For more precise matching of the amplitudes of the two PWM signals, some inexpensive CMOS logic buffers, B1 and B2 in Figure 2 and B3 and B4 in Figure 3 on the isolated side, can be used on each square wave signal to force the amplitudes to be identical. Two like buffers powered from the same supply with the same current loading will produce matched output levels. Any supply voltage variation moves each of the two compared signals the same amount for a good measure of supply variation insensitivity.

Figure 4 shows the duty cycle difference between the source-side PWM and the replicate isolated-side PWM—results are shown with and without the amplitude-matching logic buffers.

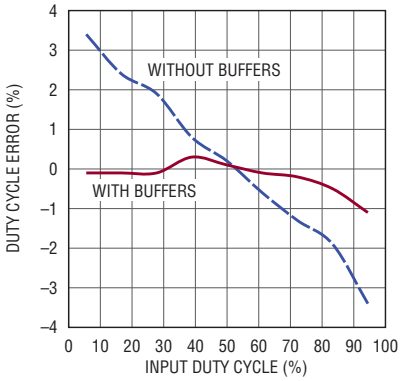

Figure 4. Using simple CMOS buffers to match the amplitudes of all PWM signals can reduce duty cycle error to less than 1%.

Anticipator Amplifier Predicts and Speeds Response to the Final Value

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Circuit operation relies on knowing the exact time constant of the exponentially responding input signal, τ_1, which is set at 500ms by R1 and C1. Any step change in duty cycle of the PWM input signal creates a voltage at the plus input of the amplifier that changes from an initial voltage, V_i, to a final voltage, V_f, in an exponential fashion per the familiar equation:

$$V_{IN} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1}$$

The time domain step response at the output of this circuit can be found by the following series of equations:

$$V_{OUT} = V_{IN} + R2 \bullet I_{C2}(t)$$

$$I_{C2}(t) = C2 \bullet \frac{dV_{IN}}{dt}$$

Recall from the math that:

$$\frac{dae^x}{dt} = ae^x \bullet \frac{dx}{dt}$$

so

$$\frac{dV_{IN}}{dt} = -(V_f - V_i) \bullet e^{-t/\tau_1} \bullet \frac{-1}{\tau_1}$$

$$= \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

continued on page 43

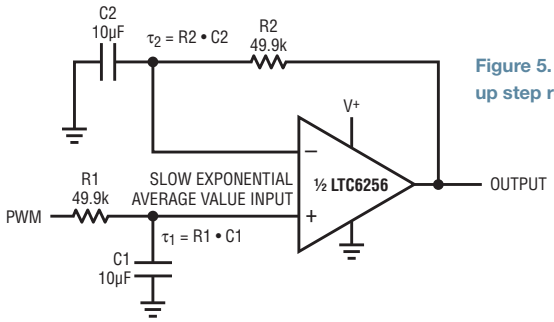

Figure 5. Anticipator amplifier circuit speeds up step response by a factor of 10.

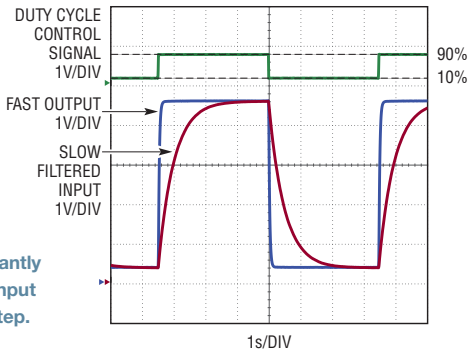

Figure 6. The anticipator output moves nearly instantly to the final value of a slow changing exponential input signal. Input change is a 10% to 90% duty cycle step.

Product Briefs

OP AMP DRIVES SAR ADCs TO TRUE ZERO ON A SINGLE 5V SUPPLY

The LTC6360 is a very low noise, high speed amplifier that can drive to 0V while maintaining high linearity on a single 5V supply. The LTC6360's integrated ultralow noise charge pump provides an internal negative rail, eliminating the need for a negative supply. Compared to typical rail-to-rail output single-supply amplifiers that can only swing to within a few hundred millivolts of ground, the LTC6360 provides improved linearity and dynamic range in applications that benefit from a true zero output swing.

The LTC6360 achieves outstanding precision and is ideal for driving 16- and 18-bit SAR ADCs (successive approximation register analog-to-digital converters). Input offset voltage is less than 250µV max, and noise is only 2.3nV/√Hz, providing excellent dynamic range. The device settles to 16-bits in 150ns, and achieves a closed loop –3dB bandwidth of 250MHz. Harmonic distortion (HD2/HD3) is –103dBc/–109dBc at f_{IN} = 40kHz. The LTC6360 is unity gain stable, allowing it to be used as a buffer to achieve the lowest output noise. The output is designed to drive a series 10Ω resistor and 330pF capacitor filter network, although larger load capacitances can be driven.

The LTC6360 is available in a compact 3mm × 3mm, 8-pin leadless DFN package and an 8-pin MSOP package with exposed pad and operates over a –40°C to 125°C temperature range.

ULTRALOW NOISE AND SPURIOUS 0.37GHZ TO 5.7GHZ INTEGER-N SYNTHESIZER WITH INTEGRATED VCO

The LTC6946 is a high performance, low noise, 5.7GHz phase-locked loop (PLL) with a fully integrated VCO, including a reference divider, phase-frequency detector (PFD) with phase-lock indicator, ultralow noise charge pump, integer feedback divider, and VCO output divider. The charge pump contains selectable high and low voltage clamps useful for VCO monitoring. The integrated low noise VCO uses no external components. It is internally calibrated to the correct output frequency with no external system support. The part features a buffered, programmable VCO output divider with a range of 1 through 6, providing a wide frequency range. ■

(TimerBlox, continued from page 42)

$$I_{C2}(t) = C2 \bullet \frac{dV_{IN}}{dt} = \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

$$V_{OUT} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1} + R2 \bullet C2 \bullet \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

If τ_2 (R2C2) is exactly equal to τ_1 (R1C1) then:

$$V_{OUT} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1} + (V_f - V_i) \bullet e^{-t/\tau_1}$$

$$V_{OUT} = V_f$$

When the input starts to change at an exponential rate, the circuit extrapolates the final value and jumps there instantly. This look-ahead response drives the duty cycle servo integrator in Figure 2 to quickly change the 250kHz PWM generator to its final value without waiting for the 500ms time constant filter to get there.

The closed loop gain of this stage increases directly with frequency and is inherently unstable. Frequency response shaping is accomplished in Figure 2 via R3 and C3. The low frequency step response is still dominated by R2 and C2.

Figure 6 shows the quick response to a step change in control signal duty cycle from 10% to 90%. The anticipated output arrives at the final voltage in about 200ms, ten times faster than the two to three seconds for the input signal to fully settle.

CONCLUSION

Generating control signals across an isolation barrier from a low frequency PWM control source can be implemented by up-shifting the PWM frequency. The LTC6992-2 PWM TimerBlox function easily handles frequency scaling with simple resistor programmability. Op amp integrators ensure that the duty cycle control information is accurately reproduced on the isolated side. ■