2-Channel and 4-Channel Pin-Selectable I²C Multiplexer Features High Noise Margin, Capacitance Buffering, Level Translation and Stuck Bus Recovery

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The inherent simplicity of I²C and SMBus 2-wire protocols has made them a popular choice for communicating vital information in large systems. Both standards employ simple open-drain pull-down drivers with resistive or current source pull-ups. Nevertheless, several practical problems arise as systems grow in complexity.

The first problem with large systems is that devices with hard-wired I²C addresses require address expansion to prevent conflicts. Second, noise causes glitches that can be interpreted as legitimate clock or data transitions, compromising data reliability. Third, I²C devices can cause the bus to stick low. Finally, timing specifications are increasingly difficult to meet, and clock frequencies are limited by the equivalent bus capacitance, which increases with system size and complexity. The LTC4312 and LTC4314 pin-selectable 2-channel and 4-channel I²C multiplexers with bus buffers address these issues with a number of powerful features (see Table 1). Since these two devices share the same features, except for the number of channels, this article focuses on the LTC4314.

An upstream I²C bus (SDAIN, SCLIN) can be connected to any combination of downstream buses through the LTC4314's bus buffers and multiplexer switches by driving the ENABLE pins of the desired output buses high. Multiple devices having the same address can be placed on different buses and isolated using the ENABLE pins, thereby achieving address expansion.

The buffers provide capacitance isolation between the upstream bus and the downstream buses, allowing for partitioning of the bus capacitance. In single supply systems, the buffers regulate the bus up to 0.33 • V_{CC}, providing a large logic low noise margin. Rise time accelerators (RTAs) of appropriate strength can be activated to overcome bus capacitance limitations, reduce rise time and allow for higher switching frequencies even when operating with heavy loads.

The LTC4314 is compatible with the I²C standard and Fast Mode, SMBus and PMBus specifications. Stuck bus recovery circuitry disconnects the upstream bus from downstream buses when SDA and SCL have not been simultaneously high at least once in 45ms, freeing the upstream bus to resume communications. The recovery circuitry also attempts to convince

Table 1. Key features of the LTC4312 and LTC4314

FEATURE	BENEFITS
2- and 4-Pin Selectable Downstream Buses	• Maximum flexibility of bus configurations • Address expansion when used as a MUX
I²C Buffers	• Breaks up bus capacitance, which allows large I²C compliant systems to be built, by keeping the capacitance of each section < 400pF
Selectable V_{IL}	• High logic low noise margin up to 0.33 • V_{CC} • Selectable RTA Operating voltage range
Level Translation	• Provides I²C communication between 1.5V, 1.8V, 2.5V, 3.3V and 5V buses
Rise Time Accelerators (RTAs)	• Reduce rise time • Allow larger bus pull-up resistors for better noise margin • Selectable RTA pull-up current strength
Disconnection and Recovery from Stuck Bus	• Free masters to resume upstream communications • Generates up to to 16 clock pulses and a stop bit on the stuck buses to convince the stuck device to release high

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the stuck device to release high by generating up to 16 clock pulses and a stop bit on the enabled downstream buses.

Finally, cards can be hot-swapped into and out of the LTC4314's I²C output buses provided that the channel being hot-swapped has been disabled. The LTC4314's operating voltage range is V_{CC} from 2.9V to 5.5V, V_{CC2} from 2.25V to 5.5V and bus voltages from 2.25V to 5.5V. The LTC4314 can level translate down to 1.5V and 1.8V buses under certain conditions if RTAs are disabled on the low voltage bus.

HIGH BANDWIDTH BUFFERS IMPROVE NOISE MARGIN AND SPEED WHILE MAINTAINING LOW OFFSET

High noise margin is obtained by leaving the LTC4314 buffers on until both the input and output bus voltages are > 0.33 • V_{MIN}, where V_{MIN} is the lower of the V_{CC} and V_{CC2} voltages. This is possible because the high bandwidth buffers do not limit the rise rate of the bus, permitting them to stay on to a higher bus voltage.

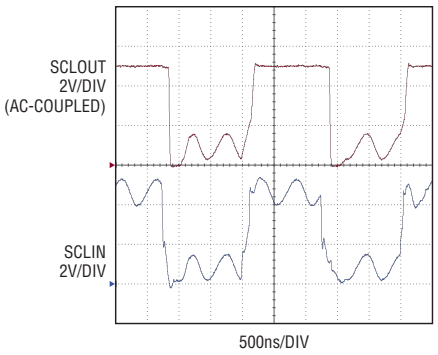

Figure 1. The LTC4314 transmitting a noisy 400kHz I²C signal applied to SCLIN. The SCLOUT1 waveform tracks SCLIN when SCLIN is a logic low. During logic highs, noise on SCLIN above 0.33 • V_{MIN} is not propagated to SCLOUT.

As seen in Figure 1, when a noisy 400kHz square wave signal is applied to SCLIN, the SCLOUT1 waveform tracks SCLIN when the SCLIN voltage is < 0.33 • V_{MIN}, and releases high when the SCLIN voltage is > 0.33 • V_{MIN}. The low offset makes the SCLOUT1 waveform almost identical to the SCLIN waveform for voltages < 0.33 • V_{MIN}. No output glitches occur as the input crosses the V_{IL} level of 0.33 • V_{MIN}, as seen in the SCLOUT1 waveform.

As the buffers are disconnected when both input and output bus voltage are > 0.33 • V_{MIN}, any noise applied to the logic high state on one side is not propagated to the other side as long as that bus voltage does not drop below 0.33 • V_{MIN}. This is seen in Figure 1 where the logic high state of SCLOUT1 is unaffected by noise on SCLIN.

Designers who are in control of the entire I²C system can set the LTC4314 to operate at frequencies of up to 1MHz by adjusting the RC load on the bus and using strong RTAs (see Table 2). The LTC4314's high-to-low propagation delay t_{PDHL} is always positive, on the order of 100ns. Depending on bus loading conditions on the upstream and downstream sides of the LTC4314, the low-to-high propagation delay t_{PDLH} of the LTC4314 can be either positive or negative. For systems operating at high frequencies (>400kHz) designers should quantify the t_{PDLH}-t_{PDHL} skew in their SDA and SCL pathways and ensure data set-up and hold times are acceptable on all buses.

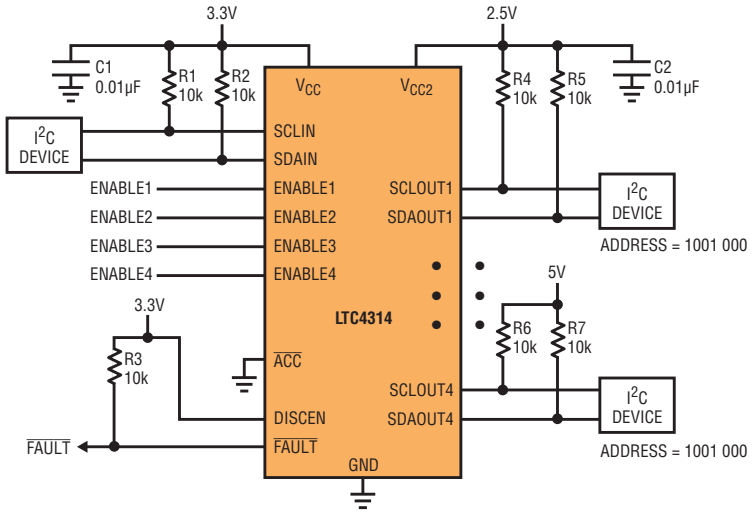

Figure 2. The LTC4314 in a nested addressing and level shifting application where a device on the upstream 3.3V bus communicates with devices on the 2.5V and 5V downstream buses. Only buses 1 and 4 are shown for simplicity.

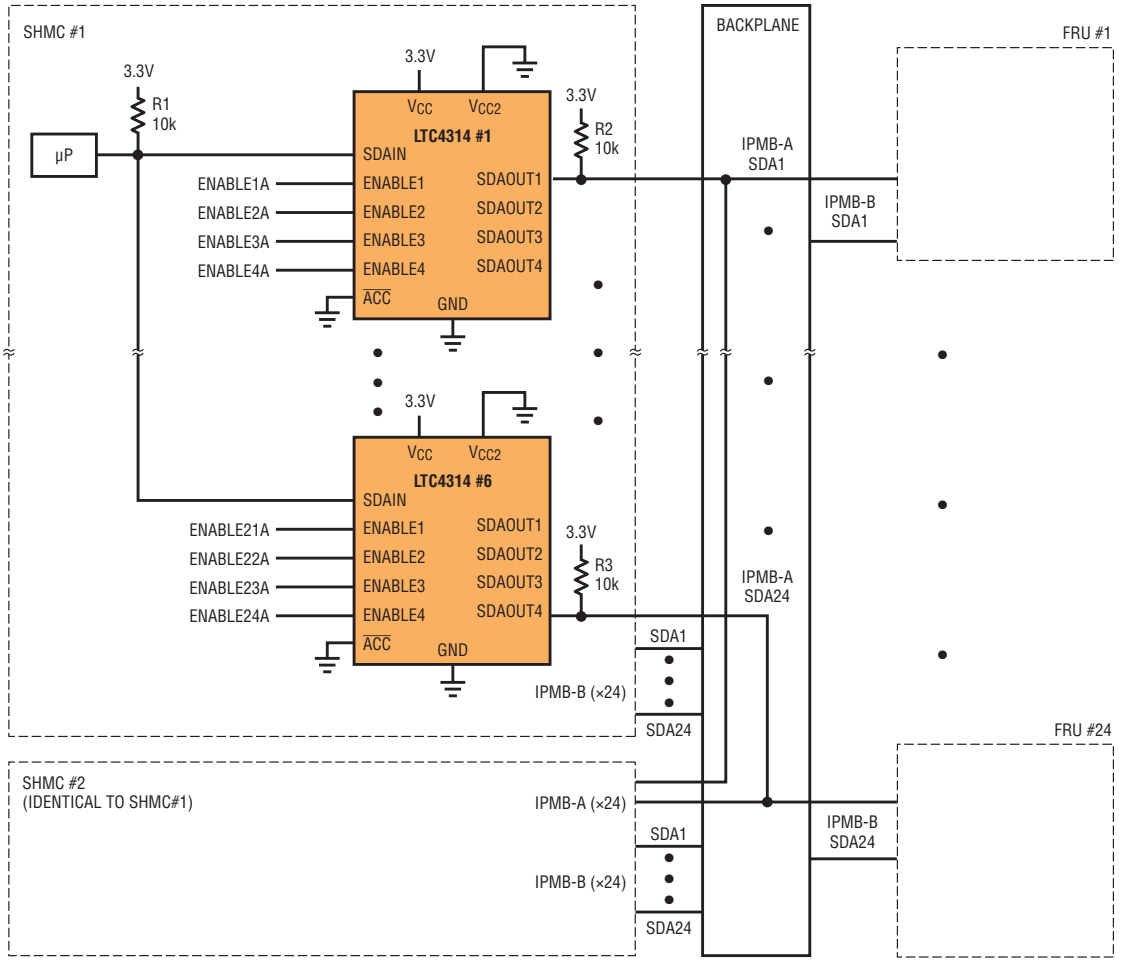

Figure 3. The LTC4314 used in a radially connected telecommunications system in a 6 × 4 arrangement. The ENABLE pins of only one shelf manager are high at any given time. Only the SDA pathway is shown for simplicity.

LEVEL TRANSLATION AND NESTED ADDRESSING

The circuit shown in Figure 2 illustrates level translation and nested addressing features of the LTC4314. The LTC4314 can level translate the input and output buses to voltages between 2.25V (1.5V and 1.8V under some circumstances) and 5.5V. In Figure 2 the LTC4314 translates a 3.3V input to 5V and 2.5V outputs. Only downstream buses 1 and 4 are shown for simplicity. Each output channel has a dedicated ENABLE pin select that allows the master to communicate independently with slave devices with identical I²C addresses provided that only one downstream bus is enabled at a time.

RADIALLY CONNECTED TELECOMMUNICATIONS APPLICATION

Figure 3 shows the LTC4314 used in a radially connected telecommunications application such as ATCA. Two shelf managers (SHMCs) are used to communicate with slave I²C devices for redundancy. Each shelf manager can have as many LTC4314s as required depending on the number of boards in the system and the desired radial/star configuration (6 × 4 in Figure 3). The ENABLE pins inside only one shelf manager are asserted high at any time. Since the LTC4314 can be cascaded with other Linear Technology bus buffers, up to 24 FRUs with Linear Technology bus buffers on their edges can be plugged into the backplane.

PARALLELING LTC4314s TO ACHIEVE MULTIPLEXING OF MORE BUSES

Multiple LTC4314s can be connected in parallel to perform higher order multiplexing. Figure 4 shows a 1:8 multiplexer using two LTC4314s.

INTEROPERABILITY WITH NONCOMPLIANT I²C DEVICES

The high buffer turn-off voltage of the LTC4314 ensures interoperability with noncompliant I²C devices that drive a high V_{OL} > 0.4V. This is shown in Figure 5 where a noncompliant device on channel 4 drives a high V_{OL} = 0.6V. The buffer turn-off voltage is 1.089V, yielding a logic low noise margin of > 0.4V at both the input and output.

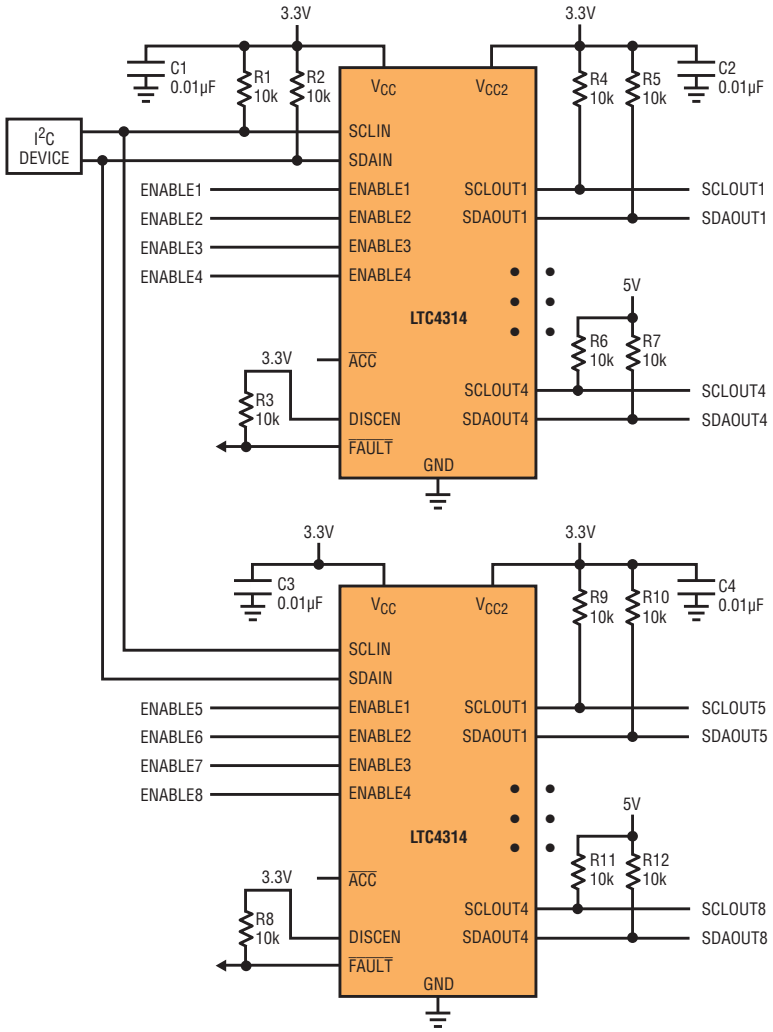

Figure 4. Paralleling LTC4314 devices to realize a 1:8 multiplexer

HOT SWAP™ APPLICATION

I/O cards can be hot swapped into the downstream buses of an LTC4314 residing on a live backplane as shown in Figure 6. Before plugging or unplugging an I/O card, care must be taken to disable the corresponding output channel so that the card does not disturb any I²C transaction that may be in progress. The connection to the inserted card must be enabled only when all ongoing transactions on the bus have completed and the bus is idle.

STUCK BUS DETECTION AND RECOVERY

Occasionally, slave devices get confused and get stuck in a low state. The LTC4314 monitors the enabled output buses to detect if clock and data have been simultaneously high at least once in 45ms. If this condition is not detected, the LTC4314 asserts the $\overline{\text{FAULT}}$ flag low. If DISCEN is tied high, the LTC4314 also disconnects the input and output sides and generates clock pulses on the enabled downstream buses in an attempt to free the stuck bus. Clocking is stopped when data releases high or 16 clocks have been generated, whichever comes first. After the final clock pulse, a stop bit is generated to reset the bus for further communication.

A rising edge on one or more ENABLE pins, after all ENABLEs have been taken low, is required to reestablish connection between the input and output. Doing this also clears the $\overline{\text{FAULT}}$ flag. The master can wait for the fault condition to clear ($\overline{\text{FAULT}}$ released high), either on its own or through the 16 clock pulses issued by the LTC4314, before toggling the LTC4314's ENABLE pins, or it can do so preemptively before the fault has cleared to reestablish connection. The master can then take appropriate action to clear the stuck low condition.

Figure 7 shows the waveforms during an SDAOUT1 stuck low and recovery event. After the 45ms timeout period has elapsed, the $\overline{\text{FAULT}}$ flag is asserted low and the input and output sides are disconnected. This causes SDAIN to release high.

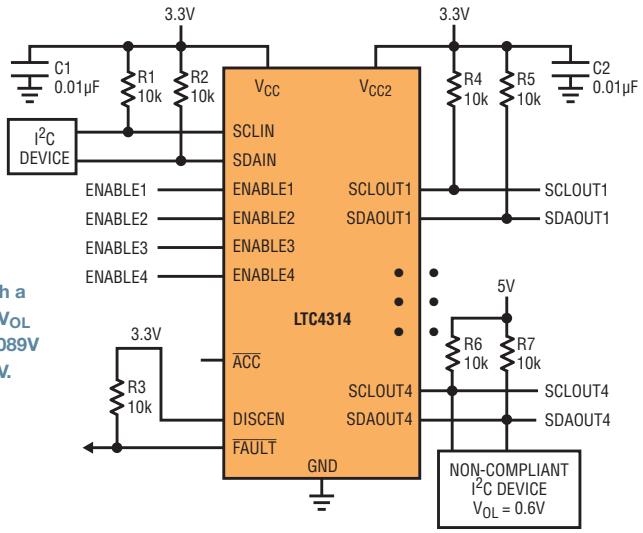

Figure 5. The LTC4314 in operation with a noncompliant I²C device that drives a V_{OL} = 0.6V. The buffer turn-off voltage is 1.089V yielding a logic low noise margin > 0.4V.

Table 2. $\overline{ACC}$ control of the rise time accelerator current I_{RTA} and buffer turn-off voltage $V_{IL,RISING}$(typ)

$\overline{ACC}$	I_{RTA}	$V_{RTA(TH)}$	$V_{IL,RISING}$
Low	Strong	0.8V	0.6V
Hi-Z	3mA	0.4 • V_{MIN}	0.33 • V_{MIN}
High	None	N/A	0.33 • V_{MIN}

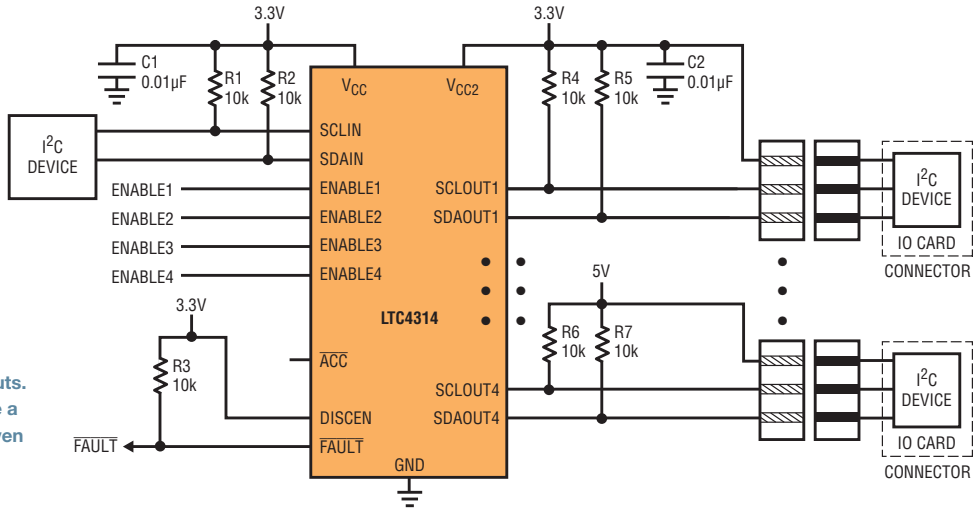

Figure 6. The LTC4314 in a Hot Swap™ application where cards are being plugged in to or unplugged from the outputs. The corresponding ENABLE pin must be driven low before a card can be plugged or unplugged and should only be driven high when the other buses are idle.

Clock pulses are generated on SCLOUT1. SDAOUT1 releases high before 16 clock pulses have been generated. Clock pulsing is stopped and a stop bit is generated. When the ENABLE1 pin is toggled, a connection is established between the input and output and a driven low level on SDAOUT1 is propagated to SDAIN.

If automatic stuck bus disconnection is not desired, this feature can be disabled by tying DISCEN low. In this case, during a stuck bus event, the $\overline{FAULT}$ flag is asserted low, but no stop bit or clock generation occurs and the input and output sides stay connected.

RISE TIME ACCELERATORS

The rise time accelerators (RTAs) of the LTC4314 can be configured either in current source mode ($\overline{ACC}$ open), slew limited switch mode ($\overline{ACC}$ grounded), or disabled ($\overline{ACC}$ high). In the current source mode the RTAs source a constant 3mA current into the bus. In the slew controlled switch mode, the RTAs turn on in a controlled manner and source current into the buses making them rise at a typical rate of 40V/µs. The RTA current and the buffer turn-off voltage are selected by the $\overline{ACC}$ setting as shown in Table 2.

For heavily capacitive buses with low to moderate noise, tie $\overline{ACC}$ low to meet system rise times and maximize SCL switching frequency. Tying $\overline{ACC}$ low provides the strongest pull-up current over the maximum voltage range. For higher noise immunity, leave $\overline{ACC}$ open or tie it to 0.5 • V_{CC} to set the buffer V_{IL} to 0.33 • V_{MIN} and to get 3mA of RTA current. The 3mA RTA current is enough to meet the 1µs standard mode I²C rise time requirement (100kHz operation) for bus capacitances up to 690pF with DC bus pull-up currents < 4mA. Tie $\overline{ACC}$ high if no acceleration is needed. To selectively disable RTAs only on the outputs, ground V_{CC2} and either ground $\overline{ACC}$ or leave $\overline{ACC}$ open.

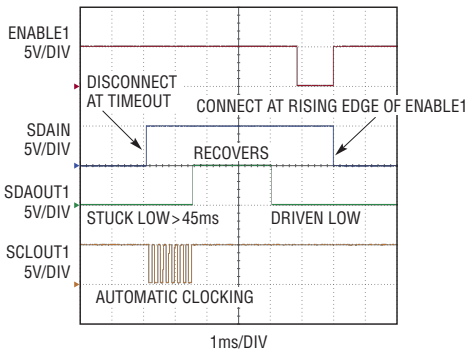

Figure 7. Bus waveforms during a SDAOUT1 stuck low and recovery event

CONCLUSION

The LTC4314 and LTC4312 are pin-selectable I²C multiplexers that solve practical design issues associated with large I²C bus systems by providing capacitance buffering, nested addressing and level translation. These parts maintain a low offset and high logic low noise margin up to 0.33 • V_{CC}. Their high bandwidth buffers and integrated RTAs allow for operation at frequencies up to 1MHz with guaranteed stability from zero to 1.2nF capacitive loads. They also disconnect and recover buses when buses are stuck low and allow I/O cards to be hot swapped into and out of live systems. ■