4- and 6-Supply Monitors Feature ±1.5% Accuracy and Watchdog Timers for Rails Down to 1.2V

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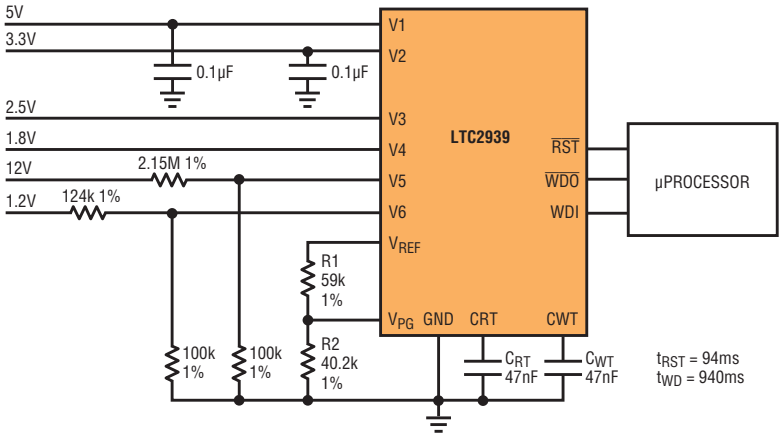
Two new power supply monitors from Linear Technology, the LTC2938 and LTC2939, are specifically designed to monitor lower supply voltages (down to 1.2V) in multivoltage systems. The LTC2938 and LTC2939 share the same architecture and differ only in the number of voltages monitored. The LTC2938 is a 4-supply monitor and comes in compact 12-pin MSOP and DFN packages. The LTC2939 monitors six supplies and is offered in a 16-pin MSOP package. Both monitors have a tight threshold accuracy of 1.5% over the operating temperature range, which eases the voltage headroom requirements of circuits powered by the monitored supplies and is much tighter than supply monitors from other manufacturers. Neither monitor requires external calibration or trimming. Both parts are designed for systems with 5% power supply tolerance.

The watchdog circuit in these monitors includes a watchdog input (WDI) and a watchdog output ($\overline{\text{WDO}}$), which facilitates microprocessor monitoring and control. The $\overline{\text{WDO}}$ output is latched low in the event of a watchdog timeout and allows the microprocessor to distinguish between resets caused by a supply undervoltage from those due to software malfunction. Both devices feature reset and watchdog timers that can be arbitrarily adjusted using external capacitors for greater flexibility in system design.

SINGLE PIN SELECTS FROM 16 POSSIBLE THRESHOLD COMBINATIONS

A single pin (V_{PG}) allows the selection of one of 16 possible threshold configurations. This programmability eliminates the need to qualify, source and stock unique part numbers for different threshold voltage combinations. Figure 1 shows a typical application of the LTC2939 monitoring 12V, 5V, 3.3V, 2.5V, 1.8V and 1.2V supplies with no external resistive dividers required for V1 through V4.

Figure 1. Typical application using the LTC2939 to monitor 6 supply voltages



The LTC2938 and LTC2939 supply threshold voltages are configured by an external resistive divider from the V_{REF} pin to ground (see Figure 2). The center tap of the divider drives the V_{PG} pin. During power-up, the voltage at the V_{PG} pin is detected and used to select one of 16 possible configurations as shown in Table 1. Recommended ±1% resistor values to select each configuration can also be found in Table 1.

The actual supply thresholds are set by integrated precision dividers for 5V, 3.3V, 2.5V, 1.8V, 1.5V and 1.2V supply monitoring. For modes 6 (see Figure 1), 7 and 10, no external resistors are needed at the comparator inputs (V1 through V4) to monitor the combinations of voltages shown in Table 1. For other supply combinations, uncommitted comparators (in ADJ mode) with 0.5V thresholds allow virtually any positive supply to be monitored as shown in Figure 3. The V4 input also monitors negative voltages with the same 1.5% accuracy using the integrated buffered reference for offset (see Figure 4). The LTC2939 has two additional uncommitted

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comparators with 0.5V thresholds for systems that need to monitor up to six supplies. All uncommitted inputs (V3 through V6) can be disabled by tying them to V1.

TIGHT THRESHOLD ACCURACY PREVENTS NUISANCE RESETS AND SYSTEM MALFUNCTIONS

Consider a 5V system with ±5% supply tolerance. The 5V supply may vary between 4.75V to 5.25V. System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). A perfectly accurate supervisor for this supply generates a reset at exactly 4.75V. However, no supervisor is perfect. The actual reset threshold of a supervisor fluctuates over a specified band; the LTC2938 and LTC2939 vary ±1.5% around their nominal threshold voltage over temperature (Figure 5). The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band.

The LTC2938 and LTC2939 boast a ±1.5% reset threshold accuracy, so a "5%" threshold is usually set to 6.5% below the nominal input voltage. Therefore, a typical 5V, "5%" threshold is 4.675V. The threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued. A less accurate monitor increases the required system voltage margin and increases the probability of system malfunction. The tight ±1.5% accuracy specification of the LTC2938 and LTC2939 improves the reliability of the system over monitors with wider threshold specifications.

Table 1. Voltage threshold modes

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	V_{PG}/V_{REF}
0	5.0	3.3	ADJ	ADJ	Open	Short	0
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	1.8	1.5	ADJ	71.5	28	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59	40.2	0.406
7	3.3	1.8	1.5	1.2	53.6	47.5	0.469
8	3.3	1.8	1.2	ADJ	47.5	53.6	0.531
9	3.3	1.8	ADJ	ADJ	40.2	59	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28	71.5	0.719
12	3.3	1.8	ADJ	–ADJ	22.1	78.7	0.781
13	3.3	1.5	ADJ	ADJ	16.2	86.6	0.844
14	5	3.3	1.8	ADJ	9.53	93.1	0.906
15	3.3	1.2	ADJ	ADJ	Short	Open	1

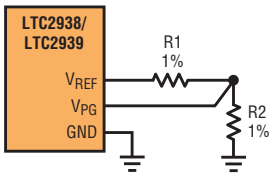


Figure 2. Programming the voltage monitoring mode

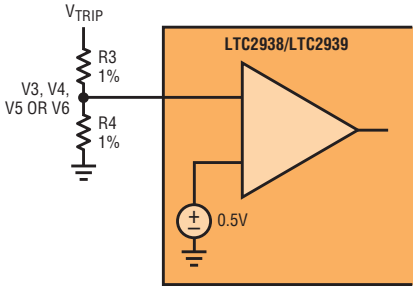


Figure 3. Setting the positive adjustable trip point, $V_{TRIP} = 0.5V \bullet (1 + R3/R4)$

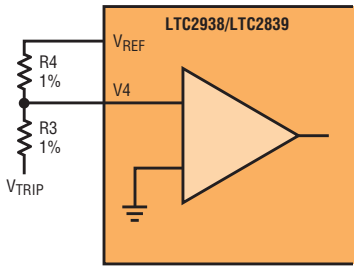


Figure 4. Setting the negative adjustable trip point, $V_{TRIP} = -V_{REF} \bullet (R3/R4)$

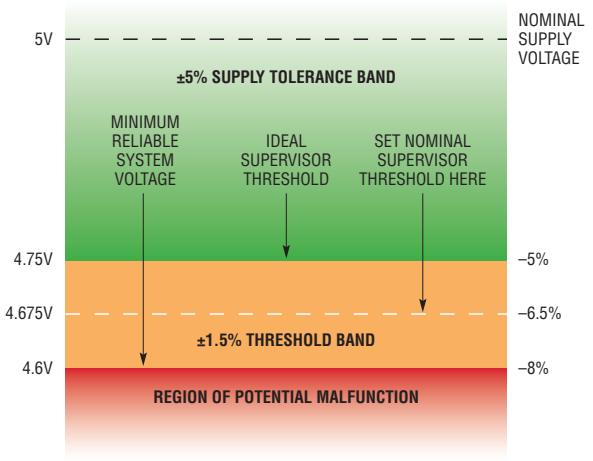


Figure 5. Tight 1.5% threshold accuracy improves system reliability

BUILT-IN GLITCH IMMUNITY

Monitored supply voltages are not perfectly flat DC signals but are contaminated by high frequency components caused by a number of sources such as the output ripple of the power supply or coupling from other signals. If the monitored voltage is near or at the reset threshold voltage, this noise could cause spurious resets. Fortunately, the LTC2938 and LTC2939 have been designed to deal with this potential issue, so spurious noise is of little to no concern.

Some supply monitors overcome spurious noise by adding hysteresis to the input comparator but this degrades monitor accuracy because the true accuracy of the trip threshold is now the percentage of added hysteresis plus the advertised accuracy of the part. The LTC2938 and LTC2939 do not use hysteresis, but instead use an integration scheme that requires transients to possess enough magnitude and duration to switch the comparators. This suppresses spurious resets without degrading the monitor accuracy. Figure 6 shows the response time of the input comparator versus input overdrive.

ADDITIONAL GLITCH FILTERING

Although all the comparators monitoring the supplies have built-in glitch filtering, additional bypass capacitors should be added to V1 and V2 as the higher of these voltages supplies the V_{CC} for the entire chip. Bypass capacitors may also be added to the V3, V4, V5 and V6 inputs to suppress troublesome noise on these supplies.

ADJUSTABLE RESET TIMEOUT PERIOD

The reset timer determines the minimum time duration (t_{RST}) that the $\overline{RST}$ output pulls low to reset the microprocessor and its peripheral circuits (see Figure 7). These are reset whenever any of the monitored supplies falls below its voltage threshold long enough to defeat the glitch filters or a watchdog timeout occurs. Once all the supplies are back above their respective threshold voltages again, the reset timer is started. $\overline{RST}$ remains low for t_{RST} seconds before $\overline{RST}$ is pulled back high, taking the microprocessor and the peripheral circuits out of reset.

To suit a variety of microprocessor applications, t_{RST} can be adjusted by connecting a capacitor (C_{RT}) between the CRT pin and ground. t_{RST} is chosen to allow the power supplies to settle down and ensure proper system reset. The value of this capacitor can be calculated from:

$$C_{RT} = \frac{t_{RST}}{2M} = 500\ \frac{pF}{ms} \bullet t_{RST}$$

This capacitor is charged by a nominal charging current of 2µA. The accuracy of the timeout period can be affected by capacitor leakage, so low leakage ceramic capacitors are recommended for C_{RT}. Leaving the CRT pin open generates a minimum reset period of approximately 20µs, a number that is highly sensitive to PCB stray capacitances.

OPEN-DRAIN RESET OUTPUT

The $\overline{RST}$ output of the LTC2938 and LTC2939 is an open-drain output and is internally pulled up to V2 by a weak current source (6µA). $\overline{RST}$ can be pulled to voltages higher than V2 by an external pull-up resistor. Multiple devices operating from different I/O voltages can be connected in a wired-OR configuration where the open-drain outputs are all tied together. This allows more than six supplies to be monitored with the same $\overline{RST}$ line. The open-drain output also permits $\overline{RST}$ to drive I/O circuits operating from different supply voltages and to reset these circuits at the same time as the microprocessor for a clean system restart. $\overline{RST}$ is guaranteed to be in the low state for V_{CC} > 1V ensuring reliable reset of the microprocessor until all the supplies have reached safe levels regardless of supply turn-on characteristics.

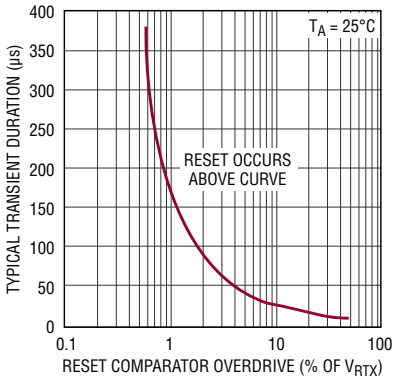


Figure 6. Transient duration versus comparator overdrive

WATCHDOG TIMER

The watchdog timer provides a means for a system to recover from software malfunctions or errors. For example, systems can fail when cosmic radiation corrupts registers or memory in today's microprocessors built with ultrafine geometries. A well designed watchdog timer is crucial for recovery from such conditions. The LTC2938 and LTC2939 watchdog timer works independently of the microprocessor and starts working on power-up once all the supplies are valid.

The watchdog timer starts whenever $\overline{RST}$ goes from low to high. The system software must clear the watchdog timer periodically to prevent it from timing out and resetting the microprocessor. This is done by flipping the state of the watchdog input (WDI) before the end of the watchdog timeout period (t_{WD}). Failing this, the watchdog times out and the watchdog output ($\overline{WDO}$) is latched low, which in turn causes $\overline{RST}$ to be pulled low, for a reset timeout period (t_{RST}), to reset the microprocessor. Once the reset timeout period has expired, the latched state of the watchdog output ($\overline{WDO}$) is cleared when transitions on the watchdog input (WDI) resume.

Before flipping WDI, the microprocessor may check the system to make sure that it is working properly, for it is possible for the code that kicks the watchdog to remain alive while the rest of the system has malfunctioned. If the system checks fail, then letting the watchdog timeout intentionally causes the system to reset completely for a proper recovery.

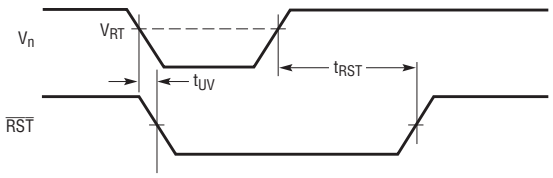
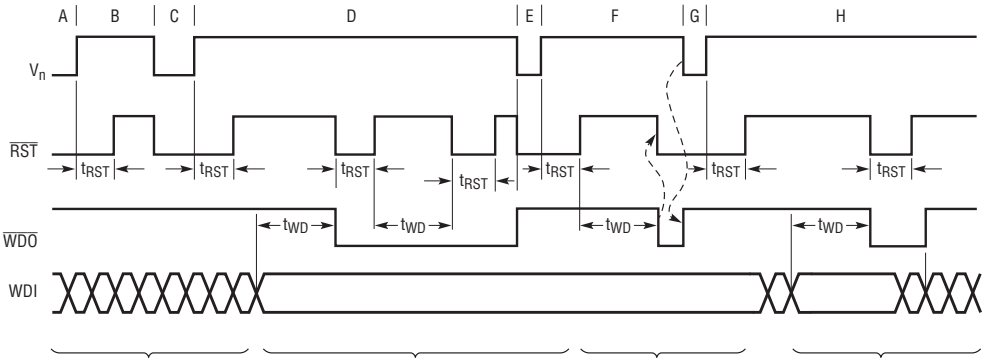


Figure 7. Reset timing

The WDI pin is a 3-state input. If this pin is left unconnected or tied to a high impedance node or if it is driven from a logic high or low state to a high impedance state, the watchdog timer is disabled and the C_{WT} capacitor is discharged to ground but $\overline{WDO}$ is not cleared. When left disconnected, a weak internal buffer drives the WDI pin to about 0.9V to detect a high impedance condition. This pin sinks or sources 10µA or less within the 0.7V to 1.1V range that defines the high impedance point. While WDI is high or low, it can sink or source up to 30µA. Another way to disable the watchdog is to simply short CWT to ground as this prevents timer operation. Disabling the watchdog is useful in systems that require the low supply monitoring capability of the LTC2838/39 but not the watchdog function.

Forcing or tying WDI either high or low enables the watchdog timer. WDI must transition between its V_{IL} and V_{IH} logic levels to either reset the timer to prevent timeout and discharge the C_{WT} capacitor

Figure 8. Watchdog and reset timing



The LTC2938 and LTC2939 are specifically designed to allow a microprocessor to distinguish between resets caused by input supply undervoltage or those due to software malfunction (watchdog timeout).

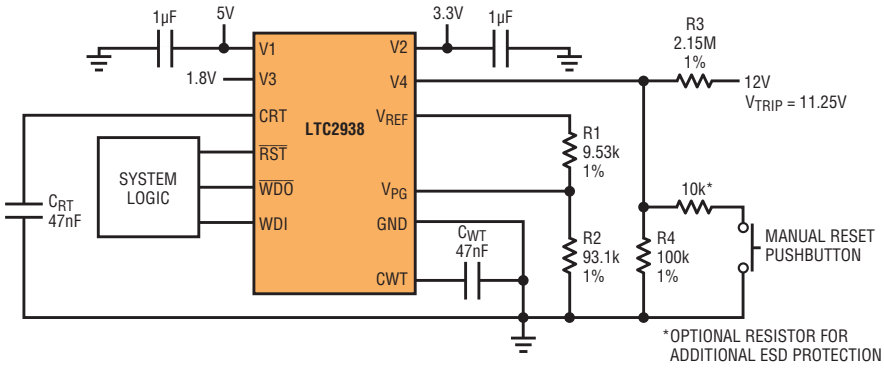


Figure 9. Quad-supply monitor (mode 14) with pushbutton reset

to ground or to clear the watchdog timer output ($\overline{WDO}$). Alternatively, if the WDI pin is pulsed between its low and high states to clear the watchdog timer, the pulse width must be at least 2µs. If WDI is driven from a high impedance state to a high or low logic state, $\overline{WDO}$ is not reset but the watchdog timer starts to run. This preserves the state of WDO when the microprocessor resets and takes its I/O pins out of high impedance. While $\overline{RST}$ is low, transitions on the WDI pin are ignored so that $\overline{WDO}$ remains latched for at least one reset period (t_{RST}).

OPEN-DRAIN WATCHDOG OUTPUT

The output of the watchdog timer or $\overline{WDO}$ is an open-drain output with a weak pull-up (6µA) to V2. Like $\overline{RST}$, it may be pulled to a higher supply voltage via an external pull-up resistor or connected in a wired-OR fashion to other watchdog outputs. $\overline{WDO}$ and $\overline{RST}$ should not be connected together since the first watchdog timeout will force $\overline{RST}$ low, which resets the microprocessor, making it impossible to toggle WDI to clear $\overline{WDO}$.

ADJUSTABLE WATCHDOG TIMEOUT PERIOD FOR SOFTWARE OPTIMIZATION

The LTC2938 and LTC2939 watchdog timeout period can be adjusted for optimal software performance. A capacitor connected from the CWT pin to ground sets the watchdog time out period. The value of the capacitor is determined from:

$$C_{WT} = \frac{t_{WD}}{20M} = 50\ \frac{pF}{ms} \bullet t_{WD}$$

Leaving CWT unconnected generates a minimum watchdog timeout of approximate 200µs. The maximum timeout period is limited by the largest available low leakage capacitor. Since the charging current is only about 2µA, low leakage ceramic capacitors are also recommended for C_{WT}. The value of C_{WT} takes into account the software overhead of having to hit the WDI pin periodically and how quickly the system needs to recover from a malfunction.

RESET AND WATCHDOG TIMING

The timing diagram in Figure 8 shows the relationship between the reset and watchdog timers. V_n represents any of the monitored supplies and a low state means an undervoltage (UV) condition. During a UV condition, $\overline{RST}$ and $\overline{WDO}$ are forced low and high respectively. In addition, the reset and watchdog timers are disabled and the C_{RT} and C_{WT} capacitors are discharged to ground. $\overline{RST}$ low (see time intervals A, C, E, and G) resets the microprocessor.

Once the undervoltage condition clears (V_n high), the reset timer is enabled. $\overline{RST}$ and $\overline{WDO}$ remain low and high respectively until the end of t_{RST} when $\overline{RST}$ is pulled high to take the microprocessor out of reset allowing it to start running the system software. This is seen during time intervals B, D, F and H. Once out of reset, the watchdog timer starts to run. During normal operation, the microprocessor toggles the WDI pin periodically to prevent watchdog timeout.

The LTC2938 (4-supply) is available in a 12-pin MSOP package while the LTC2939 (6-supply) is available in 16-pin MSOP and DFN packages.

However, if the software malfunctions and stops toggling WDI, the watchdog timer times out and latches $\overline{WDO}$ to a low state (e.g. interval D) and remains low until an undervoltage event occurs or WDI is toggled. Upon watchdog timeout, $\overline{RST}$ is also pulled low, resetting the microprocessor for t_{RST} seconds. It is then pulled high, allowing the microprocessor to restart the software from the beginning and recover from the malfunction. While the reset timer is running ($\overline{RST}$ low), toggling WDI does not clear $\overline{WDO}$ from a low state as seen at the extreme right of Figure 8. On exiting reset, the microprocessor examines the state of $\overline{WDO}$ to determine if the reset is caused by an undervoltage condition, which resets $\overline{WDO}$ to a high state; or by a watchdog timeout as indicated by a low $\overline{WDO}$ state. After $\overline{RST}$ is released, any transition between logic low and logic high at WDI clears $\overline{WDO}$. Therefore, the WDI pin should not be toggled until $\overline{WDO}$ state has been checked by the microprocessor. Some microprocessors place their I/O pins in high impedance during reset. Putting WDI in high impedance disables the watchdog timer and discharges C_{WT} to ground but does not affect the state of $\overline{WDO}$. If the microprocessor does not clear $\overline{WDO}$ and it remains in its latched low state, the reset and watchdog timers will run alternately and $\overline{RST}$ is pulled low each time the reset timer runs, thus repeatedly resetting the microprocessor. This can be useful in systems where $\overline{RST}$ is used to drive an interrupt rather than to reset the system, and the interrupt service routine hangs or is flawed.

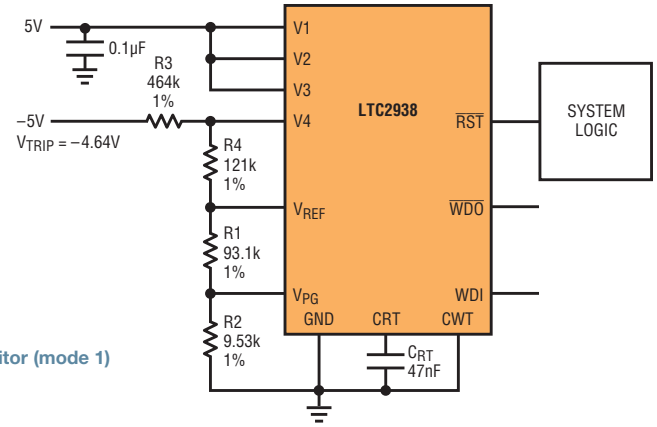


Figure 10. A ±5V supply monitor (mode 1) with unused inputs disabled

APPLICATIONS

Figure 9 shows a quad supply monitor with pushbutton reset. R1 and R2 are chosen to select mode 14 (see Table 1). In this mode, the V1, V2 and V3 inputs of the LTC2938 monitor 5V, 3.3V and 1.8V respectively while the V4 input, which is an adjustable input, is configured by resistors R3 and R4 to monitor a 12V supply with a trip point of 11.25V. The pushbutton function is simply implemented by shorting out the R4 resistor so that the V4 input registers an undervoltage condition, causing the LTC2938 to reset.

Figure 10 shows a circuit that monitors a split supply of ±5V. In this application, the LTC2938 is configured in mode 1 in which V1 monitors 5V and V4 becomes an adjustable pin that monitors negative voltages. R3 and R4 configure V4 to monitor –5V with a threshold of –4.64V. In this application, the CWT pin is tied to ground to disable the watchdog circuit. The V2 and V3 inputs are unused and are tied to V1 to prevent the V2 and V3 comparators from affecting the $\overline{RST}$ Output.

CONCLUSION

The LTC2938 and LTC2939 are specifically designed to allow a microprocessor to determine whether a system reset is due to undervoltage or to software malfunction (watchdog timeout). They can monitor four or six supplies respectively and come in small DFN or MSOP packages to save valuable board space. The LTC2938 is available in a 12-pin MSOP package while the LTC2939 is available in 16-pin MSOP and DFN packages. Both include single-pin selection of one of 16 possible supply threshold configurations. Thresholds are accurate to ±1.5%, which simplifies system design by narrowing the voltage range in which the system must operate. Commercial, industrial and automotive temperature grades are all available. Comparator glitch immunity prevents false resets and adjustable reset and watchdog timeout periods allow customization to the hardware and software requirements of individual systems. ■