Buck, Boost and LDO Regulators Combined in a 4mm × 4mm QFN

by Chris Falvey

Introduction

The LT3570 simplifies complex multi-rail power supply designs by integrating three DC/DC regulators into a single package: a current mode buck regulator, a current mode boost regulator, and an LDO controller.

The buck and boost regulators each have a current limit of 1.5A. The LDO controller has an output current capability of 10mA and combines with an external NPN transistor to create a linear regulator. The frequency of the switching regulators can be set from 500kHz to 3MHz by an external resistor or synchronized to an external oscillator. The independent input voltages for each regulator offers a wide operating range from 2.5V up to 40V. Each regulator also has its own shutdown circuitry and the buck and boost regulators have their own soft-start circuitry.

The typical application shown in Figure 1 generates 3.3V at 1A from the buck regulator, 2.5V at 40mA from the LDO controller and 12V at 275mA from the boost regulator, all from a 5V input supply voltage and with an overall efficiency around 85%.

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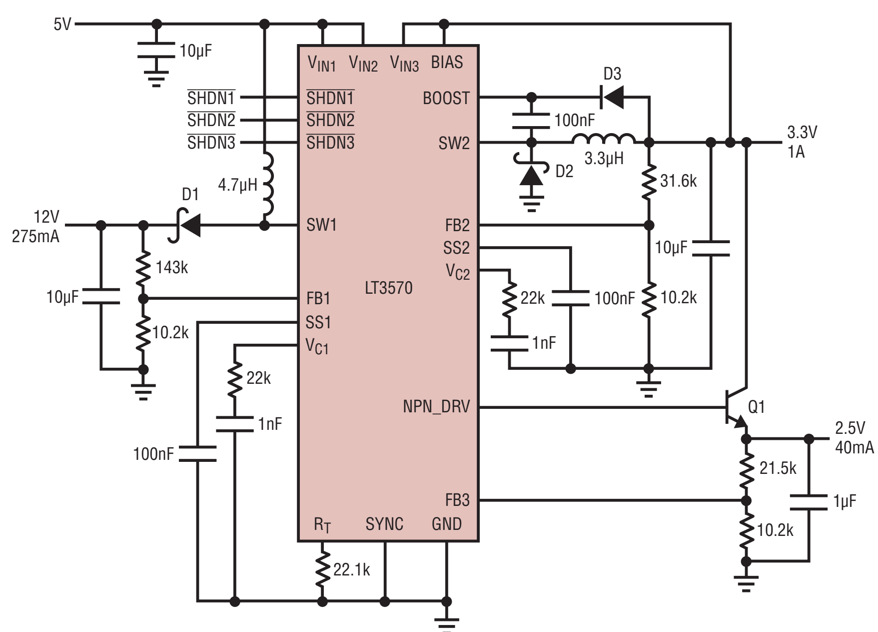
Features

Available in either a 24-lead 4mm × 4mm QFN or a 20-pin TSSOP package, the LT3570 is a constant frequency current mode regulator. If all $\overline{\text{SHDN}}$ pins are held low, zero quiescent current is drawn from the input supplies and the part is turned off. Any $\overline{\text{SHDN}}$ pin voltage exceeding 1.5V will turn on the corresponding regulator. A precise shutdown pin threshold allows for easy integration of input supply undervoltage lockout. All three regulators share the same internal 800mV reference voltage. For each regulator, an external resistor divider programs the output voltage to any value above the part's reference voltage. The switching frequency is set with an external resistor from the R_T pin to GND. This allows a trade off between minimizing component size (by using higher switching frequencies) and maximizing efficiency (by using lower switching frequencies). Additionally, running at a low switching frequency allows for applications that require larger V_{IN}-to-V_{OUT} ratios. The adjustable and synchronizable switching frequency also allows the user to keep the switching noise out of critical wireless and audio bands.

Both the buck and boost regulators control the slew rate of the output



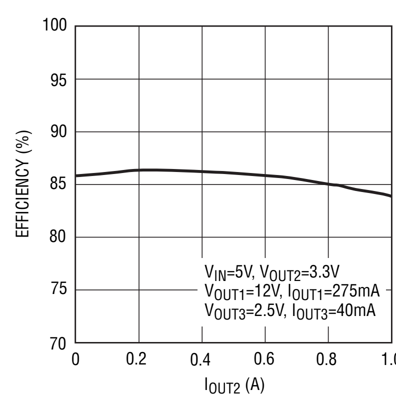


Figure 1. A typical 5V input to 3.3V, 2.5V and 12V application

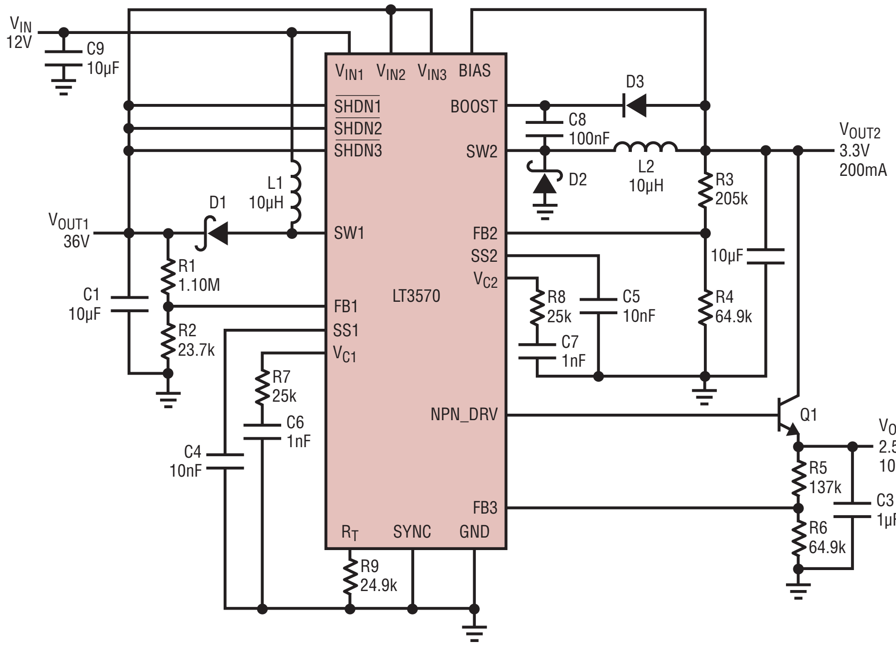


Figure 2. Dying gasp system keeps power even when battery is disconnected.

voltage during start-up. A controlled ramp reduces inrush current on the input supply and minimizes output overshoot. An external capacitor connected between the SS pin and ground programs the slew rate. The voltage on the SS pin overrides the internal reference voltage to the error amplifier and is charged by a 4.5µA internal current source.

The BIAS pin allows the internal circuitry to draw current from a lower voltage supply than the input, reducing power dissipation and increasing efficiency. Normally, the quiescent current is supplied from V_{IN2}, but when the voltage on the BIAS pin exceeds 2.5V the current is supplied from the BIAS pin. The BIAS pin is only available on the 24-lead QFN package.

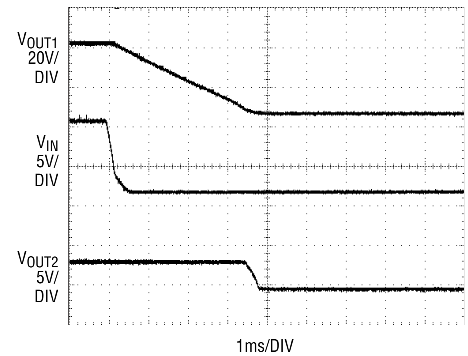


Figure 3. Output waveforms when power is removed from the circuit in Figure 2

Applications

"Dying Gasp" Application

The LT3570 provides an ideal solution for any "dying gasp" system. Figure 2 shows a typical application powering an airbag controller. In an automobile accident, the battery may get disconnected from the shock sensors yet the airbag must still fire. In this application, the battery supplies power to the boost regulator. V_{OUT1} is set to 36V and drives V_{IN2} and V_{IN3}, the inputs to the buck regulator and the LDO controller, respectively. Even after the input supply is removed, the buck regulator and the LDO continue to function properly for more than 3ms, as the energy continues to be supplied from the output capacitor of the boost regulator. The buck regulator turns off when V_{IN2} approaches the input undervoltage lockout of 2.3V (see Figure 3). *continued on page 41*

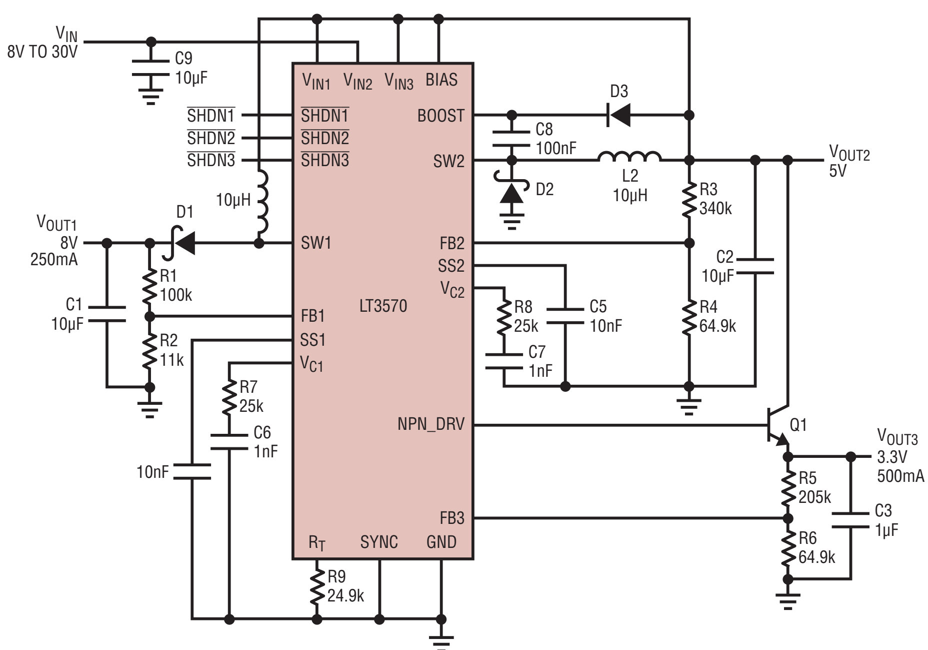


Figure 4. DSL modem application

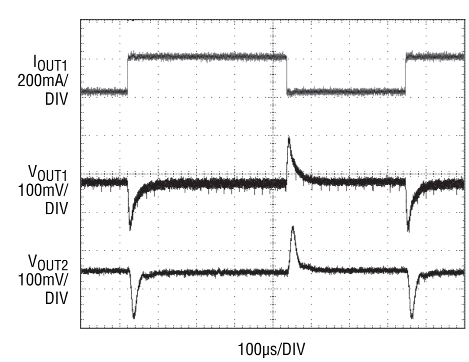


Figure 5. Step response of Figure 4 with boost current stepped from 200mA to 400mA

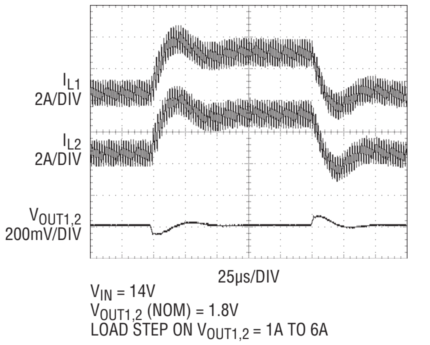


Figure 2. Post-package trimming of the LTC3853's current sense comparators provides excellent current sharing between channels 1 and 2, even during a transient.

sync with frequencies between 250kHz and 750kHz.

The LTC3853 can be set to operate in one of three modes under light load conditions. Burst Mode operation offers the highest light load efficiency by switching in a "burst" of one to several pulses replenishing the charge stored in the output capacitors, followed by a long sleep period when the load current is supplied by the output capacitors. Forced continuous mode offers fixed frequency operation from no load to full load, providing the lowest output voltage ripple at the cost of light load efficiency. Pulse-skipping mode operates by preventing inductor current reversal by turning off the synchronous switch as needed. This mode is a compromise between the other two modes, offering lower ripple than Burst Mode operation and better light load efficiency than forced continuous mode. Regardless of the mode selected, the LTC3853 operates in constant frequency mode at higher load currents. Figure 3 shows the efficiency in each of the three modes.

Each of the LTC3853's channels can be enabled with its own RUN pin, or slewed up or down with its own TRACK/SS pin. Tracking holds the feedback voltage to the lesser of the internal reference voltage or the voltage on TRACK/SS, which can be brought up with an external ramp or with its own 1.2µA internal current source. With all of the TRACK/SS pins held low and any output enabled through its RUN pin, the 5V $INTV_{CC}$ is still available for ancillary keep-alive circuits.

Pulse-skipping mode is always enabled at start-up to prevent sinking current from a pre-biased output voltage. When the output reaches 80% of the set value, the part switches over to forced continuous mode until the output has entered the POWER GOOD window, at which point it switches over to the selected mode of operation. Forced continuous mode reduces the output ripple as the power good threshold is crossed, to ensure that the POWER GOOD indicators make just one low to high transition.

Three different max current comparator sense thresholds can be set via the ILIM pin. The current is sensed using a high speed rail-to-rail differential current sense comparator. The circuit of Figure 1 uses accurate sense resistors between the inductors and the outputs. For reduced power loss at high load currents, the LTC3853 can also monitor the parasitic resistance of the inductor (DCR sensing). Peak inductor current is limited on a cycle-by-cycle basis and is independent of duty cycle. If load current is high enough to cause the feedback voltage

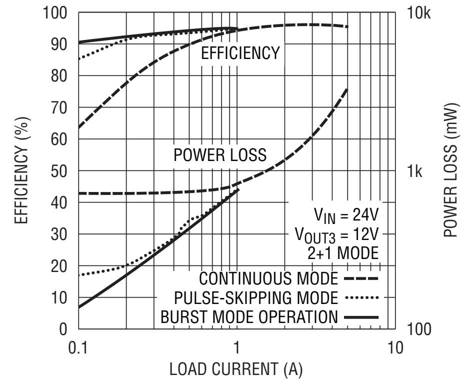


Figure 3. Efficiency for channel 3 in Figure 1—in each of the three modes of operation

to drop, current limit fold back protects the power components by reducing the current limit. For predictable tracking, current limit fold back is disabled during start-up. Input undervoltage lockout, output overvoltage shutdown and thermal shutdown also protect the power components and the IC from damage.

Conclusion

The LTC3853's small footprint belies its versatility and extensive feature set. From inputs up to 24V it can regulate three separate outputs, or it can be configured for higher currents by tying channels 1 and 2 together. Either way, the phase relationship between channels is automatically optimized to reduce ripple currents. At low duty cycles, the short minimum on-time ensures constant frequency operation, and peak current limit remains constant even as duty cycle changes. The cost-effective LTC3853 incorporates these features, and more, into a 40-pin 6mm × 6mm QFN package.

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DSL Modem

Figure 4 shows an application for a DSL modem or set-top box. The supply voltage for V_{IN2} comes from a wall adapter that can range from 8V to 30V. This voltage is stepped down to 5V at 100mA for V_{OUT2}, which then supplies the power to drive both the boost regulator and LDO controller. V_{OUT1} is set to 8V at 200mA and V_{OUT3} is set to 3.3V at 500mA. Figure 5 shows the load step response of V_{OUT1} and V_{OUT2} with a 200mA load step on V_{OUT1}.

Conclusion

The LT3570 is a monolithic dual output switching regulator (buck and boost) with a NPN LDO controller and is ideal for a broad variety of applications. Because the LT3570 offers a high level of system integration, it greatly simplifies board design for complex applications that need multiple voltage supply rails. With the flexibility of independent supply inputs and adjustable frequency, the user can set a wide array of custom output voltages. The LT3570 is a feature rich solution that satisfies the needs for multiple output voltages in a compact solution.