Ultrafast, Low Noise, Low Dropout Linear Regulators Running in Parallel Produce Clean, Efficient, High Current Point-of-Load Power for FPGA and Server Backplanes

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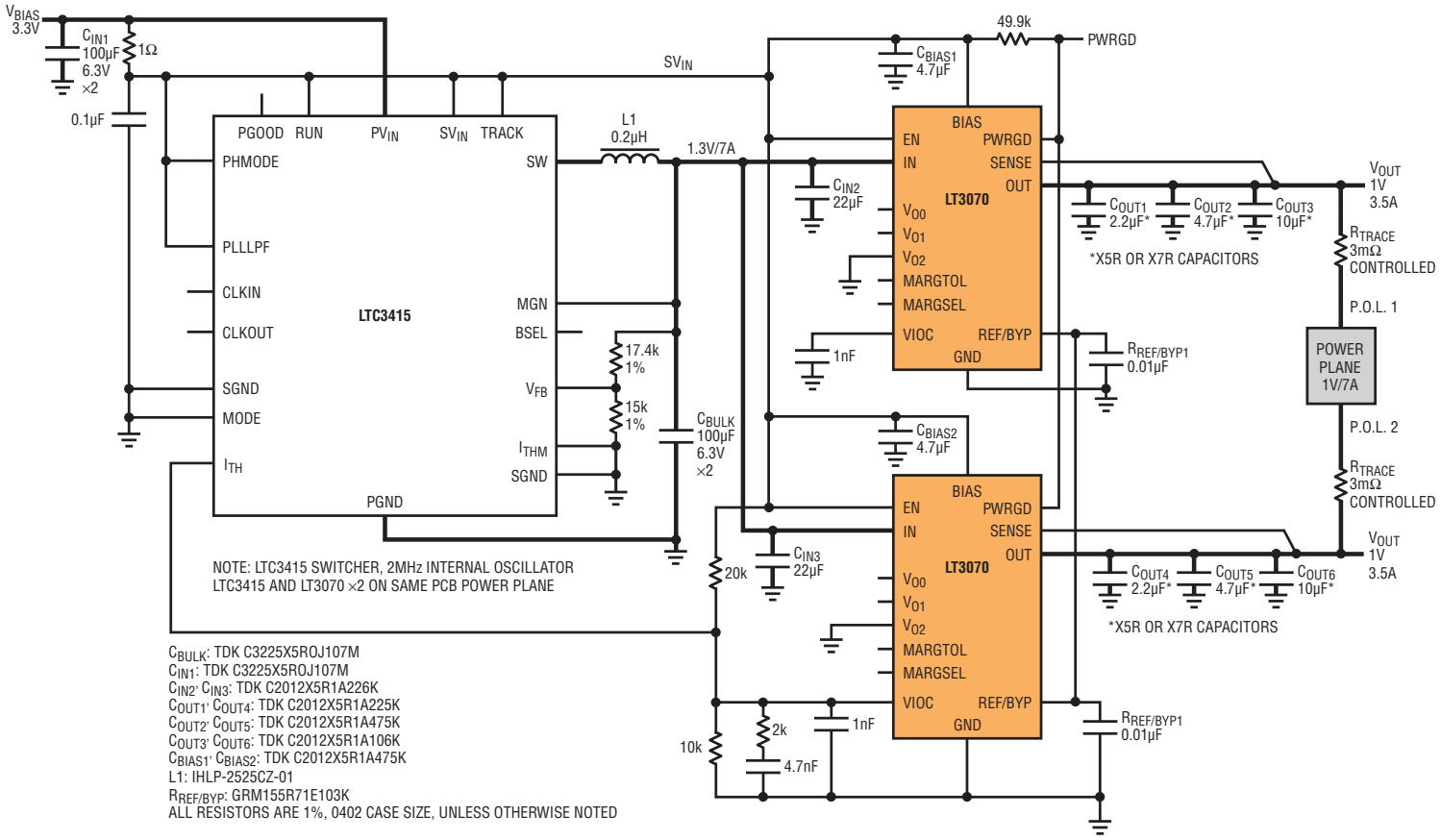
The latest FPGAs and processors have migrated to deep submicron geometries with gigahertz+ data rates and integrated telemetry channels that operate from 0.9V to 1.8V supply rails. The transient power demand for these processors can reach more than 10A peak current in nanoseconds. At these processor speeds and high currents even the local PCB backplane impedances around the processor can contribute to supply droop, where millivolts of supply droop or supply noise can degrade data integrity.

To manage the system power distribution, switching regulators may be used locally to downconvert from a higher voltage rail. These regulators are traditionally bypassed with a large quantity of bulk caps to reduce ripple and buffer the load transients. Unfortunately, bulk tantalum and electrolytic caps have parasitic ESL and ESR that limits their ability to bypass fast high current load transients. To a lesser extent, even large ceramic caps are bandwidth limited by their inherent ESL.

The LT3070 and LT3071 family of UltraFast™ transient response, low noise, low dropout linear regulators addresses this challenge. The high bandwidths of the LT3070 and LT3071 reduce the supply impedance at the point-of-load using

Figure 1. Paralleled LT3070s with VIOC control of upstream LTC3415 switcher implementation



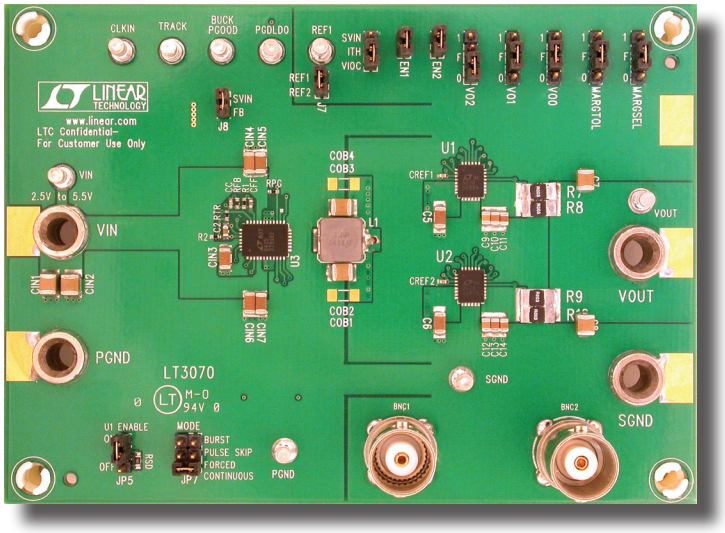


Figure 2. Two paralleled LT3070s clean up the power produced by an LTC3415 switching regulator with minimal impact on efficiency and board real estate

only a few small, low ESR, ceramic capacitors, saving bulk capacitance and cost. These linear regulators supply up to 5A of output current with a typical dropout voltage of 85mV. A 0.01µF reference bypass capacitor decreases output voltage noise to 25µV_{RMS}, yielding an output that is not only responsive but also very quiet. The LT3070 and LT3071 incorporate a unique VIOC tracking function to control the switching regulator powering the input.

The LT3070 has digital controls that allow the user to margin the system output voltage in increments of ±1%, ±3% or ±5%. The LT3071 has an analog margining pin that allows the user to margin the system output voltage ±10%. The LT3071 also has a IMON output current monitor to support system load current diagnostics.

The features included in the LT3070 and LT3071 make them ideal for high performance FPGAs, microprocessors or sensitive communication supply applications.

A TIME FOR SHARING

Multiple LT3070/71s can be paralleled to increase available output current with minimal ballasting. In fact, eight LT3070s have successfully been paralleled to share a common 30A load.

Simply tie the REF/BYP pins of the paralleled regulators together. This effectively gives an averaged value of multiple 600mV reference voltage sources. Tie the OUT pins of the paralleled regulators to the common load plane through a small piece of PC trace ballast or an actual surface mount sense resistor beyond the primary output capacitors of each regulator.

The required ballast is dependent on the application output voltage and peak load current. The recommended ballast is the value that contributes 1% to load regulation. For example, two LT3070/71 regulators configured to output 1V, sharing a 10A load require 2mΩ of ballast at each output. The Kelvin SENSE pins connect to the regulator side of the ballast resistors to keep the individual control loops from conflicting with each other, as shown in Figure 1. Keep this ballast trace area free of solder to maintain a controlled resistance.

SIMPLIFIED INTEGRATION WITH SWITCHING REGULATORS YIELDS HIGH EFFICIENCY

Figure 1 illustrates the use of the LT3070's VIOC function. This feature transfers control of the switcher output (LDO input) to one of the LDOs such that the digital output control of the LDO sets the output of the LTC3415 to maintain 300mV headroom V_{IN} to V_{OUT}, across the LDOs , optimizing power dissipation on the fly.

The demo board in Figure 2 demonstrates a single LTC3415 switching regulator supplying two LT3070 LDOs with co-joined outputs ballasted by sense resistors. Close examination of this board layout reveals a pair of small routes from the switcher PGND to the LDO SGND. Likewise, similar routes are incorporated in a buried layer between the switcher output and the LDO inputs, terminated by the LDO input decoupling capacitors. These serve as π-filters to help isolate the LDO reference from the switching noise.

Figure 3 illustrates the quiet performance the two LT3070s sharing a pulsed 0.1A to 7A load while exhibiting less than 10mV of excursion on the output load. This is in sharp contrast to the relatively noisy load regulation waveform of the of the adjoining switching regulator.

In conclusion, the LT3070 and LT3071 provide power efficient, area efficient, UltraFast transient response, low noise, point-of-load regulation for the most demanding server applications. ■

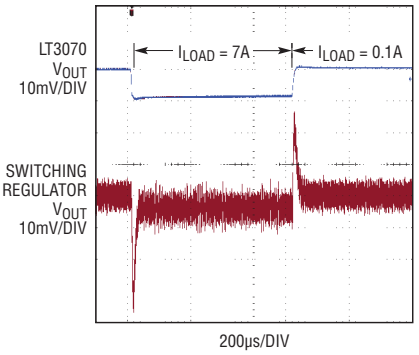


Figure 3. Waveform of paralleled LT3070s contrasted to the LT3415 switcher output