Driving Lessons for a Low Noise, Low Distortion, 16-Bit, 1Msps SAR ADC

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It is challenging to design an ADC driving topology that delivers uncompromising performance, especially when designing around an ultralow noise SAR ADC such as the 1Msps LTC2393-16. For both single-ended and differential applications, a well thought out driving topology fully realizes the ultralow noise and low distortion performance required in your data acquisition system.

The LTC2393-16 is the first in a family of high performance SAR ADCs from Linear Technology that utilizes a fully differential architecture to achieve an excellent SNR of 94.2dB and THD of –105dB. In order to take full advantage of the ADC performance, we present driving solutions for both single-ended and differential applications. Both topologies fully demonstrate the ultralow noise and low distortion capabilities of the LTC2393-16.

SINGLE-ENDED TO DIFFERENTIAL CONVERTER

The circuit of Figure 1 converts a single-ended 0V to 4.096V signal to a differential ±4.096V signal. This circuit is useful for sensors that do not produce a differential signal. Resistors R1, R2 and capacitor C2 limit the input bandwidth to approximately 100kHz.

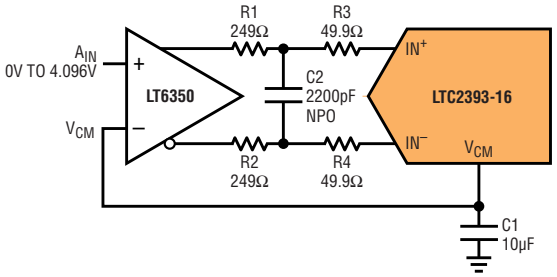

Figure 1. Single-ended to differential converter

When driving a low noise, low distortion ADC such as the LTC2393-16, component choice is essential for maintaining performance. All of the resistors used in this circuit are relatively low values. This keeps the noise and settling time low. Metal film resistors are recommended to reduce distortion caused by self-heating. An NPO capacitor is used for C2 because of its low voltage coefficient, which minimizes distortion. The excellent linearity characteristics of NPO and silver mica capacitors make these good choices for low distortion applications. Finally, the LT6350 features low noise, low distortion and a fast settling time.

The 16k-point FFT in Figure 2 shows the performance of the LTC2393-16 in the circuit of Figure 1. The measured SNR of 94dB and THD of –103dB match closely with the typical data sheet specs for the LTC2393-16, showing that little, if any, degradation of the ADC's specifications result from inserting the single-ended to differential converter into the signal path.

FULLY DIFFERENTIAL DRIVE

The circuit of Figure 3 AC-couples and level shifts the sensor output to match the common mode voltage of the ADC. The lower frequency limit of this circuit is about 10kHz. The lower frequency limit can be extended by increasing the values of C3 and C4. This circuit is useful for sensors with low impedance differential outputs.

The circuit of Figure 1 could be AC-coupled in a similar manner. Simply bias AIN to VCM through a 1k resistor and couple the signal to AIN through a 10µF capacitor.

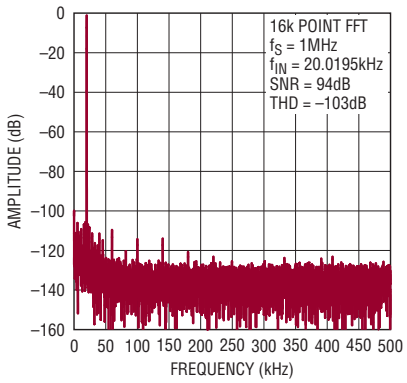

Figure 2. LTC2393-16 16k point FFT using circuit of Figure 1

The LTC2393-16 with its fully differential inputs can improve SNR by as much as 6dB over conventional differential input ADCs. This ADC is well suited for applications that require low distortion and a large dynamic range.

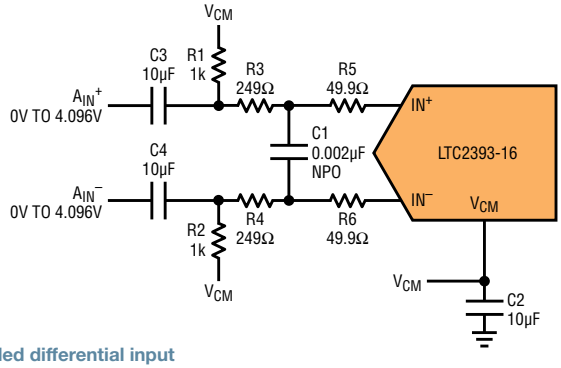

Figure 3. AC-coupled differential input

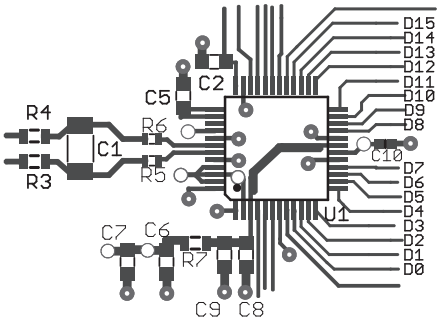

Figure 4. Sample layout for LTC2393-16

PCB LAYOUT

The circuits shown are quite simple in concept. However, when dealing with a high speed 16-bit ADC, PC board layout must also be considered. Always use a ground plane. Keep traces as short as possible. If a long trace is required for a bias node such as VCM, use additional bypass capacitors for each component attached to the node and make the trace as wide as possible. Keep bypass capacitors as close to the supply pins as possible. Each bypass capacitor should have its own low impedance return to ground. The analog input traces should be screened by ground. The layout involving the analog inputs should be as symmetrical as possible so that parasitic elements cancel each other out.

Figure 4 shows a sample layout for the LTC2393-16. Figure 4 is a composite of the top metal, ground plane and silkscreen layers. See the DC1500A Quick Start Guide at www.linear.com for a complete LTC2393-16 layout example.

CONCLUSION

The LTC2393-16 with its fully differential inputs can improve SNR by as much as 6dB over conventional differential input ADCs. This ADC is well suited for applications that require low distortion and a large dynamic range. Realizing the potential low noise, low distortion performance of the LTC2393-16 requires combining simple driver circuits with proper component selection and good layout practices. ■

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capacitors can be used, which would result in correspondingly slower rise/fall times.

The LT5579 upconverting mixer circuit shown in Figure 1 was optimized and tested at an RF output frequency of 2140MHz. The RF output envelope in Figure 2 shows a dip about 300ns after the V_{CC} switch turns on, followed by another, smaller dip at about the 500ns point. Both dips represent the mixer's internal feedback circuit reaction to the ramping supply voltage.

LO leakage to the RF output of the LT5579 was measured at –40dBm when V_{CC} is on and –46dBm for V_{CC} off. The LO port of the LT5579 is internally matched and has a return loss of 10dB to 18dB over a frequency range of 1100MHz to 3200MHz.

When the LT5579 mixer is in the off state, the return loss of the LO port is about 3dB to 5dB across the same frequency range of 1100MHz to 3200MHz. It is advisable to use an LO injection VCO with a buffered output for better reverse isolation, and to avoid any VCO pulling while the LO port impedance changes when switching between the on and off states.

CONCLUSION

LT5579 and LT5578 mixers without an ENABLE pin can be used in TDD applications with external V_{CC} switching. Using only three parts (IRLML6401, 2N7002 and an MC74HC1G04), a high performance high side V_{CC} switch allows turn-on and turn-off in under 1µs. ■