Description

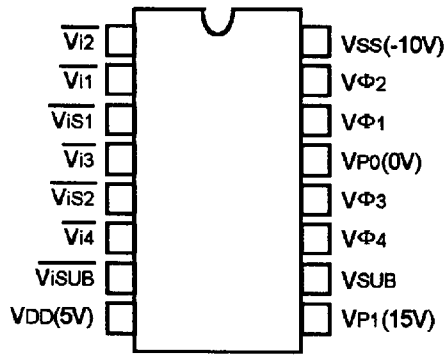
The GCD1001S is a clock driver for the vertical resister drive of CCD.

GCD1001S is well suited for the B/W or color CCD camera/camcorder in NTSC or PAL system.

Feature

- 4 channel vertical clock driver and 1 channel substrate driver.
- Implemented with high voltage(50V) and high performance CMOS process.

Pin Configuration



16SSOP

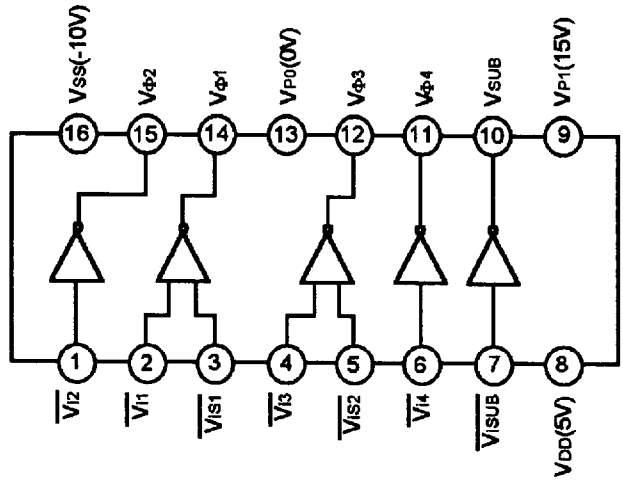
Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{SS} V_{DD}, V_{P0}, V_{P1}	Reference voltage Vss-0.3 to Vss+35	V V
Input voltage	V_I	Vss-0.3 to V_{DD}+0.3	V
Output voltage	V_{02}, V_{04} V_{01}, T_{03}, T_{Sub}	Vss-0.3 toVP0+0.3 Vss-0.3 toVP1+0.3	V V
Operating temperature	T_{OPR}	-25 to +85	℃
Storage temperature	T_{STG}	-40 to +125	℃

Recommended Operatng Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD VP0 VP1	Vss +15 Vss +10 Vss +25	V V V
Operating temperature	T_{OPR}	-20 to +75	℃

Block Diagram and Pin Configuration (Top View)



Truth Table

Input				Output		
$\overline{Vi1,3}$	$\overline{ViS1,2}$	$\overline{Vi2,4}$	$\overline{Visub}$	V01,3	V02,4	Vsub
L L H H	L H L H			VP1 VP0 *Z VSS		
		L H			VP0 VSS	
			L H			VP1 VSS

*Z is high impedance.

DC Characteristics (T_A=25℃, V_{DD}=5V, VSS=-10V, VP0=0V, VP1=15V)

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Input high voltage	V_{IP1}		3.5			V
Input low voltage	V_{ISS}				1.5	V
Output high voltage	$V_{ΦP1}$	$I_{ΦP1}$ = - 20 μA	14.9	15		V
Output middle voltage	$V_{ΦP0}$	$I_{ΦP0}$ = - 20 μA		0	0.1	V
Output middle voltage	$V_{ΦP0}$	$I_{ΦP0}$ = 20 μA	-0.1	0		V
Output low voltage	$V_{ΦSS}$	$I_{ΦSS}$= 20 μA		-10	-9.9	V
Input current	I_{IN}			1.0		μA
Power supply current	I_{P0}			0.3	0.5	mA
Power supply current	I_{PI}			0.15	0.3	mA
Power supply current	I_{P0}			4.5	5.0	mA

Pin Description

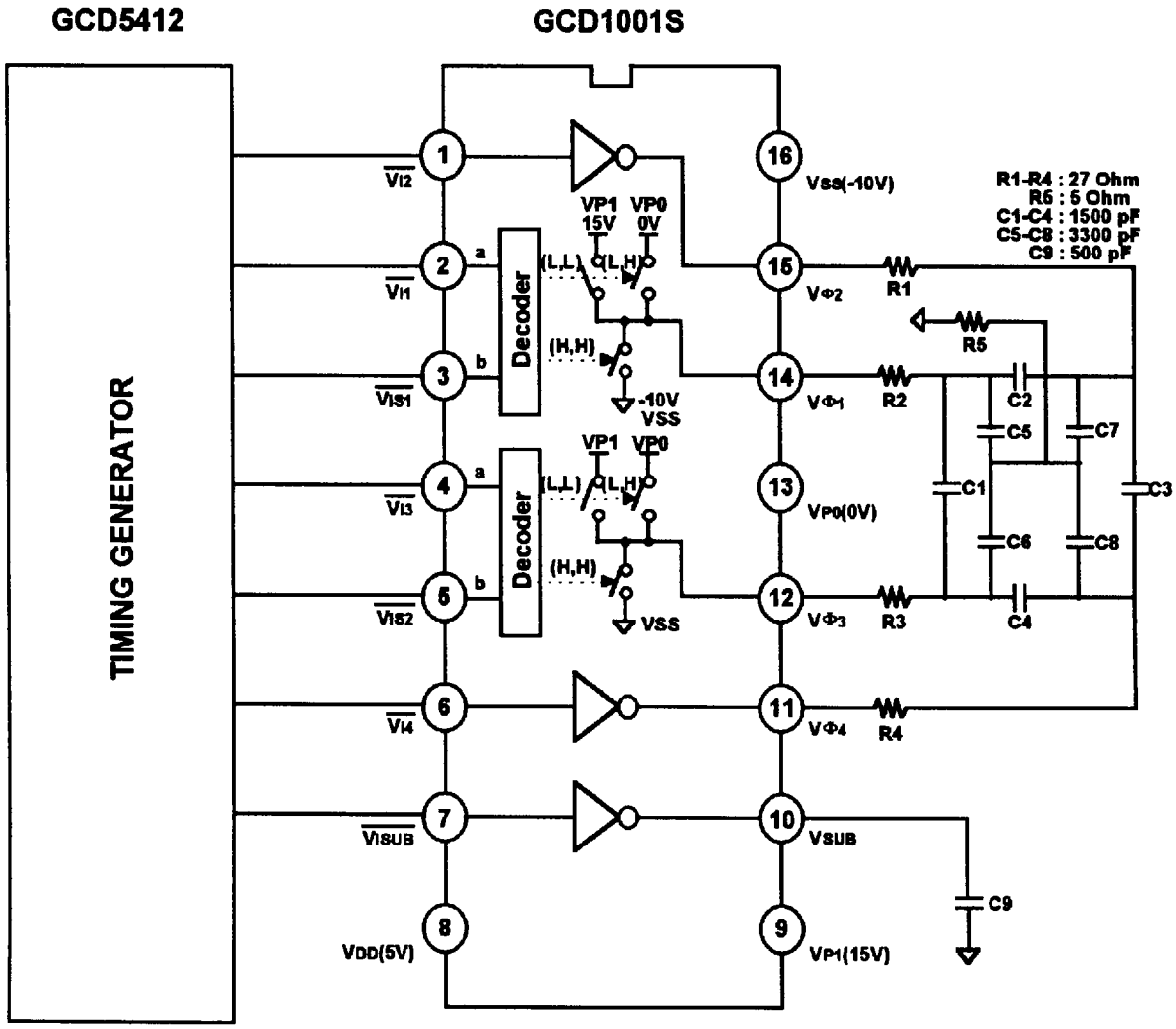
No.	Symbol	I/O	Description
1	$\overline{Vi2}$	I	Output control (V02)
2	$\overline{Vi1}$	I	Output control (V01)
3	$\overline{ViS1}$	I	Output control (V01)
4	$\overline{Vi3}$	I	Output control (V03)
5	$\overline{ViS2}$	I	Output control (V03)
6	$\overline{Vi4}$	I	Output control (V04)
7	$\overline{ViSUB}$	I	Output control (VSub)
8	V_{DD}	-	Power supply (5V)
9	V_{P1}	-	Power supply (15V)
10	V_{SUB}	O	Output (2 level : VP1, VSS)
11	$V\Phi_4$	O	Output (2 level : VP0, VSS)
12	$V\Phi_3$	O	Output (3 level : VP1, VP0, VSS)
13	V_{P0}	-	Power supply (0V)
14	$V\Phi_1$	O	Output (3 level : VP1, VP0, VSS)
15	$V\Phi_2$	O	Output (2 level : VP0, VSS)
16	V_{SS}	-	Power supply (-10V)

Switching Characteristics

(See the Test Circuit T_A = 25℃, VP1=15V, VP0=0V, V_{DD}=5V, VSS=-10V)

Item	Symbol	Conditions	Max.	Min.	Unit
Output Current	I_L	V01 to 4 = -9.5V	-25		mA
Output Current	I_{M1}	V01 to 4 = -0.5V		10	mA
Output Current	I_{M2}	V01, 3= 0.5V	-9		mA
Output Current	I_H	V01, 3 = 14.5V		12	mA
Output Current	I_{SL}	VSub = -9.5V	-12		mA
Output Current	I	VSub = 14.5V		12	mA
Rise time VSS → VP0	T_{TLM}	V01 to 4 = -0.5V After input transient	1000		ns
Fall time VP0 → VSS	T_{TML}	V01, 3= -9.5V After input transient	1000		ns
Rise time VP0 → VP1	T_{TMH}	V01, 3 = 14V After input transient	1000		ns
Fall time VP1 → VP0	T_{THM}	V01, 3= 1V After input transient	1000		ns
Rise time VP0 → VP1	T_{TLHH}	VSub= 14V	200		ns
Fall time Vp1 → VSS	T_{THHL}	VSub = -9.5V	200		ns
Coupling amplitude (millde level)	V_{COM}	V01 to 4	0.5		V
Coupling amplitude (low level)	V_{COL}	V01 to 4	0.5		V

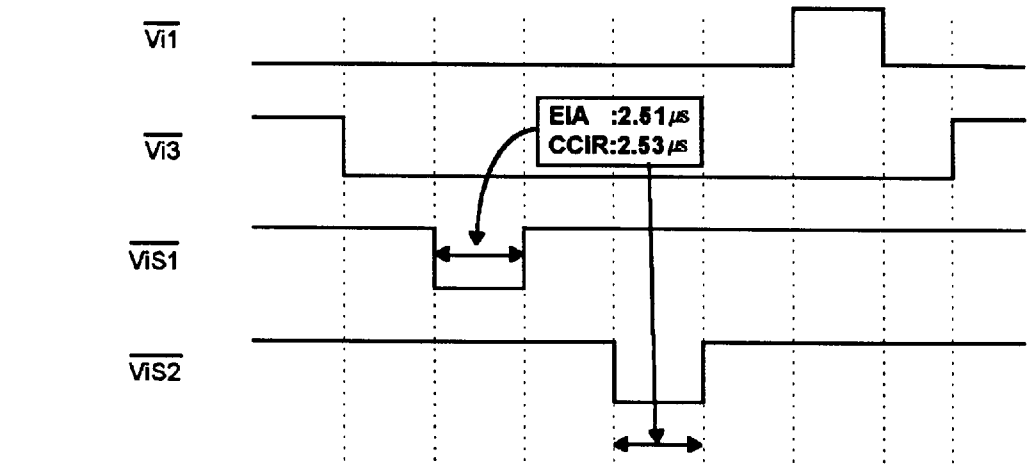
Test Circuit



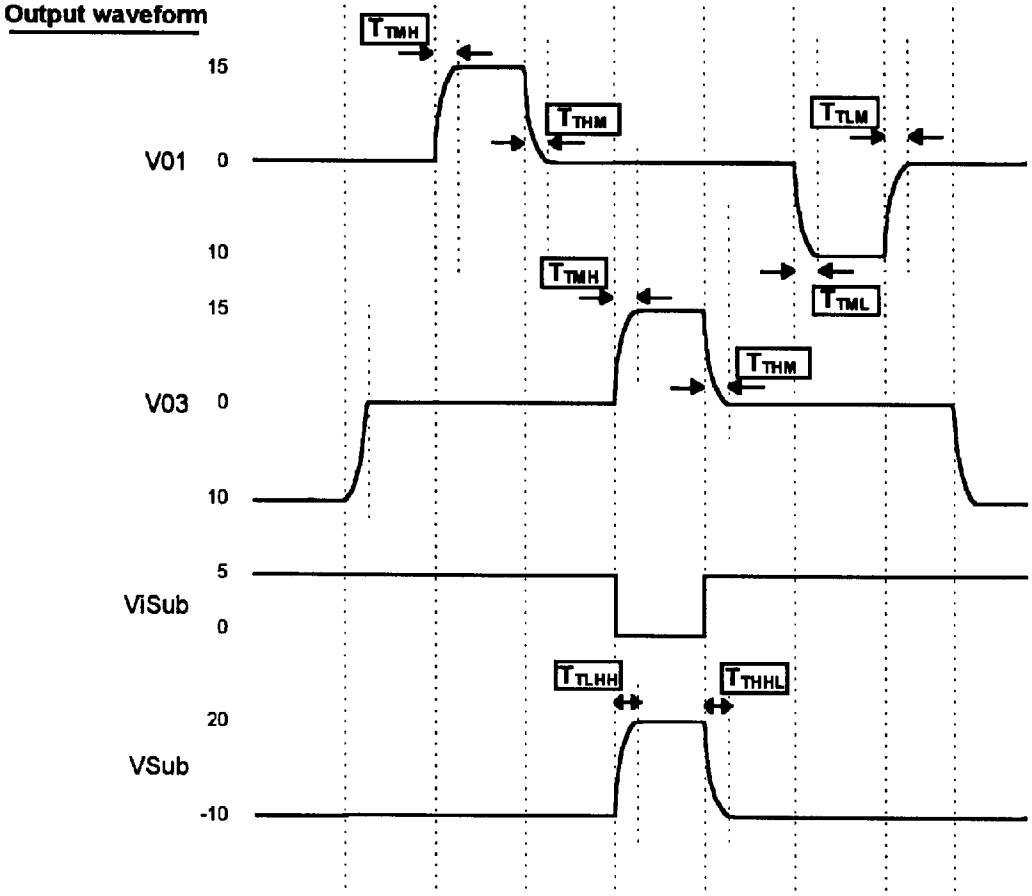
*(L, H) means the on-status of the switch when a = "L", b = "H".

Test Circuit I/O Waveform Diagram

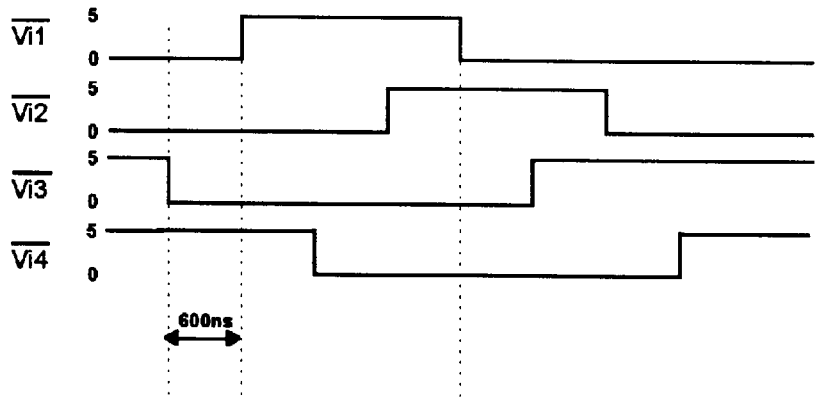
Input waveform



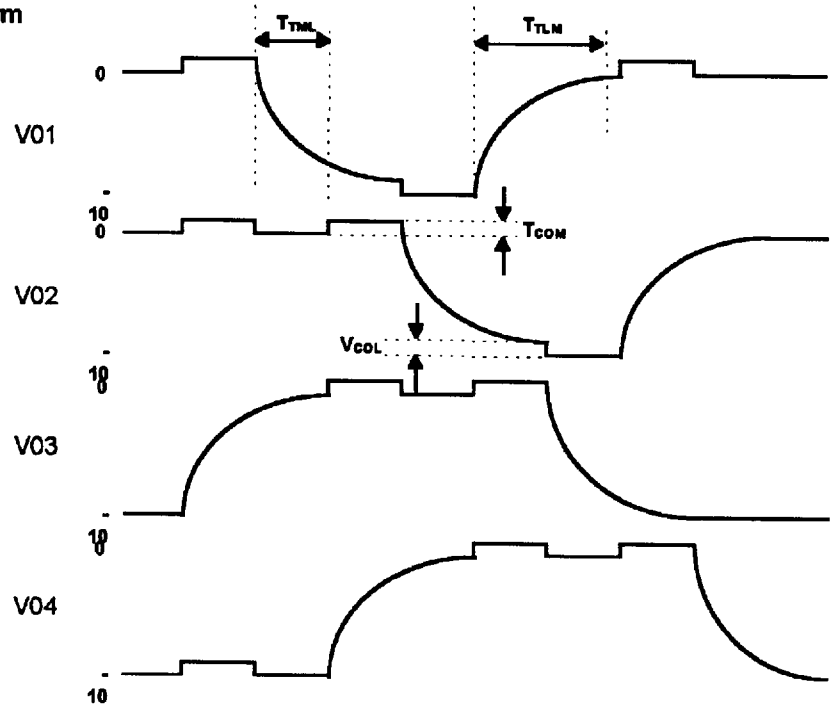
Output waveform



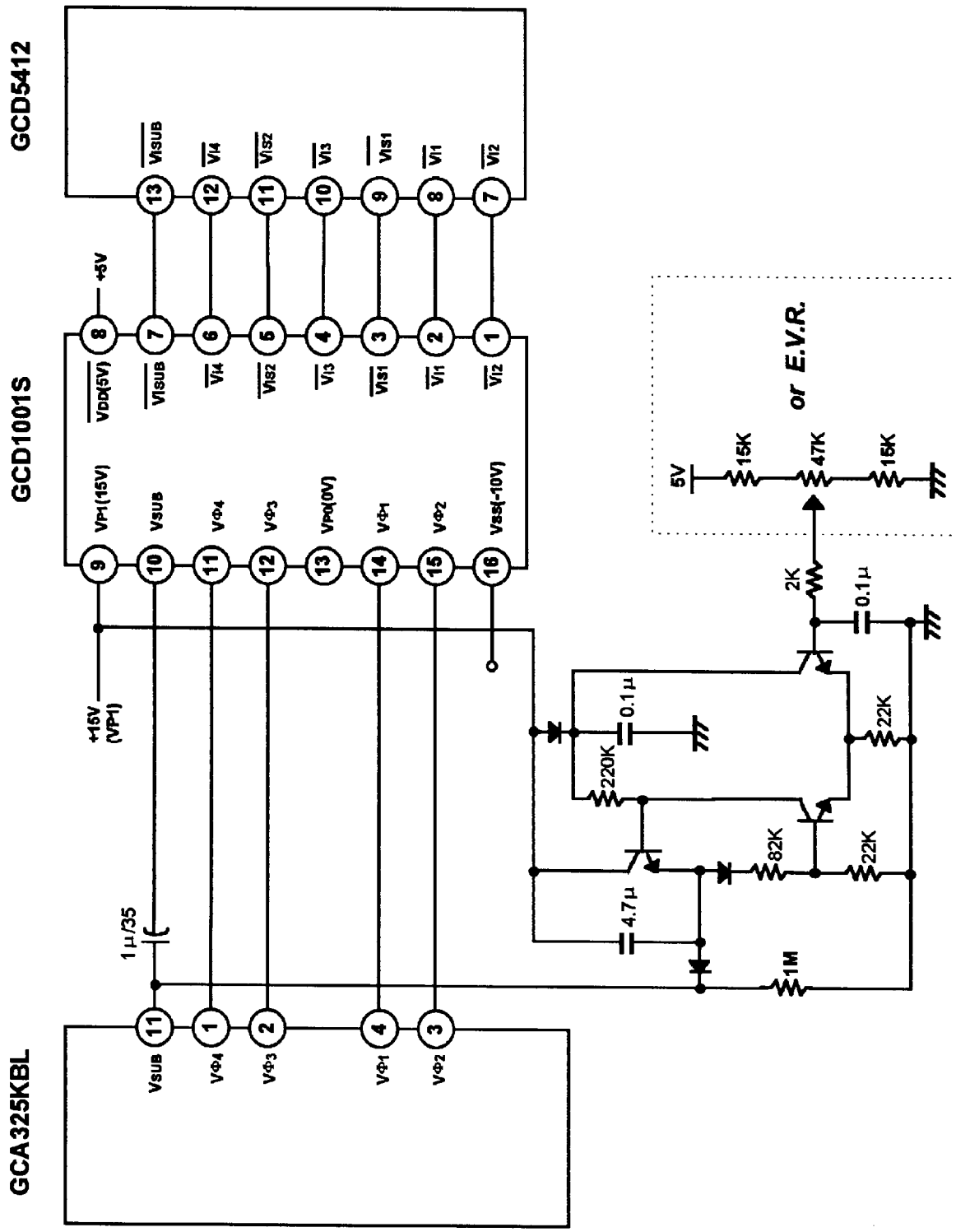
Input waveform
(Receat Cycle 15.7kHz)



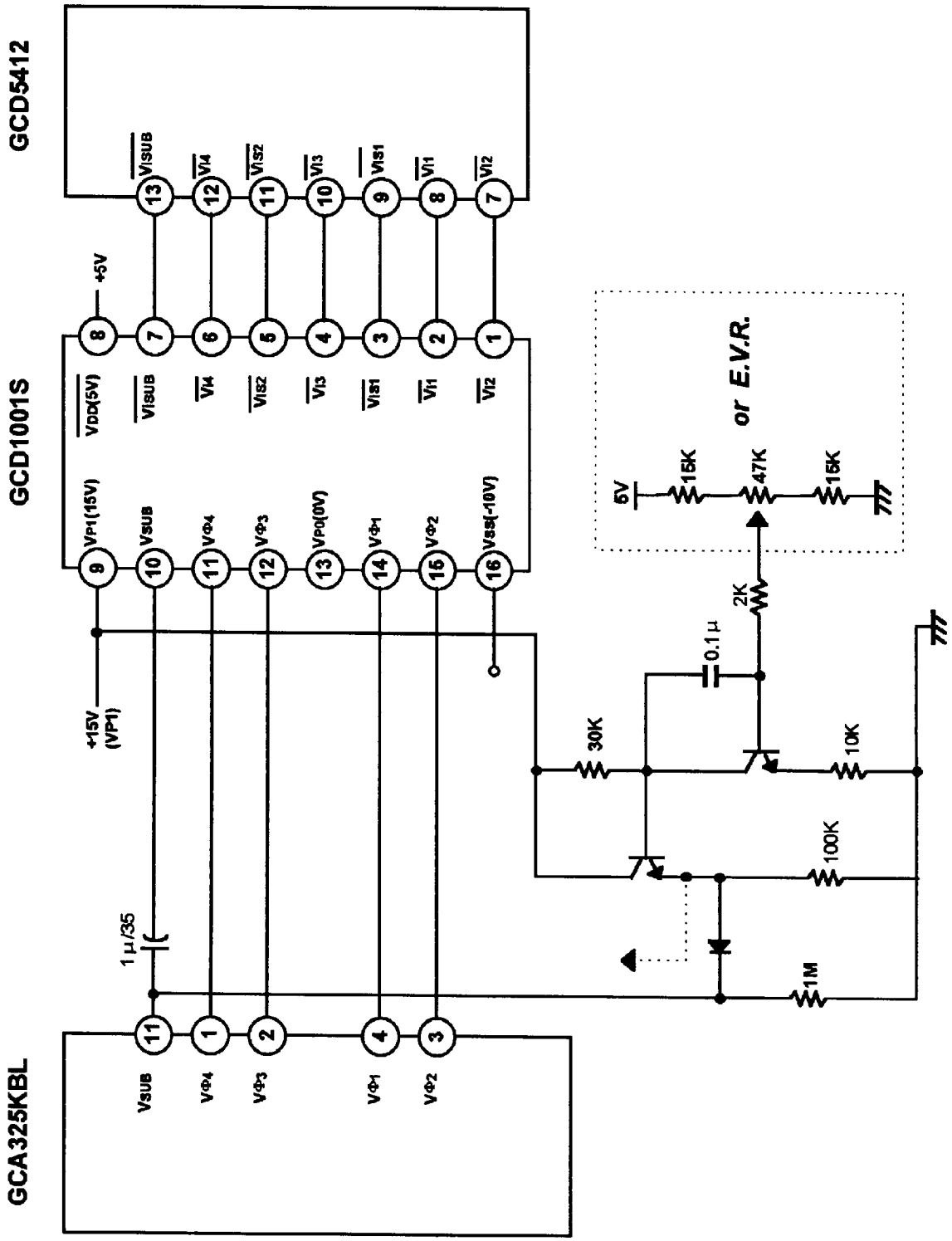
Output waveform



Application Circuit I



Application Circuit II



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Unit: inches(mm)