

ICPL4502



HIGH SPEED, NON BASE LEAD OPTICALLY COUPLED ISOLATOR PHOTOTRANSISTOR OUTPUT

APPROVALS

- UL recognised, File No. E91231

DESCRIPTION

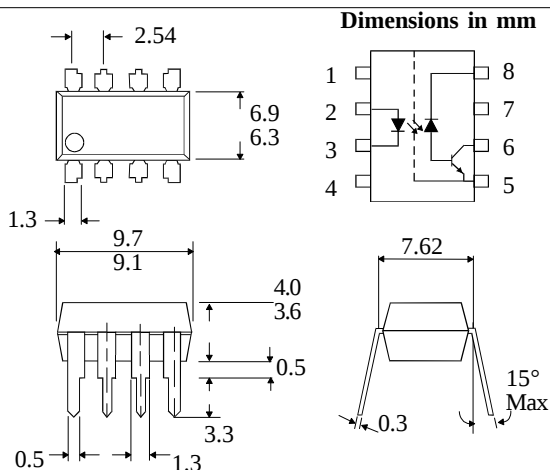
These diode-transistor optocouplers use a light emitting diode and an integrated photon detector to provide 2500Volts_{RMS} electrical isolation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

FEATURES

- High speed - 1 MBits/s
- High Common Mode Transient Immunity 10000V/μs typical
- Pin 7 not connected to give enhanced Noise Immunity
- TTL Compatible
- 2 MHz Bandwidth
- Open Collector Output
- 2500V_{RMS} Withstand Test Voltage, 1 Min
- Options :-
10mm lead spread - add G after part no.
Surface mount - add SM after part no.
Tape&reel - add SMT&R after part no.
- All electrical parameters 100% tested
- Custom electrical selections available

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Wide bandwidth analog coupling
- Output interface to CMOS-LSTTL-TTL



ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise specified)

Storage Temperature _____ -55°C to + 125°C
Operating Temperature _____ -55°C to + 100°C
Lead Soldering Temperature
(1/16 inch (1.6mm) from case for 10 secs) 260°C

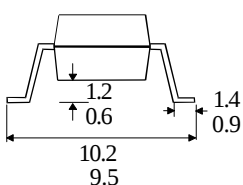
INPUT DIODE

Average Forward Current _____ 25mA (1)
Peak Forward Current _____ 50mA (2)
(50% duty cycle, 1ms pulse width)
Peak Transient Current _____ 1.0A
(equal to or less than 1μs P.W., 300 pps)
Reverse Voltage _____ 5V
Power Dissipation _____ 45mW (3)

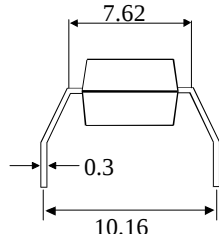
DETECTOR

Average Output Current _____ 8mA
Peak Output Current _____ 16mA
Supply and Output Voltage _____ -0.5 to +15V
Power Dissipation _____ 100mW (4)

OPTION SM SURFACE MOUNT



OPTION G



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ELECTRICAL CHARACTERISTICS ($T_A = 0^{\circ}\text{C}$ to 70°C Unless otherwise noted)

PARAMETER	SYM		MIN	TYP*	MAX	UNITS	TEST CONDITION
Current Transfer Ratio (note 5)	CTR		19	24		%	$I_F = 16\text{mA}$, $V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$, $T_A = 25^{\circ}\text{C}$
			15	25		%	$I_F = 16\text{mA}$, $V_O = 0.5\text{V}$ $V_{CC} = 4.5\text{V}$
Logic Low Output Voltage	V_{OL}			0.1	0.4	V	$I_F = 16\text{mA}$, $I_O = 2.4\text{mA}$ $V_{CC} = 4.5\text{V}$, $T_A = 25^{\circ}\text{C}$
Logic High Output Current	I_{OH}			0.02	500	nA	$I_F = 0\text{mA}$, $T_A = 25^{\circ}\text{C}$ $V_O = V_{CC} = 5.5\text{V}$
				0.01	1	μA	$I_F = 0\text{mA}$, $T_A = 25^{\circ}\text{C}$ $V_O = V_{CC} = 15\text{V}$
					50	μA	$I_F = 0\text{mA}$ $V_O = V_{CC} = 15\text{V}$
Logic Low Supply Current	I_{CCL}				40	μA	$I_F = 16\text{mA}$, $V_O = \text{open}$ $V_{CC} = 15\text{V}$
Logic High Supply Current	I_{CCH}			0.02	1	μA	$I_F = 0\text{mA}$, $V_O = \text{open}$ $V_{CC} = 15\text{V}$, $T_A = 25^{\circ}\text{C}$
					2	μA	$I_F = 0\text{mA}$, $V_O = \text{open}$ $V_{CC} = 15\text{V}$
Input Forward Voltage	V_F			1.5	1.7	V	$I_F = 16\text{mA}$, $T_A = 25^{\circ}\text{C}$
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/ $^{\circ}\text{C}$	$I_F = 16\text{mA}$
Input Reverse Voltage	V_R		5			V	$I_R = 10\mu\text{A}$, $T_A = 25^{\circ}\text{C}$
Input Capacitance	C_{IN}			60		pF	$f = 1\text{MHz}$, $V_F = 0$
Input-output Isolation Voltage	V_{ISO}		2500	5000		V_{RMS}	R.H.equal to or less than 50%, $t = 1\text{min}$. $T_A = 25^{\circ}\text{C}$
Resistance (Input to Output)	R_{IO}			10^{12}		Ω	$V_{IO} = 500\text{V}$ dc (note 6)
Capacitance (Input to Output)	C_{IO}			0.6		pF	$f = 1\text{MHz}$ (note 6)
Transistor DC Current Gain	H_{FE}			150			$V_O = 5\text{V}$, $I_O = 3\text{mA}$

* All typicals at $T_A = 25^{\circ}\text{C}$

SWITCHING SPECIFICATIONS AT $T_A = 25^\circ\text{C}$ ($V_{CC} = 5\text{V}$, $I_F = 16\text{mA}$ Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time To Logic Low at Output (fig 1)	t_{PHL}			0.2	0.8	μs	$R_L = 1.9\text{k}\Omega$, (note 8)
Propagation Delay Time To Logic High at Output (fig 1)	t_{PLH}			0.2	0.8	μs	$R_L = 1.9\text{k}\Omega$, (note 8)
Common Mode Transient Immunity at Logic High Level Output (fig 2)	CM_H			10000		$\text{V}/\mu\text{s}$	$I_F = 0\text{mA}$, $V_{CM} = 10V_{PP}$ $R_L = 1.9\text{k}\Omega$, (note 7,8)
Common Mode Transient Immunity at Logic Low Level Output (fig 2)	CM_L			-10000		$\text{V}/\mu\text{s}$	$V_{CM} = 10V_{PP}$ $R_L = 1.9\text{k}\Omega$, (note 7,8)
Bandwidth	BW			2		MHz	$R_L = 100\Omega$, (note 9)

NOTES:-

1. Derate linearly above 70°C free air temperature at a rate of $0.8 \text{ mA}/^\circ\text{C}$.
2. Derate linearly above 70°C free air temperature at a rate of $1.6 \text{ mA}/^\circ\text{C}$.
3. Derate linearly above 70°C free air temperature at a rate of $0.9 \text{ mW}/^\circ\text{C}$.
4. Derate linearly above 70°C free air temperature at a rate of $1.0 \text{ mW}/^\circ\text{C}$.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100%.
6. Device considered a two-terminal device: pins 1,2,3, and 4 shorted together and pins 5,6,7 and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM} to assure that the output will remain in a Logic High state (i.e. $V_O > 2.0\text{V}$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} to assure that the output will remain in Logic Low state (i.e. $V_O < 0.8\text{V}$).
8. The $1.9\text{k}\Omega$ load represents 1 TTL unit load of 1.6mA and the $5.6\text{k}\Omega$ pull-up resistor.
9. The frequency at which the a.c. output voltage is 3dB below the low frequency asymptote.

FIG.1 SWITCHING TEST CIRCUIT

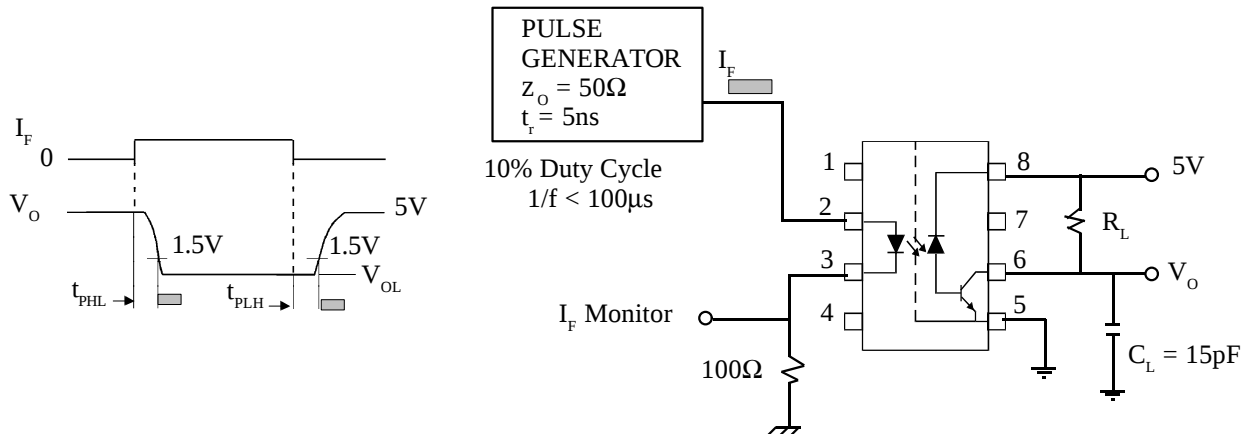


FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS

