X9317

Low Noise, Low Power, 100 Taps

Data Sheet | September 9, 2005 | FN8183.1

Digitally Controlled Potentiometer (XDCP™)

The Intersil X9317 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer for voltage control or as a two-terminal variable resistor for current control in a wide variety of applications.

Features

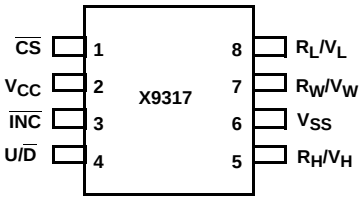
- Solid-State Potentiometer
- 3-Wire Serial Up/Down Interface
- 100 Wiper Tap Points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 99 Resistive Elements
  - Temperature compensated
  - End to end resistance range ±20%
- Low Power CMOS
  - V_{CC} = 2.7V to 5.5V, and 5V ±10%
  - Standby current < 1µA
- High Reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} Values = 1kΩ, 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, DIP, TSSOP, and MSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

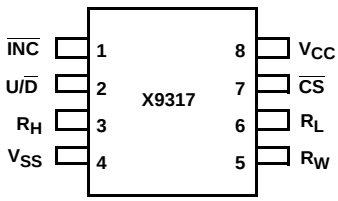
- LCD Bias Control
- DC Bias Adjustment
- Gain and Offset Trim
- Laser Diode Bias Control
- Voltage Regulator Output Control

Pinouts

X9317
(8 LD TSSOP)
TOP VIEW



X9317
(8 LD DIP, 8 LD SOIC, 8 LD MSOP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE
X9317ZM8*		5 ±10%	1	0 to 70	8 Ld MSOP
X9317ZM8Z* (Note)	DDA			0 to 70	8 Ld MSOP (Pb-free)
X9317ZM8I*	AFI			-40 to 85	8 Ld MSOP
X9317ZM8IZ* (Note)	DCY			-40 to 85	8 Ld MSOP (Pb-free)
X9317ZP	X9317ZP			0 to 70	8 Ld PDIP
X9317ZS8*	X9317Z			0 to 70	8 Ld SOIC
X9317ZS8Z* (Note)	X9317Z Z			0 to 70	8 Ld SOIC (Pb-free)
X9317ZS8I*	X9317Z I			-40 to 85	8 Ld SOIC
X9317ZS8IZ* (Note)	X9317Z Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9317ZV8*	9317Z			0 to 70	8 Ld TSSOP
X9317ZV8Z* (Note)	9317Z Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317ZV8I*	317ZI			-40 to 85	8 Ld TSSOP
X9317ZV8IZ* (Note)	9317ZI Z			-40 to 85	8 Ld TSSOP (Pb-free)
X9317WM8*	ABF		10	0 to 70	8 Ld MSOP
X9317WM8Z* (Note)	DCW			0 to 70	8 Ld MSOP (Pb-free)
X9317WM8I*	ADS			-40 to 85	8 Ld MSOP
X9317WM8IZ* (Note)	DCT			-40 to 85	8 Ld MSOP (Pb-free)
X9317WP	X9317WP			0 to 70	8 Ld PDIP
X9317WPI	X9317WP I			-40 to 85	8 Ld PDIP
X9317WS8*	X9317W			0 to 70	8 Ld SOIC
X9317WS8Z* (Note)	X9317W Z			0 to 70	8 Ld SOIC (Pb-free)
X9317WS8I*	X9317W I			-40 to 85	8 Ld SOIC
X9317WS8IZ* (Note)	X9317W Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9317WV8*	9317W			0 to 70	8 Ld TSSOP
X9317WV8Z* (Note)	9317W Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317WV8I*	317WI			-40 to 85	8 Ld TSSOP
X9317WV8IZ* (Note)	9317WI Z			-40 to 85	8 Ld TSSOP (Pb-free)
X9317UM8*	AEC		50	0 to 70	8 Ld MSOP
X9317UM8Z* (Note)	DCS			0 to 70	8 Ld MSOP (Pb-free)
X9317UM8I*	AFE			-40 to 85	8 Ld MSOP
X9317UM8IZ* (Note)	DCR			-40 to 85	8 Ld MSOP (Pb-free)
X9317UP	X9317UP			0 to 70	8 Ld PDIP
X9317UPI	X9317UP I			-40 to 85	8 Ld PDIP
X9317US				0 to 70	8 Ld SOIC
X9317US8*	X9317U			0 to 70	8 Ld SOIC
X9317US8Z* (Note)	X9317U Z			0 to 70	8 Ld SOIC (Pb-free)
X9317US8I*	X9317U I			-40 to 85	8 Ld SOIC
X9317US8IZ* (Note)	X9317U Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9317UV8*	9317U			0 to 70	8 Ld TSSOP
X9317UV8Z* (Note)	9317U Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317UV8I*	317UI			-40 to 85	8 Ld TSSOP
X9317UV8IZ* (Note)	9317UI Z			-40 to 85	8 Ld TSSOP (Pb-free)

Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE
X9317TM8*	AGD		100	0 to 70	8 Ld MSOP
X9317TM8Z* (Note)	DCN			0 to 70	8 Ld MSOP (Pb-free)
X9317TM8I*	AGF			-40 to 85	8 Ld MSOP
X9317TM8IZ* (Note)	DCL			-40 to 85	8 Ld MSOP (Pb-free)
X9317TP				0 to 70	8 Ld PDIP
X9317TPI	X9317TP I			-40 to 85	8 Ld PDIP
X9317TS8	X9317T			0 to 70	8 Ld SOIC
X9317TS8Z (Note)	X9317T Z			0 to 70	8 Ld SOIC (Pb-free)
X9317TS8I	X9317T I			-40 to 85	8 Ld SOIC
X9317TS8IZ (Note)	X9317T Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9317TV8*				0 to 70	8 Ld TSSOP
X9317TV8Z* (Note)	9317T Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317TV8I*				-40 to 85	8 Ld TSSOP
X9317TV8IZ* (Note)	9317TI Z			-40 to 85	8 Ld TSSOP (Pb-free)
X9317ZM8-2.7*	AFH	2.7-5.5	1	0 to 70	8 Ld MSOP
X9317ZM8Z-2.7* (Note)	AOA			0 to 70	8 Ld MSOP (Pb-free)
X9317ZM8I-2.7*	AFJ			-40 to 85	8 Ld MSOP
X9317ZM8IZ-2.7* (Note)	DCZ			-40 to 85	8 Ld MSOP (Pb-free)
X9317ZS8-2.7*	X9317Z F			0 to 70	8 Ld SOIC
X9317ZS8Z-2.7* (Note)	X9317Z Z F			0 to 70	8 Ld SOIC (Pb-free)
X9317ZS8I-2.7*	X9317Z G			-40 to 85	8 Ld SOIC
X9317ZS8IZ-2.7* (Note)	X9317Z Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9317ZV8-2.7*	317ZF			0 to 70	8 Ld TSSOP
X9317ZV8Z-2.7* (Note)	9317ZF Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317ZV8I-2.7*	317ZG			-40 to 85	8 Ld TSSOP
X9317ZV8IZ-2.7* (Note)	317ZG Z			-40 to 85	8 Ld TSSOP (Pb-free)
X9317WM8-2.7*	ACZ		10	0 to 70	8 Ld MSOP
X9317WM8Z-2.7* (Note)	DCX			0 to 70	8 Ld MSOP (Pb-free)
X9317WM8I-2.7*	ADT			-40 to 85	8 Ld MSOP
X9317WP-2.7	X9317WP F			0 to 70	8 Ld PDIP
X9317WPI-2.7	X9317WP G			-40 to 85	8 Ld PDIP
X9317WS8-2.7*	X9317W F			0 to 70	8 Ld SOIC
X9317WS8Z-2.7* (Note)	X9317W Z F			0 to 70	8 Ld SOIC (Pb-free)
X9317WS8I-2.7*	X9317W G			-40 to 85	8 Ld SOIC
X9317WS8IZ-2.7* (Note)	X9317W Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9317WV8-2.7*	317WF			0 to 70	8 Ld TSSOP
X9317WV8Z-2.7* (Note)	9317WF Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317WV8I-2.7*	317WG			-40 to 85	8 Ld TSSOP
X9317WV8IZ-2.7* (Note)	AKZ			-40 to 85	8 Ld TSSOP (Pb-free)

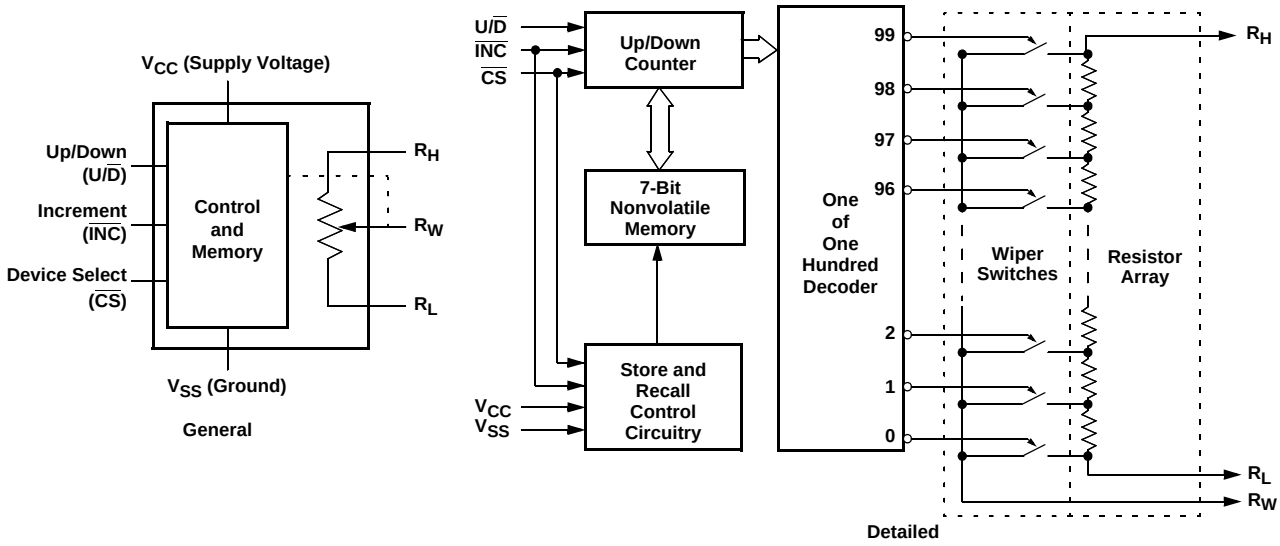
Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE
X9317UM8-2.7*	AED		50	0 to 70	8 Ld MSOP
X9317UM8Z-2.7* (Note)	AOB			0 to 70	8 Ld MSOP (Pb-free)
X9317UM8I-2.7*	AFF			-40 to 85	8 Ld MSOP
X9317UM8IZ-2.7* (Note)	AOH			-40 to 85	8 Ld MSOP (Pb-free)
X9317UP-2.7	X9317UP F			0 to 70	8 Ld PDIP
X9317UPI-2.7	X9317UP G			-40 to 85	8 Ld PDIP
X9317US8-2.7*	X9317U F			0 to 70	8 Ld SOIC
X9317US8Z-2.7* (Note)	X9317U Z F			0 to 70	8 Ld SOIC (Pb-free)
X9317US8I-2.7*	X9317U G			-40 to 85	8 Ld SOIC
X9317US8IZ-2.7* (Note)	X9317U Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9317UV8-2.7*	9317UF			0 to 70	8 Ld TSSOP
X9317UV8Z-2.7* (Note)	9317UF Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317UV8I-2.7*	9317UG			-40 to 85	8 Ld TSSOP
X9317UV8IZ-2.7* (Note)	9317UG Z			-40 to 85	8 Ld TSSOP (Pb-free)
X9317TM8-2.7*	AGE		100	0 to 70	8 Ld MSOP
X9317TM8Z-2.7* (Note)	DCP			0 to 70	8 Ld MSOP (Pb-free)
X9317TM8I-2.7*	AGG			-40 to 85	8 Ld MSOP
X9317TM8IZ-2.7* (Note)	DCM			-40 to 85	8 Ld MSOP (Pb-free)
X9317TP-2.7				0 to 70	8 Ld PDIP
X9317TPI-2.7	X9317TP G			-40 to 85	8 Ld PDIP
X9317TS8-2.7*				0 to 70	8 Ld SOIC
X9317TS8Z-2.7* (Note)	X9317T Z F			0 to 70	8 Ld SOIC (Pb-free)
X9317TS8I-2.7*	X9317T G			-40 to 85	8 Ld SOIC
X9317TS8IZ-2.7* (Note)	X9317T Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9317TV8-2.7*				0 to 70	8 Ld TSSOP
X9317TV8Z-2.7* (Note)	9317TF Z			0 to 70	8 Ld TSSOP (Pb-free)
X9317TV8I-2.7*	317TG			-40 to 85	8 Ld TSSOP
X9317TV8IZ-2.7* (Note)	9317TG Z			-40 to 85	8 Ld TSSOP (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add "T1" suffix for tape and reel.

Block Diagram



Pin Descriptions

DIP/SOIC	SYMBOL	BRIEF DESCRIPTION
1	$\overline{INC}$	**Increment**. Toggling $\overline{INC}$ while $\overline{CS}$ is low moves the wiper either up or down.
2	$U/\overline{D}$	**Up/Down**. The $U/\overline{D}$ input controls the direction of the wiper movement.
3	R_H	The high terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
4	V_{SS}	**Ground.**
5	R_W	The wiper terminal is equivalent to the movable terminal of a mechanical potentiometer.
6	R_L	The low terminal is equivalent to one of the fixed terminals of a mechanical potentiometer.
7	$\overline{CS}$	**Chip Select**. The device is selected when the $\overline{CS}$ input is LOW, and de-selected when $\overline{CS}$ is high.
8	V_{CC}	**Supply Voltage.**

Absolute Maximum Ratings

Junction Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC} with Respect to V_{SS} . . . . . -1V to +7V
R_H, R_W, R_L to Ground . . . . . .+6V
Lead Temperature (soldering 10s). . . . . .300°C
I_W (10s) . . . . . .±8.8mA

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Potentiometer Specifications

V_{CC} = Full Range, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	TYP (Note 4)	MAX	UNIT
R_{TOTAL}	End to end resistance tolerance	See ordering information for values	-20		+20	%
$V_{RH}/_{RL}$	R_H/R_L terminal voltage	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Power rating	$R_{TOTAL} \geq 10k\Omega$			10	mW
		R_{TOTAL} = 1kΩ			25	mW
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 5V		200	400	Ω
		I_W = 1mA, V_{CC} = 2.7V		400	1000	Ω
I_W	Wiper current (Note 5)	See test circuit	-4.4		+4.4	mA
	Noise (Note 7)	Ref: 1kHz		-120		dBV
	Resolution			1		%
	Absolute linearity (Note 1)	V(RH) = V_{CC}, V(RL) = 0V	-1		+1	MI (Note 3)
	Relative linearity (Note 2)		-0.2		+0.2	MI (Note 3)
	R_{TOTAL} temperature coefficient (Note 5)			±300		ppm/°C
	Ratiometric temperature coefficient (Notes 5, 6)		-20		+20	ppm/°C
$C_H/C_L/C_W$ (Note 5)	Potentiometer capacitances	See equivalent circuit		10/10/25		pF
V_{CC}	Supply Voltage	X9317	4.5		5.5	V
		X9317-2.7	2.7		5.5	V

DC Electrical Specifications

V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNIT
I_{CC1}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL}/V_{IH} @ min. t_{CYC} R_L, R_H, R_W not connected			50	µA
I_{CC2}	V_{CC} active current (Store) (non-volatile write)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL} or V_{IH}. R_L, R_H, R_W not connected			400	µA
I_{SB}	Standby supply current	$\overline{CS} \geq V_{IH}$, U/$\overline{D}$ and $\overline{INC}$ = V_{IL} R_L, R_H, R_W not connected			1	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}	-10		+10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-0.5		V_{CC} x 0.1	V

DC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNIT
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz			10	pF

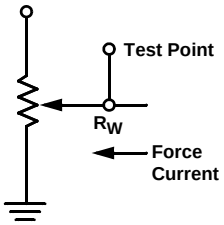
Endurance and Data Retention V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

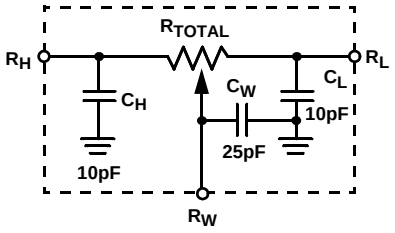
NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $[V(R_{W(n)(actual)})-V(R_{W(n)(expected)})]/MI$ $V(R_{W(n)(expected)}) = n(V(R_H)-V(R_L))/99 + V(R_L)$, with n from 0 to 99.
2. Relative linearity is a measure of the error in step size between taps = $[V(R_{W(n+1)})-(V(R_{W(n)}) - MI)]/MI$.
3. 1 MI = Minimum Increment = $[V(R_H)-V(R_L)]/99$.
4. Typical values are for T_A = 25°C and nominal supply voltage.
5. This parameter is not 100% tested.
6. Ratiometric temperature coefficient = $(V(R_W)_{T1(n)}-V(R_W)_{T2(n)})/[V(R_W)_{T1(n)}(T1-T2) \times 10^6]$, with T1 & T2 being 2 temperatures, and n from 0 to 99.
7. Measured with wiper at tap position 99, R_L grounded, using test circuit.

Test Circuit



Equivalent Circuit



AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	50			ns
t_{ID} (Note 5)	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI} (Note 5)	U/$\overline{D}$ to $\overline{INC}$ setup	1			µs
t_{IL}	$\overline{INC}$ LOW period	960			ns
t_{IH}	$\overline{INC}$ HIGH period	960			ns
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPHS}	$\overline{CS}$ deselect time (STORE)	10			ms
t_{CPHNS} (Note 5)	$\overline{CS}$ deselect time (NO STORE)	100			ns
t_{IW}	$\overline{INC}$ to R_W change		1	5	µs

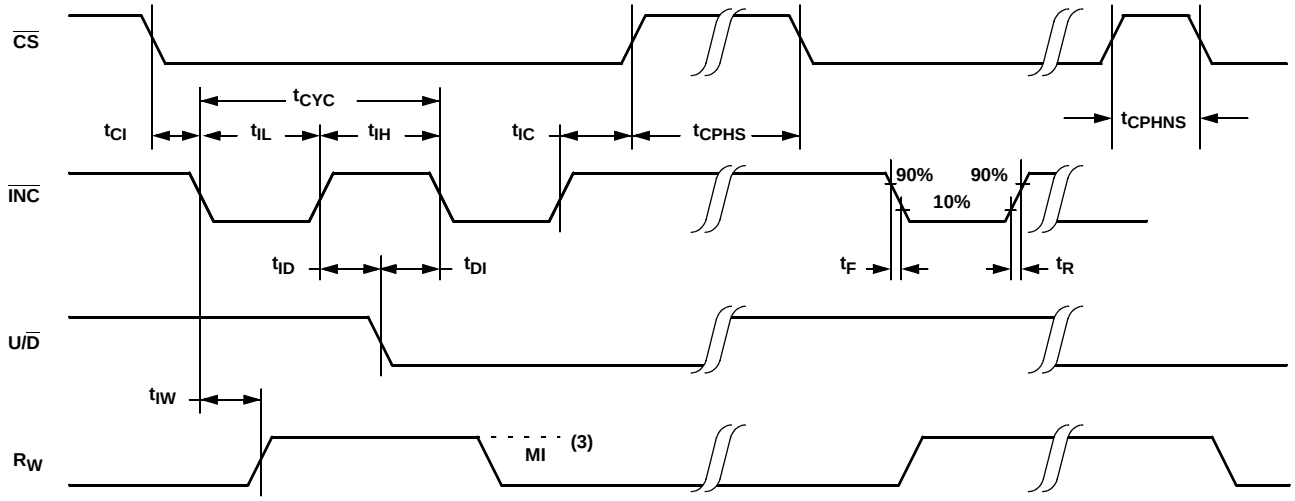
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated **(Continued)**

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNIT
t_{CYC}	$\overline{INC}$ cycle time	2			µs
t_R, t_F (Note 5)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU} (Note 5)	Power up to wiper stable			5	µs
$t_R V_{CC}$ (Note 5)	V_{CC} power-up rate	0.2		50	V/ms
t_{WR}	Store Cycle		5	10	ms

Power Up and Down Requirements

The recommended power up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1 millisecond after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on powerup.

AC Timing



Typical Performance Characteristics

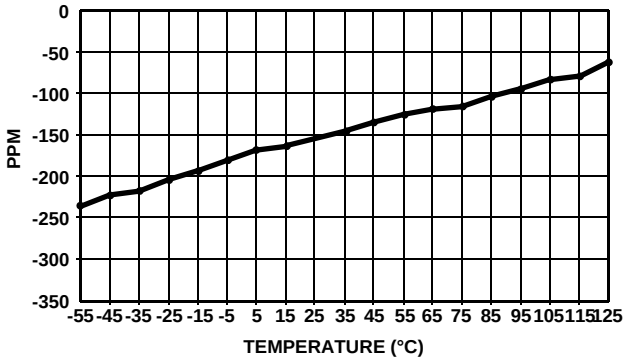


FIGURE 1. TYPICAL TOTAL RESISTANCE TEMPERATURE COEFFICIENT

Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the X9317 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

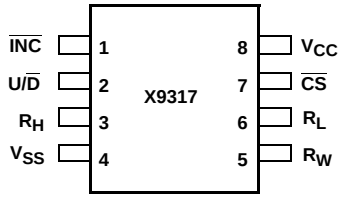
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

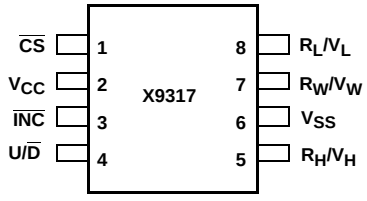
The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9317 will be placed in the low power standby mode until the device is selected once again.

Pin Configuration

DIP/SOIC/MSOP



TSSOP



Pin Names

SYMBOL	DESCRIPTION
R_H	High terminal
R_W	Wiper terminal
R_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
U/$\overline{D}$	Up/Down control input
$\overline{INC}$	Increment control input
$\overline{CS}$	Chip select control input

Principles of Operation

There are three sections of the X9317: the control section, the nonvolatile memory, and the resistor array. The control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. Electronic switches at either end of the array and between each resistor provide an electrical connection to the wiper pin, R_W.

The wiper acts like its mechanical equivalent and does not move beyond the first or last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of one hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9317, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a powerup/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

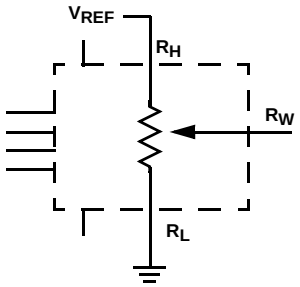
Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	Wiper up
L	↓	L	Wiper down
↑	H	X	Store wiper position to nonvolatile memory
H	X	X	Standby
↑	L	X	No store, return to standby
↓	L	H	Wiper Up (not recommended)
↓	L	L	Wiper Down (not recommended)

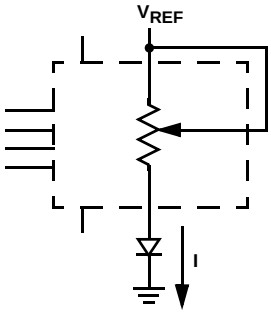
Applications Information

Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



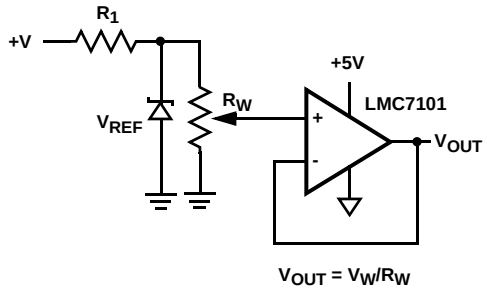
Three terminal potentiometer; variable voltage divider



Two terminal variable resistor; variable current

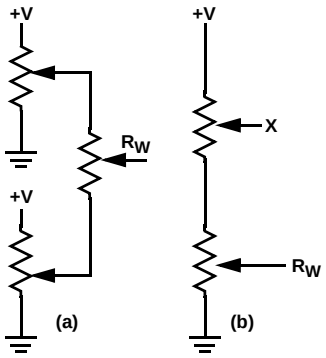
Basic Circuits

Buffered Reference Voltage

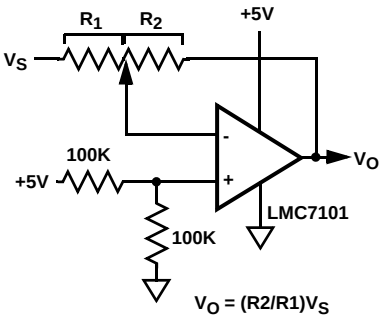


$V_{OUT} = V_W/R_W$

Cascading Techniques

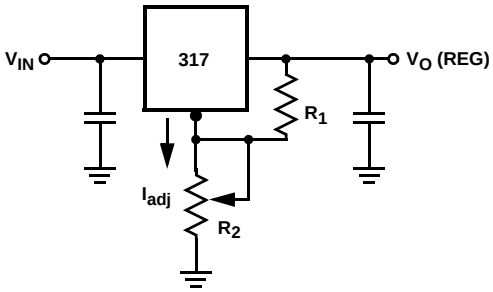


Single Supply Inverting Amplifier



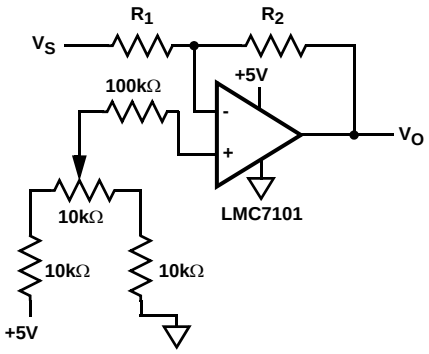
$V_O = (R2/R1)V_S$

Voltage Regulator

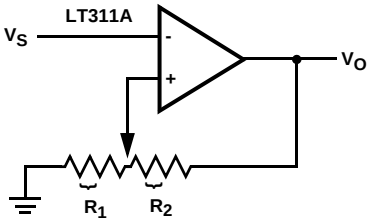


$V_O\ (REG) = 1.25V\ (1+R_2/R_1)+I_{adj}\ R_2$

Offset Voltage Adjustment



Comparator with Hysteresis

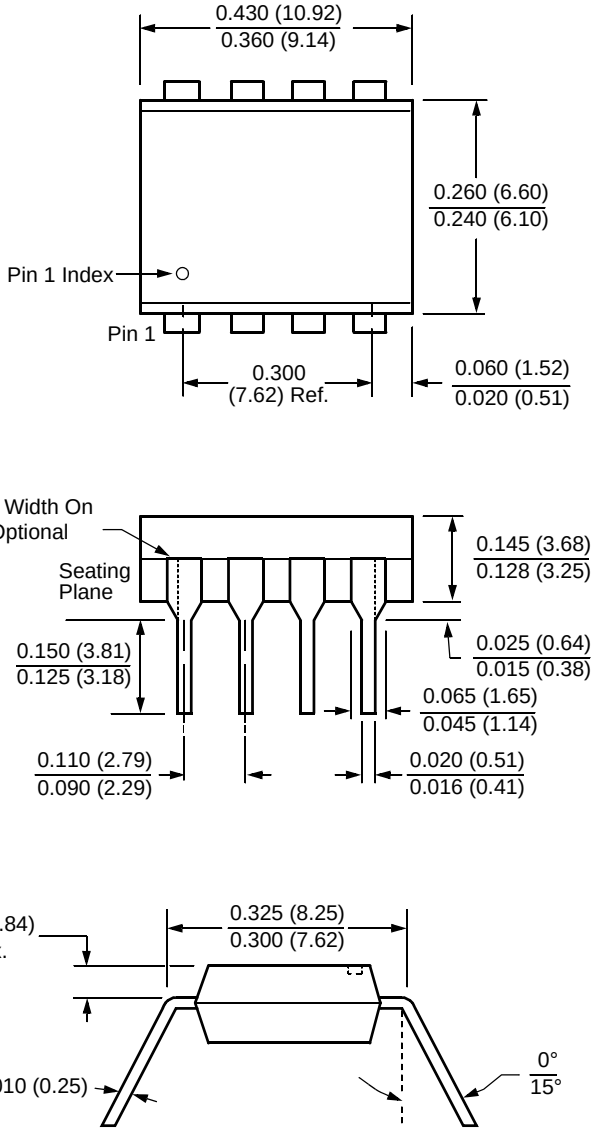


$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

(for additional circuits see AN115)

Packaging Information

8-Lead Plastic Dual In-Line (DIP) Package Type P

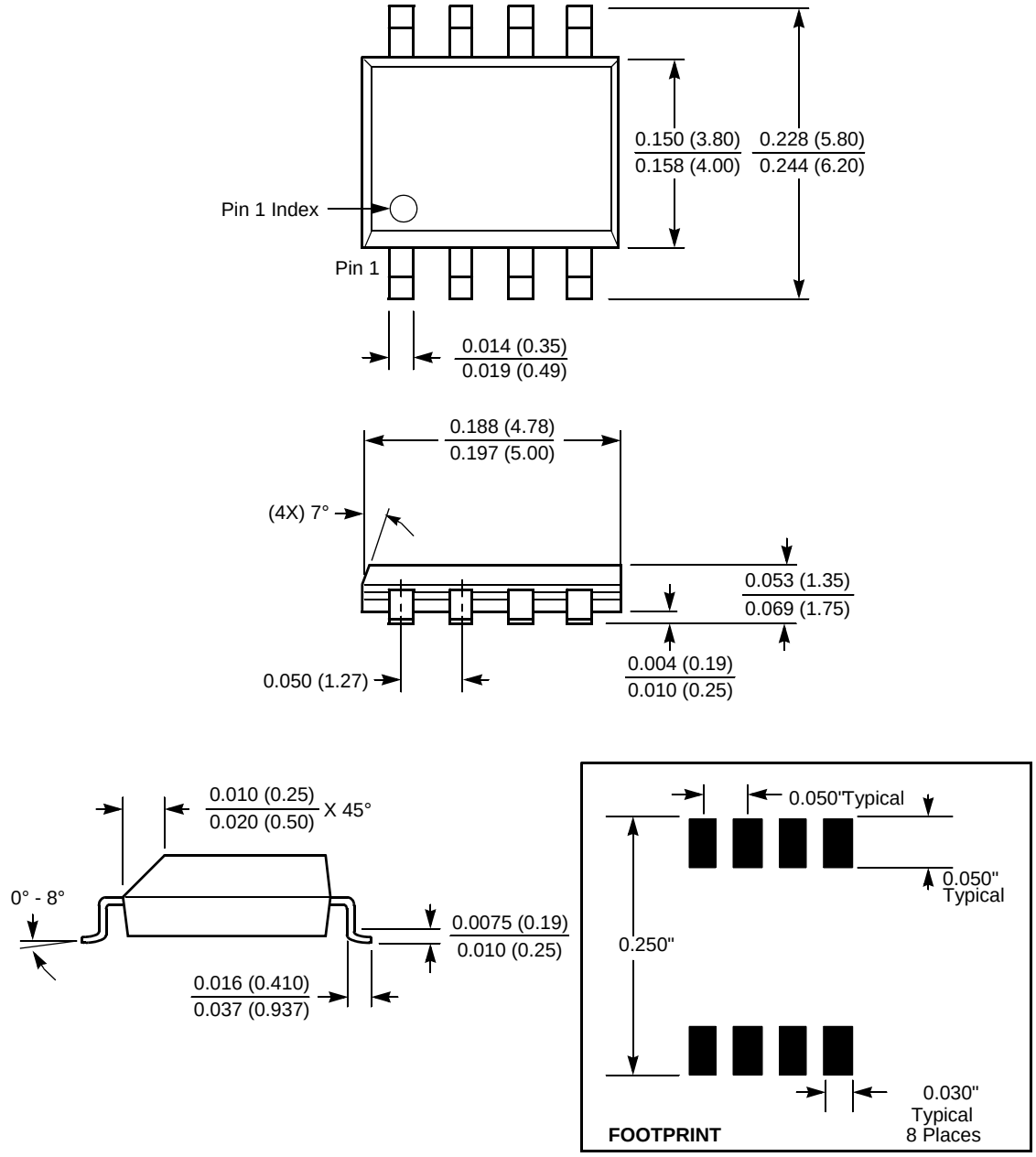


NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

Packaging Information

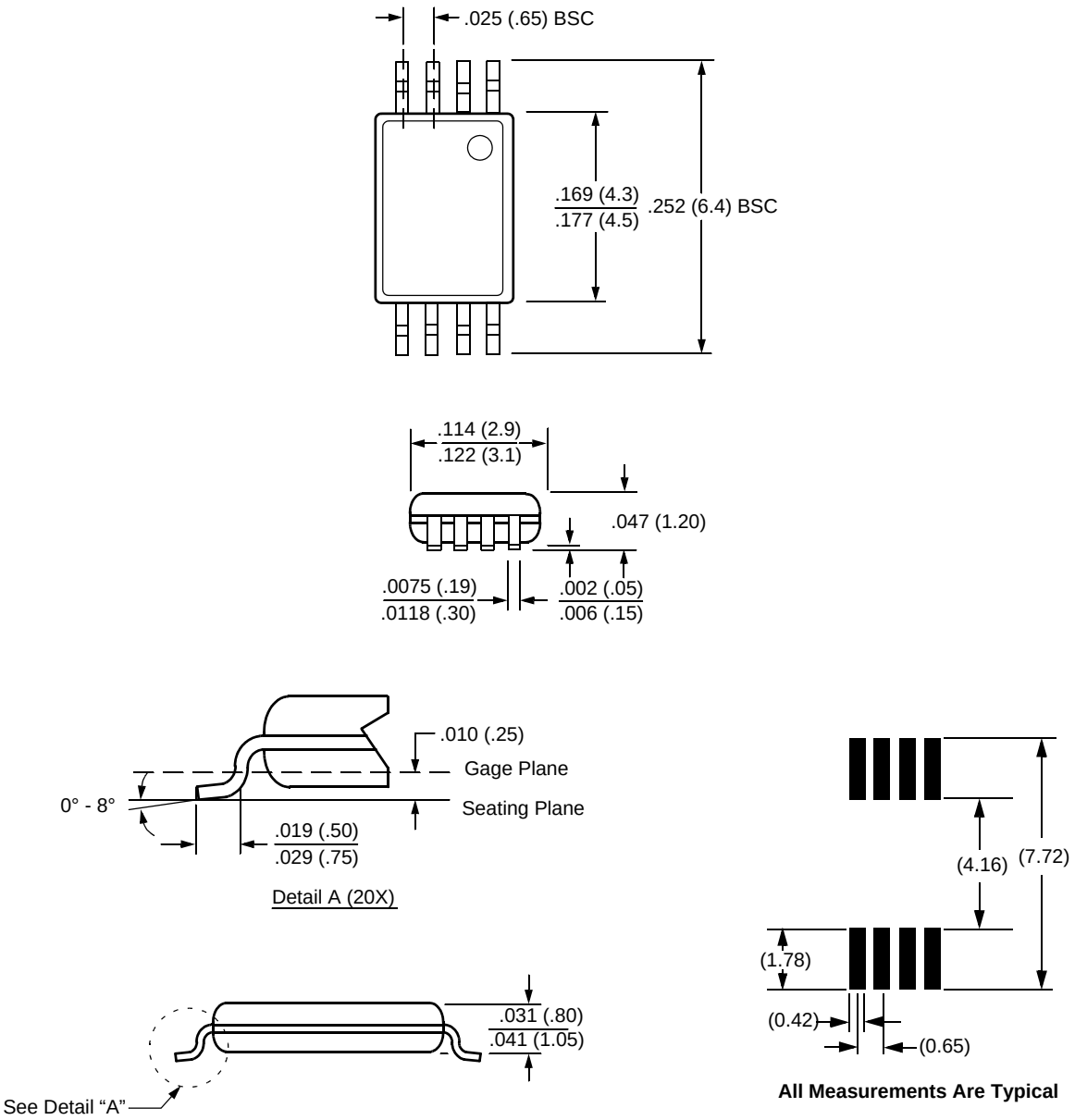
8-Lead Plastic Small Outline Gull Wing Package Type S (SOIC)



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

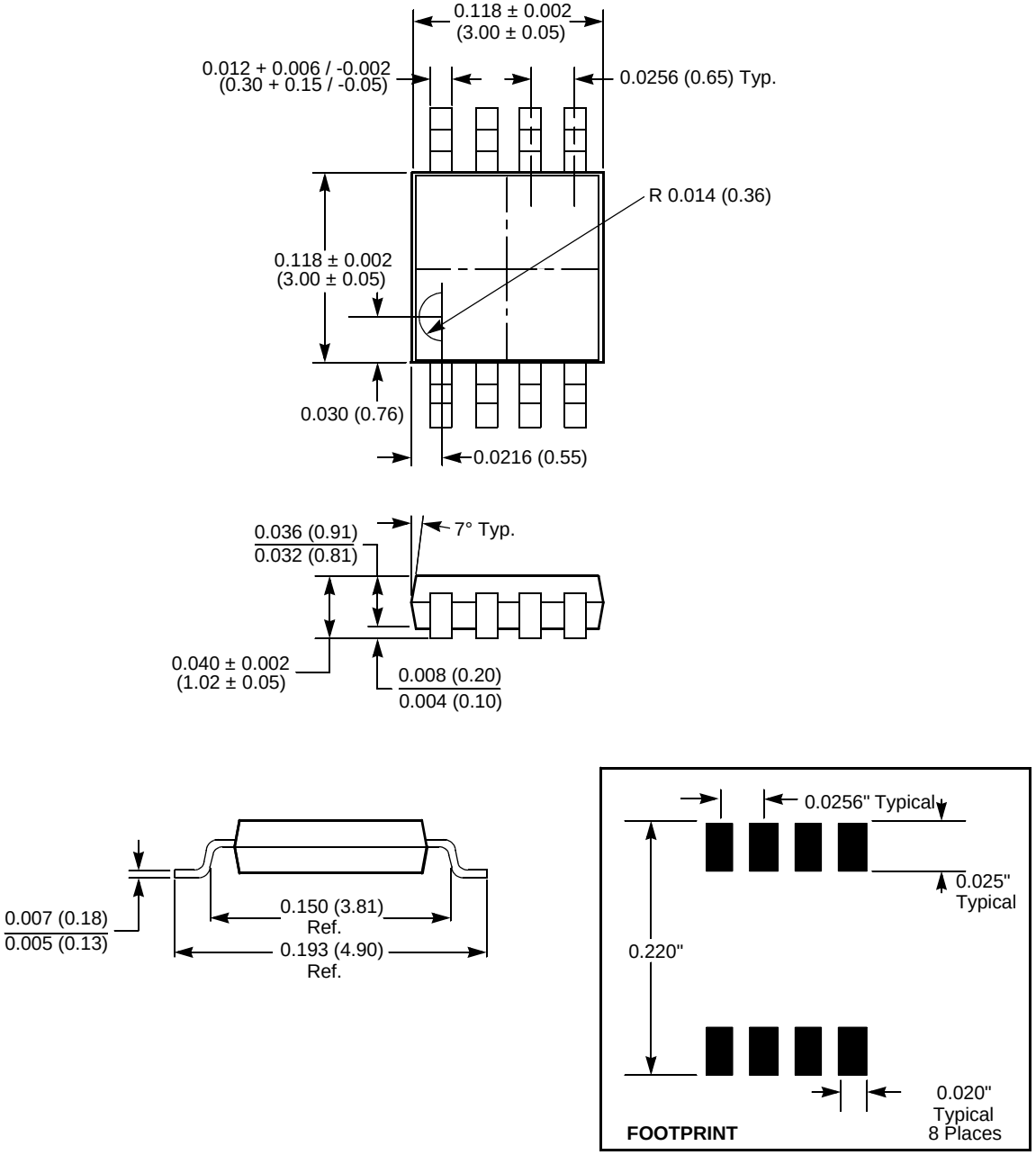
8-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

M Package
8-Lead Miniature Small Outline Gull Wing Package Type MSOP



NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality