ISL95810

Single Digitally Controlled Potentiometer (XDCP™)

Data Sheet | October 7, 2005 | FN8090.1

Low Noise, Low Power I²C Bus, 256 Taps

The ISL95810 integrates a digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR), that can be directly written to and read by the user. The content of the WR controls the position of the wiper. At power-up the device recalls the contents of the DCP's IVR to the WR.

The DCP can be used as three-terminal potentiometer or as two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 256 resistor taps - 0.4% resolution
- I²C serial interface
- Wiper resistance: 70Ω typical @ 3.3V
- Non-volatile storage of wiper position
- Standby current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ, 10kΩ total resistance
- High reliability
  - Endurance: 200,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ 75°C
- 8 Ld MSOP and 8 Ld TDFN packaging
- Pb-free plus anneal available (RoHS compliant)

Ordering Information

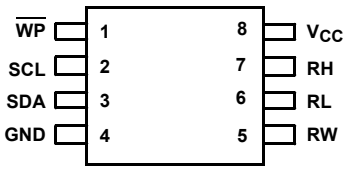
PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE
ISL95810WIU8*	AIU	10	-40 to 85	8 Ld MSOP
ISL95810WIU8Z* (Note)			-40 to 85	8 Ld MSOP (Pb-free)
ISL95810WIRT8Z* (Note)			-40 to 85	8 Ld 3 x 3 TDFN (Pb-free)
ISL95810UIU8*	AIT	50	-40 to 85	8 Ld MSOP
ISL95810UIU8Z* (Note)	AOK		-40 to 85	8 Ld MSOP (Pb-free)
ISL95810UIRT8Z* (Note)			-40 to 85	8 Ld 3 x 3 TDFN (Pb-free)

*Add "-T" suffix for tape and reel.

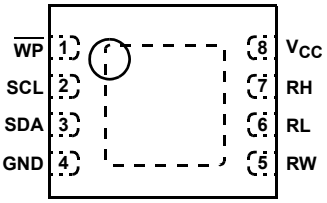
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

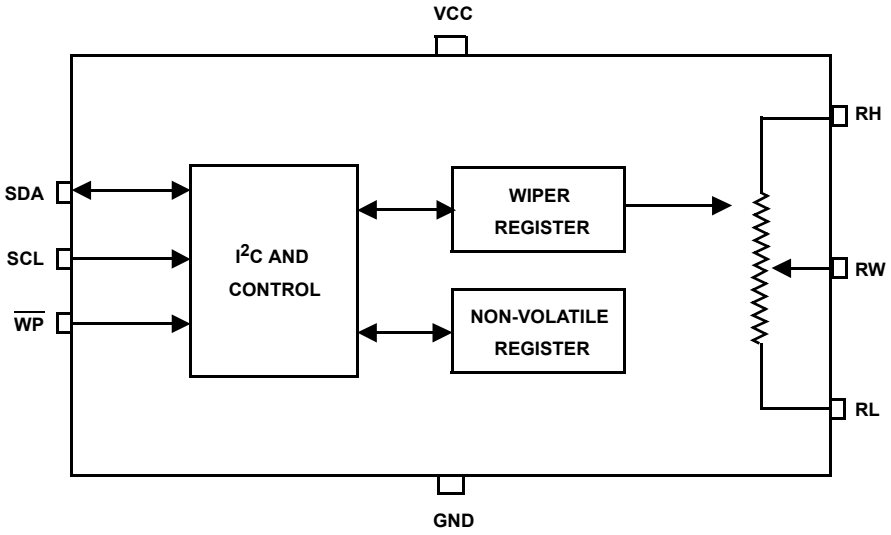
ISL95810
(8 LD MSOP)
TOP VIEW



ISL95810
(8 LD TDFN)
TOP VIEW



Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	$\overline{WP}$	Hardware write protection. Active low. Prevents any “Write” operation of the I^2C interface.
2	SCL	I^2C interface clock
3	SDA	Serial data I/O for the I^2C interface
4	GND	Ground
5	RW	“Wiper” terminal of the DCP
6	RL	“Low” terminal of the DCP
7	RH	“High” terminal of the DCP
8	V_{CC}	Power supply

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at Any Digital Interface Pin with Respect to V_{SS} . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at Any DCP Pin with Respect to V_{SS} . . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA

Recommended Operating Conditions

Industrial . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating of Each DCP 5mW
Wiper Current of Each DCP. . . . . ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W, U versions respectively			10, 50		kΩ
	R_H to R_L Resistance Tolerance			-20		+20	%
R_W	Wiper Resistance	V_{CC} = 3.3V @ 25°C Wiper current = V_{CC}/R_{TOTAL}			70	200	Ω
$C_H/C_L/C_W$	Potentiometer Capacitance (Note 13)				10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins (Note 13)	Voltage at pin from GND to V_{CC}			0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ RL; V_{CC} @ RH; measured at RW, unloaded)							
INL (Note 6)	Integral Non-Linearity			-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-Linearity	Monotonic over all tap positions	W option	-0.75		-0.75	LSB (Note 2)
			U option	-0.5		-0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-Scale Error	W option		0	1	7	LSB (Note 2)
		U option		0	0.5	2	
FSerror (Note 4)	Full-Scale Error	W option		-7	-1	0	LSB (Note 2)
		U option		-2	-0.5	0	
TC_V (Note 7, 13)	Ratiometric Temperature Coefficient	DCP Register set to 80 hex			±4		ppm/°C
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)							
RINL (Note 11)	Integral Non-Linearity	DCP register set between 20 hex and FF hex. Monotonic over all tap positions		-1		1	MI (Note 8)
RDNL (Note 5)	Differential Non-Linearity	DCP register set between 20 hex and FF hex. Monotonic over all tap positions	W option	-0.75		-0.75	MI (Note 8)
			U option	-0.5		-0.5	MI (Note 8)
Roffset (Note 9)	Offset	W option		0	1	7	MI (Note 8)
		U option		0	0.5	2	MI (Note 8)
TC_R (Note 12, 13)	Resistance Temperature Coefficient	DCP register set between 20 hex and FF hex			±45		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I_{CC1} (Note 15)	V_{CC} Supply Current (Volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			1	mA
I_{CC2} (Note 15)	V_{CC} Supply Current (Nonvolatile Write)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Nonvolatile Write State only)			3	mA
I_{SB} (Note 15)	V_{CC} Current (Standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			5	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			2	µA

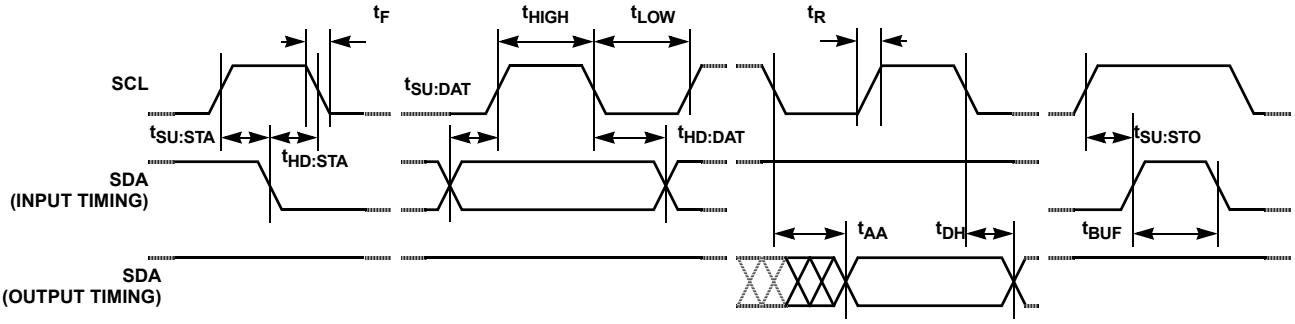
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I_{LkgDig}	Leakage Current, at Pins SDA, SCL, and $\overline{WP}$ Pins	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP} (Note 13)	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change			1	µs
Vpor	Power-On Recall Voltage	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V
V_{CC}Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D (Note 13)	Power-Up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECIFICATIONS						
	EEPROM Endurance		200,000			Cycles
	EEPROM Retention	Temperature ≤75°C	50			Years
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	$\overline{WP}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	$\overline{WP}$, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V
Hysteresis (Note 13)	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL} (Note 13)	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 13)	$\overline{WP}$, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN} (Note 13)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA} (Note 13)	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF} (Note 13)	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STO:NV}$	STOP Condition Hold Time for Non-Volatile Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	2			µs
t_{DH} (Note 13)	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 13)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns

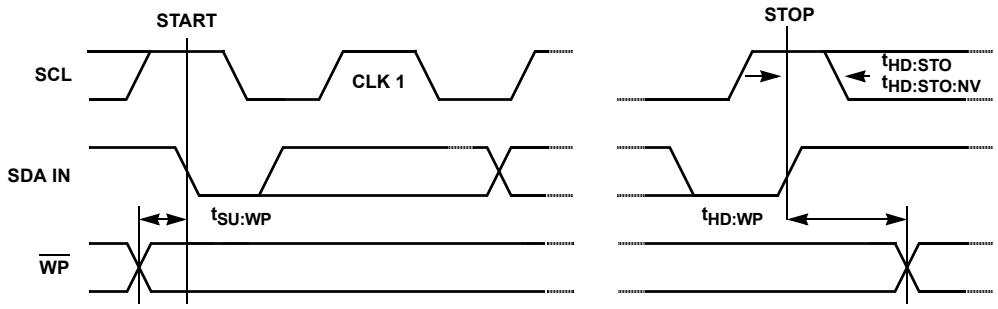
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
t_F (Note 13)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 13)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 13)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ
t_{WP} (Notes 13, 14)	Non-Volatile Write Cycle Time			12	20	ms
$t_{SU:WP}$	$\overline{WP}$ Setup Time	Before START condition	600			ns
$t_{HD:WP}$	$\overline{WP}$ Hold Time	After STOP condition	600			ns

SDA vs SCL Timing



$\overline{WP}$ Pin Timing



NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(RW)_0$/LSB.
4. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
5. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
6. INL = $[V(RW)_i – (i • LSB – V(RW)_0)]$/LSB for i = 1 to 255.
7. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$ for i = 16 to 240 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{255} – R_0|/255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively. Roffset = R_0/MI, when measuring between RW and RL.
9. Roffset = R_{255}/MI, when measuring between RW and RH.
10. RDNL = $(R_i – R_{i-1})$/MI, for i = 32 to 255.
11. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 32 to 255.
12. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$ for i = 32 to 255, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.

14. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
15. V_{IL} = 0V, V_{IH} = V_{CC}

Typical Performance Curves

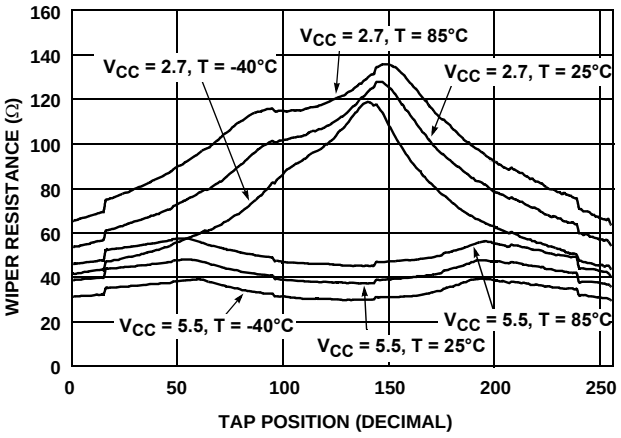


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC} / R_{TOTAL}] for 50kΩ (U)

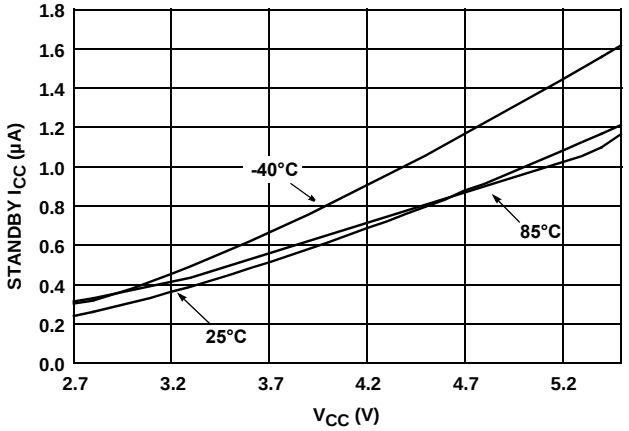


FIGURE 2. STANDBY I_{CC} vs V_{CC}

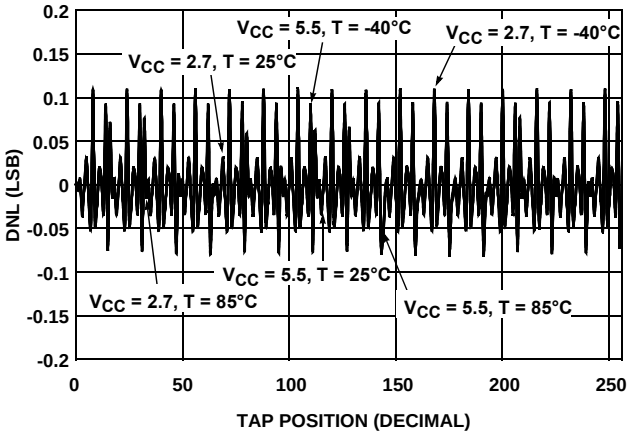


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

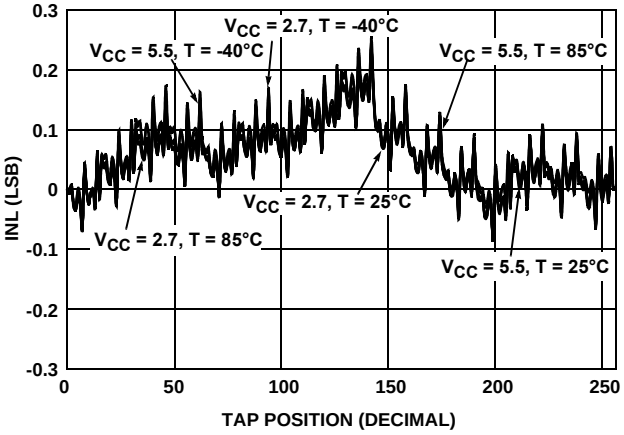


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

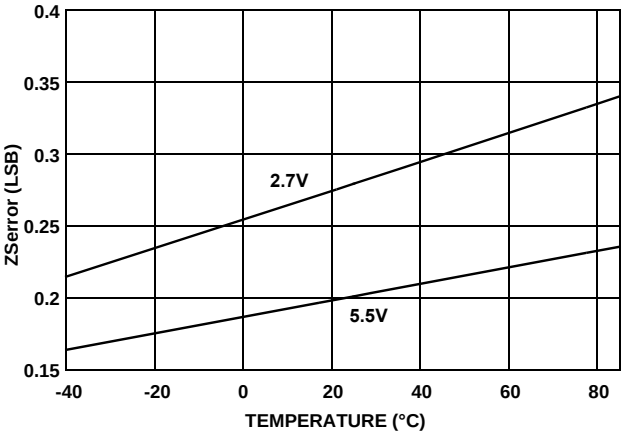


FIGURE 5. ZSerror vs TEMPERATURE

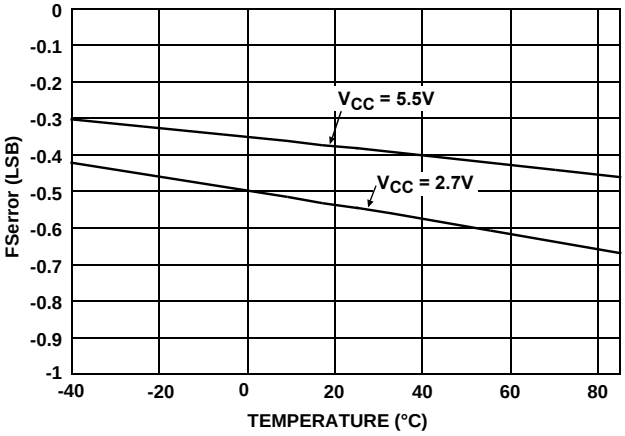


FIGURE 6. FSerror vs TEMPERATURE

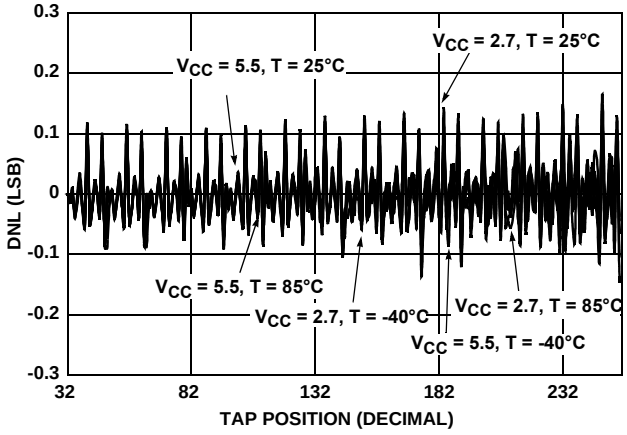


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

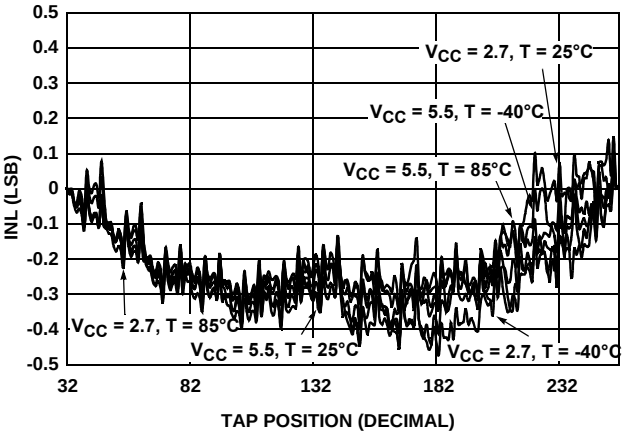


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

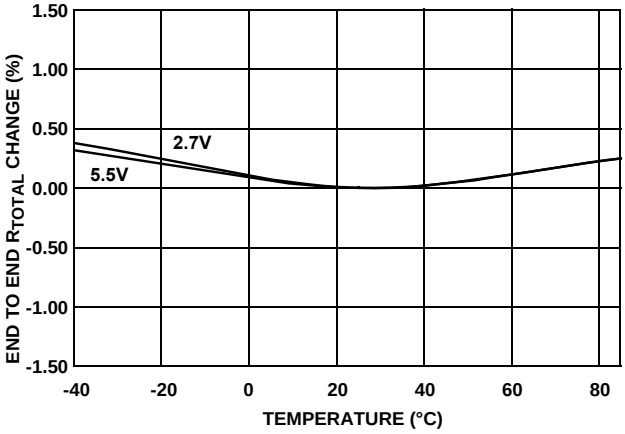


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

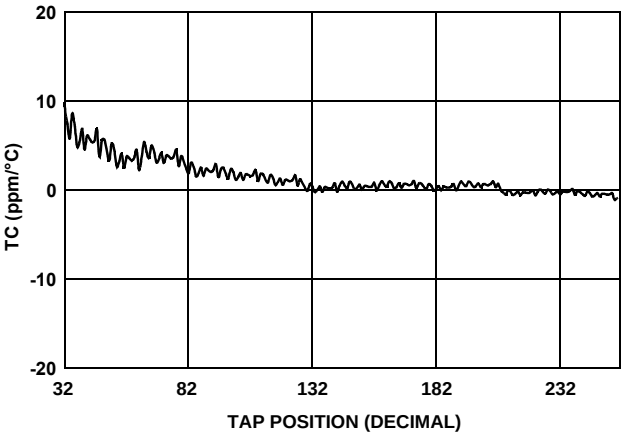


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

Typical Performance Curves (Continued)

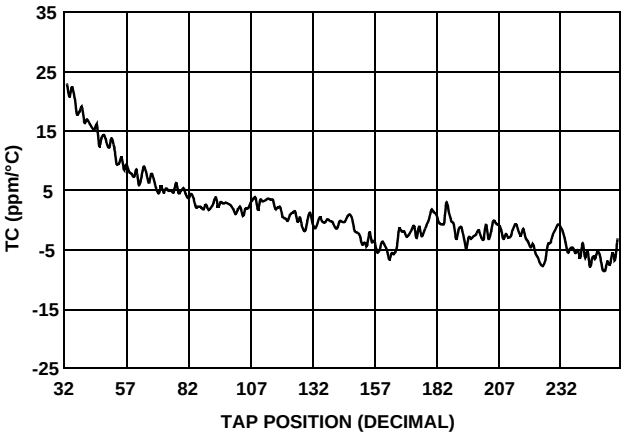


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

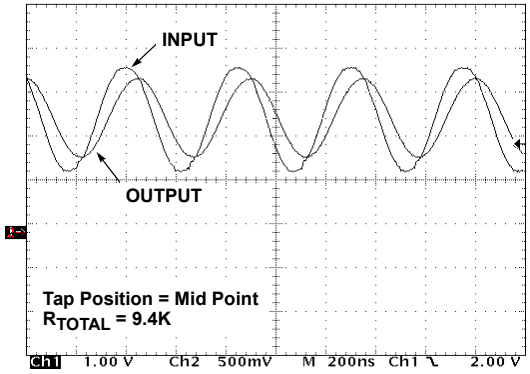


FIGURE 12. FREQUENCY RESPONSE (2.2MHz)

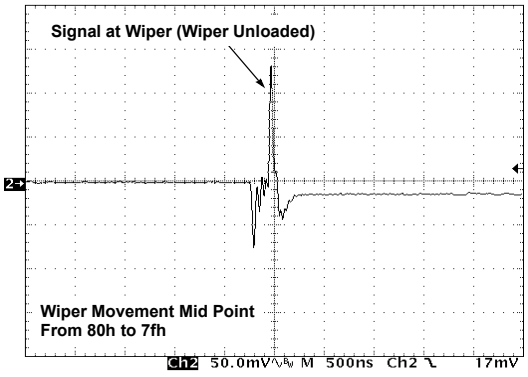


FIGURE 13. MIDSCALE GLITCH, CODE 80h to 7Fh (WIPER 0)

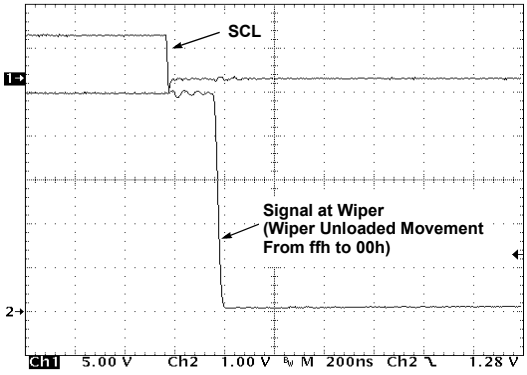


FIGURE 14. LARGE SIGNAL SETTLING TIME

Principles of Operation

The ISL95810 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory, and a I^2C serial interface providing direct communication between a host and the potentiometer and memory.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). The DCP has its own WR. When the WR of the DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR of the DCP contains all ones (WR<7:0>: FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL95810 is being powered up, The WR is reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the ISL95810 reads the value stored in non-volatile Initial Value Registers (IVRs) and loads it into the WR.

The WR and IVR can be read or written directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL95810 volatile and non-volatile registers are accessed by I^2C interface operations at addresses 0 and 2 decimal. The non-volatile byte at addresses 0 contains the initial value loaded at power-up into the volatile Wiper Register (WR) of the DCP. The byte at address 1 is reserved; the user should not write to it, and its value should be ignored if read.

The volatile WR, and the non-volatile Initial Value Register (IVR) of the DCP are accessed with the same Address Byte, set to 00 hex in both cases.

A volatile byte at address 2 decimal, controls what byte is read or written when accessing DCP registers: the WR, the IVR, or both.

When the byte at address 2 is all zeroes, which is the default at power-up:

- A read operation to addresses 0 outputs the value of the non-volatile IVR.
- A write operation to addresses 0 writes the same value to the WR and IVR of the corresponding DCP.

When the byte at address 2 is 80h (128 decimal):

- A read operation to addresses 0 outputs the value of the volatile WR.
- A write operation to addresses 0 only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

The ISL95810 is pre-programed with 80h in the IVR.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	Access Control
1	Reserved	
0	IVR	WR

WR: Wiper Register, IVR: Initial value Register.

I^2C Serial Interface

The ISL95810 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL95810 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 15). On power-up of the ISL95810 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL95810 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 15). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation to

volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 16).

The ISL95810 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL95810 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 as the seven MSBs. The LSB in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 2).

TABLE 2. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{W}$
(MSB)							(LSB)

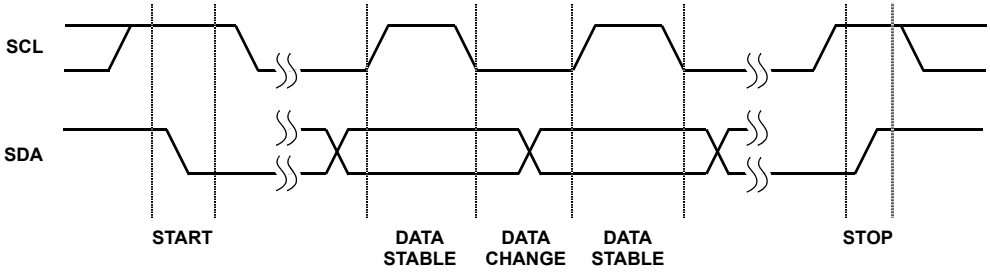


FIGURE 15. VALID DATA CHANGES, START, AND STOP CONDITIONS

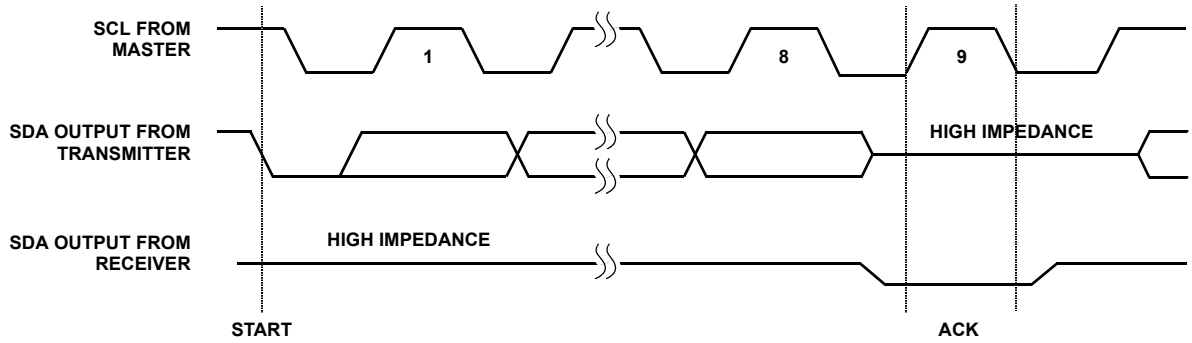


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

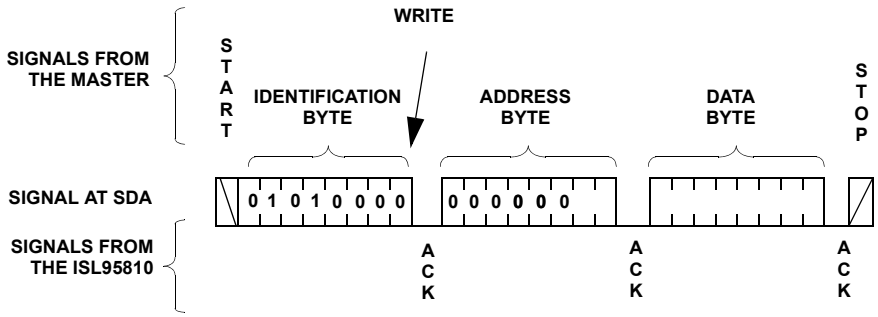


FIGURE 17. BYTE WRITE SEQUENCE

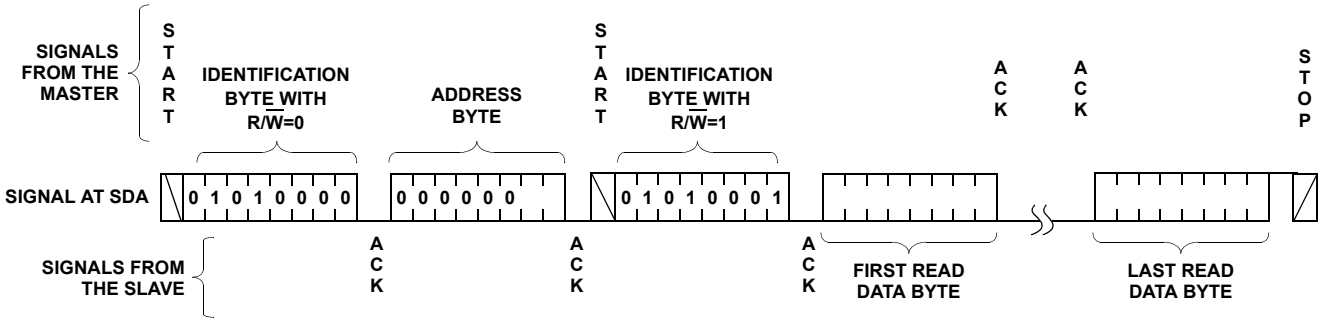


FIGURE 18. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL95810 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95810 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95810 enters its standby state (See Figure 17).

The byte at address 02h determines if the Data Byte is to be written to volatile and/or non-volatile memory (See “Memory Description” on page 7).

Data Protection

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When the $\overline{WP}$ is active (LOW) the device ignores Data Bytes of a Write Operation, does not respond to the Data Bytes with an ACK, and instead, goes to its standby state waiting for a new START condition.

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

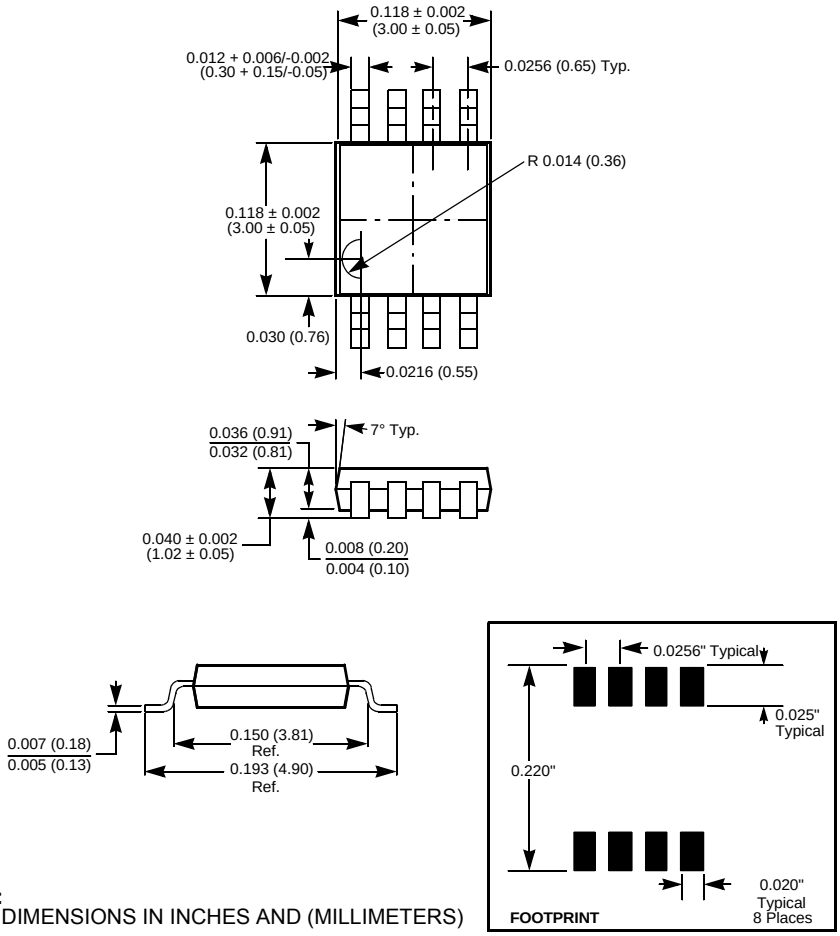
Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL95810 responds with an ACK. Then the ISL95810 then transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (See Figure 18).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory (See “Memory Description” on page 9.)

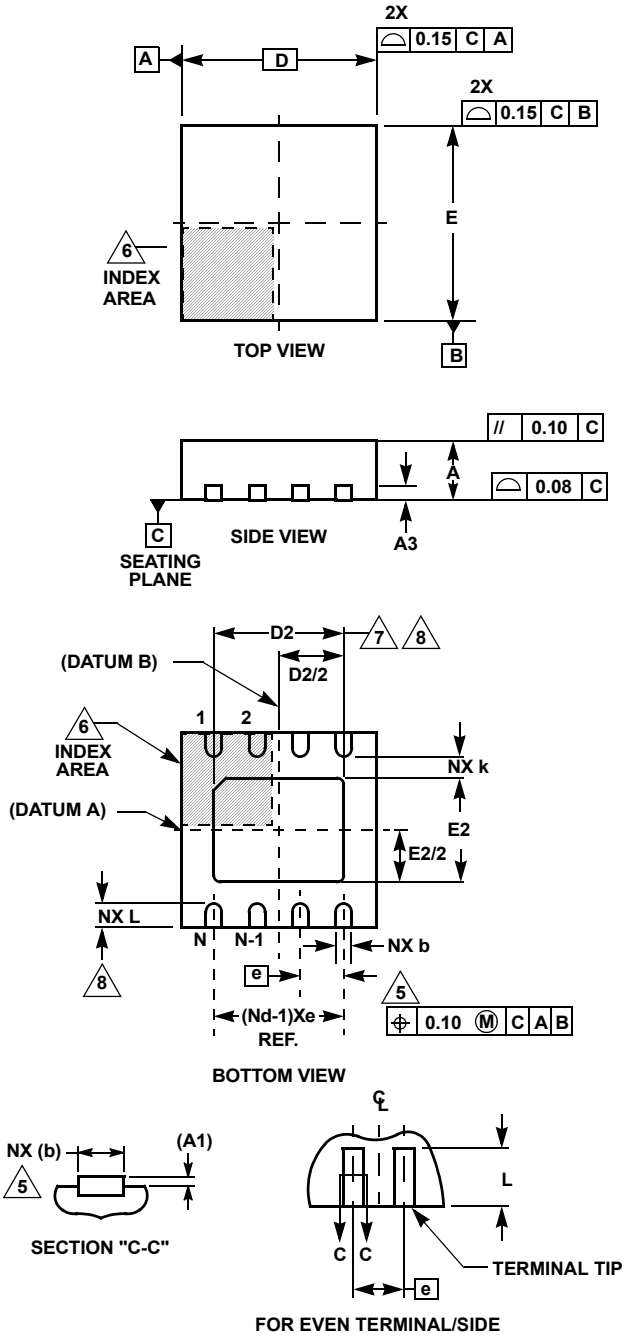
MSOP Packaging Information

8-Lead Plastic, MSOP, Package Code U8



NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3B

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.23	0.30	0.38	5, 8
D		3.00 BSC		-
D2	2.15	2.30	2.40	7, 8
E		3.00 BSC		-
E2	1.35	1.50	1.60	7, 8
e		0.65 BSC		-
k	0.20	-	-	-
L	0.20	0.30	0.40	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.