ISL95711

Digitally Controlled Potentiometer (XDCP™)

Data Sheet | August 15, 2005 | FN8241.2

Terminal Voltage ±3V or ±5V, 128 Taps I^2C Serial Interface

The Intersil ISL95711 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a I^2C interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. The wiper terminal can be connected to either end of the resistor array or at any one of the Tap Positions in between, providing 128 steps of resolution between R_L and R_H. The “position” of the wiper is determined by the value assigned to the volatile Wiper Register (WR). This register has an associated non-volatile Initial Value Register (IVR). The value stored in the IVR will be written into the WR at power-up, allowing wiper position recall after power interruption. The WR and the IVR can be directly written to and read from using standard I^2C interface protocol. The device is available in either a 10kΩ or 50kΩ version.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Industrial and automotive control
- Parameter and bias adjustments
- Amplifier bias and control

Ordering Information

PART NUMBER	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL95711WIU10Z (Notes 1& 2)	10K	-40 to +85	10-Ld MSOP
ISL95711UIU10Z (Notes 1& 2)	50K	-40 to +85	10-Ld MSOP

NOTES:

1. Add “-T” suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

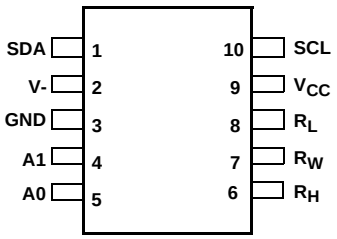
Features

- Non-Volatile Solid-State Potentiometer
- I^2C Serial Interface with Hardwire Slave Address Allows Up to Four Devices
- DCP Terminal Voltage, from V- to V_{CC}
- 128 Wiper Tap Points
  - Wiper position can be stored in nonvolatile memory and recalled on power-up
- 127 Resistive Elements
  - Typical tempco ±50ppm/°C
  - Ratiometric Tempco ±4ppm/°C
  - End to end resistance range ±20%
- Low Power CMOS
  - Standby current, 1µA
  - Active current, 200µA max
  - V_{CC} = 3V to 5.5V
  - V- = -3V to -5.5V
- High Reliability
  - Endurance, 200,000 data changes per bit
  - Register data retention, 50 years
- R_{TOTAL} Values = 10kΩ, 50kΩ
- Package
  - 10-lead MSOP
  - Pb-Free plus anneal available (RoHS compliant)

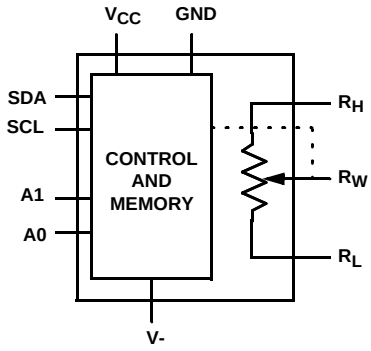
Pinout

ISL95711
(10-LD MSOP)

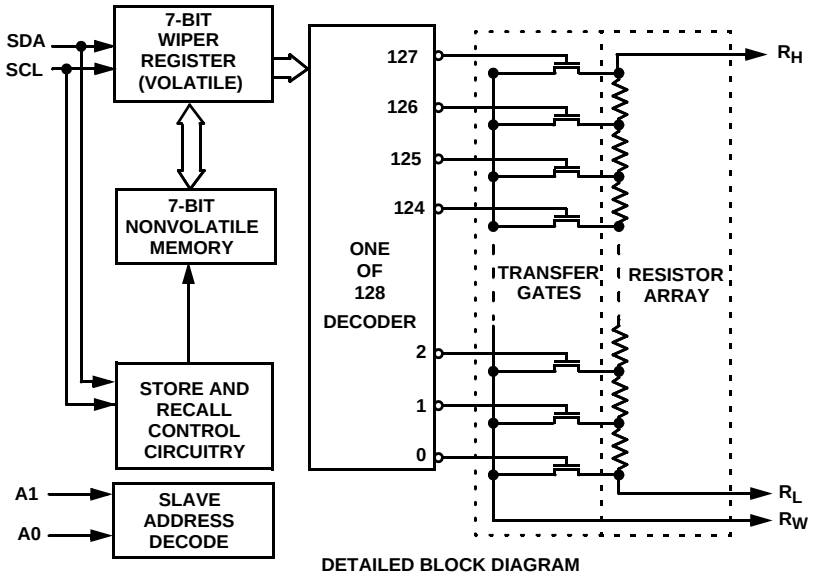
TOP VIEW



Block Diagram



SIMPLE BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	SDA	Data I/O for I^2C serial interface. It has an open drain output and may be wire or'd with other open drain active low outputs.
2	V-	Negative supply voltage for the potentiometer wiper control.
3	GND	Ground.
4	A1	A1 and A0 are address select pins used to set the slave address for the I^2C serial interface.
5	A0	A1 and A0 are address select pins used to set the slave address for the I^2C serial interface.
6	R_H	A fixed terminal for one end of the potentiometer resistor.
7	R_W	The wiper terminal which is equivalent to the movable terminal of a potentiometer.
8	R_L	A fixed terminal for one end of the potentiometer resistor.
9	V_{CC}	Positive logic supply voltage
10	SCL	Clock input for the I^2C serial interface.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on SDA, SCL, A0, and A1
with respect to GND . . . . . -0.3 to V_{CC}+0.3V
Voltage on V- (referenced to GND) . . . . . -6V
$\Delta V = |V_{(RH)}-V_{(RL)}|$ 12V
Lead temperature (soldering 10 seconds) . . . . . 300°C
I_W (10 seconds) . . . . . ±6mA
V_{CC} . . . . . -.03V to 6V
R_H, R_L, R_W . . . . . V- to V_{CC}

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 3V to 5.5V
V- . . . . . -3V to -5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L resistance tolerance		-20		+20	%
R_H,R_L	R_H,R_L terminal voltage		V-		V_{CC}	V
R_W	Wiper resistance	V- = -5.5V; V_{CC} = +5.5V, wiper current = (V_{CC}-V-)/R_{TOTAL}		70	200	Ω
C_H/C_L/C_W	Potentiometer Capacitance (Note 13)			10/10/ 25		pF
I_{LkgDCP}	Leakage on R_H, R_L, R_W pins	Voltage at pins; V- to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ R_L; V_{CC} @ R_H; Voltage at R_W = V_{RW} unloaded)						
INL (Note 6)	Integral non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential non-linearity	W, U options	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-scale error	W option	0	1	4	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-scale error	W option	-4	-1	0	LSB (Note 2)
		U option	-2	-1	0	
TC_V (Notes 7, 13)	Ratiometric Temperature Coefficient	DCP Register set between 16 to 120d, T = -40°C to +85°C		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 11)	Integral non-linearity	DCP register set between 20 hex and 7F hex. Monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential non-linearity	W and U options	-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP Register set to 00 hex, W option	0	2	5	MI (Note 8)
		DCP Register set to 00 hex, U option	0	0.5	2	
TC_R (Notes 12, 13)	Resistance Temperature Coefficient	DCP register set between 16 and 127d, T = -40°C to +85°C		±50		ppm/°C

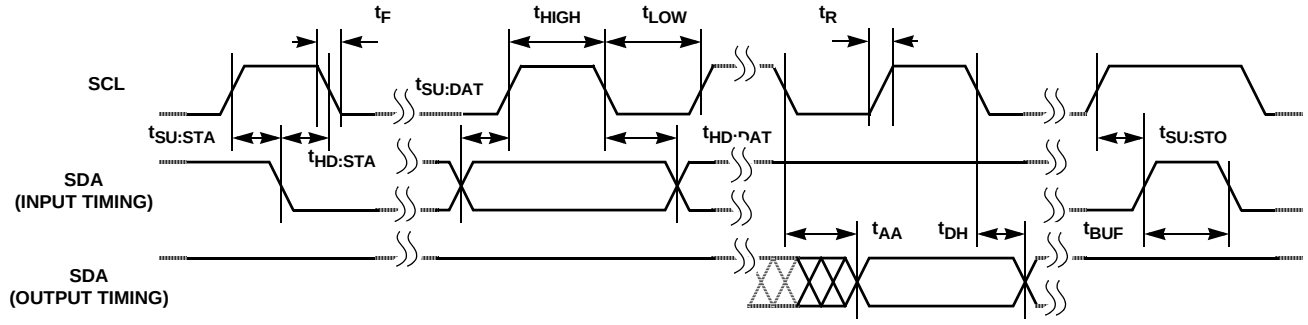
Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I_{CC1}	V_{CC} supply current, volatile write/read	f_{SCL} = 400kHz;SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			200	µA
I_{V-1}	V- supply current, volatile write/read	f_{SCL} = 400kHz;SDA = Open; (for I^2C, Active, Read and Volatile Write States only)	-100			µA
I_{CC2}	V_{CC} supply current, non volatile write	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Nonvolatile Write State only)			200	µA
I_{V-2}	V- supply current, nonvolatile write	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Nonvolatile Write State only)	-3			mA
I_{CCSB}	V_{CC} current (standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			1	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			1	µA
I_{V-SB}	V- current (standby)	V- = -5.5V, I^2C Interface in Standby State	-5			µA
		V- = -3.6V, I^2C Interface in Standby State	-2			µA
I_{LkgDig}	Leakage current, at pins SDA, SCL, A0, and A1	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP} (Note 13)	DCP wiper response time	SCL falling edge of last bit of DCP Data Byte to wiper change		1		µs
Vpor	Power-on recall for both V- and V_{CC}	V-	-2.5			V
		V_{CC}			2.5	V
V-Ramp	V- ramp rate		0.2			V/ms
t_D (Note 13)	Power-up delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state		3		ms
EEPROM SPECS						
	EEPROM Endurance		200,000			Cycles
	EEPROM Retention	Temperature ≤ 75°C	50			Years
SERIAL INTERFACE SPECS						
V_{IL}	A0, A1, SDA, and SCL input buffer LOW voltage		-0.3		0.3*V_{CC}	V
V_{IH}	A0, A1, SDA, and SCL input buffer HIGH voltage		0.7*V_{CC}		V_{CC}+ 0.3	V
Hysteresis	SDA and SCL input buffer hysteresis		0.05* V_{CC}			V
V_{OL}	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
Cpin (Note 15)	A0, A1, SDA, and SCL pin capacitance				10	pF
f_{SCL}	SCL frequency				400	kHz
t_{IN}	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA}	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW time	Measured at the 30% of V_{CC} crossing.	1300			ns

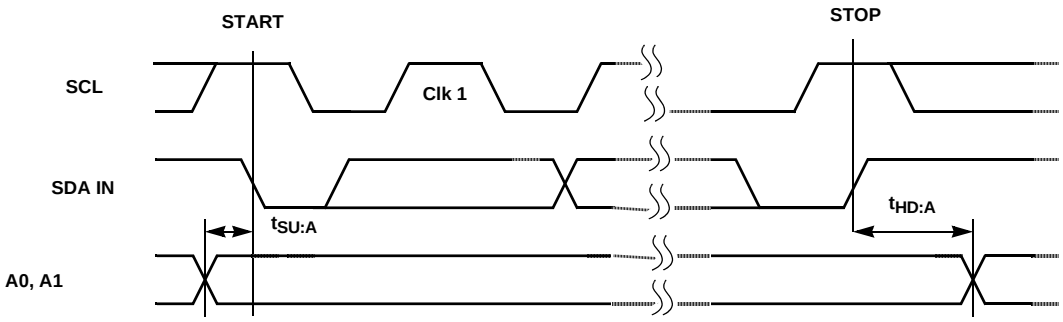
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input data hold time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP condition setup time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH}	Output data hold time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 15)	SDA and SCL rise time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 15)	SDA and SCL fall time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 15)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 15)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ.	1			kΩ
t_{WC} (Notes 14)	Non-volatile Write cycle time			12	20	ms
$t_{SU:A}$	A0, A1 setup time	Before START condition	600			ns
$t_{HD:A}$	A0, A1 hold time	After STOP condition	600			ns

SDA vs SCL Timing



A0, A1 Pin Timing



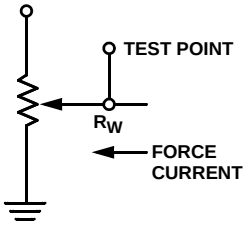
NOTES:

1. Typical values are for T_A = 25°C and ±5V supply voltage.
2. LSB: $[V(RW)_{127} – V(RW)_0] / 127$. $V(RW)_{127}$ and $V(RW)_0$ are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $(V(RW)_0 – V-) / LSB$.
4. FS error = $[V(RW)_{127} – V_{CC}] / LSB$.
5. DNL = $[V(RW)_i – V(RW)_{i-1}] / LSB-1$, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(RW)_i – (i • LSB – V(RW)_0)$ for i = 1 to 127.
7. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$

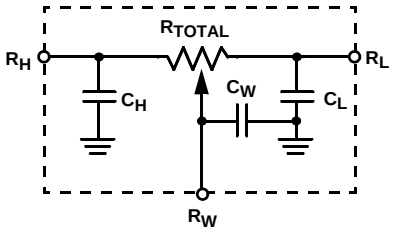
   for i = 16 to 120 decimal. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0| / 127$. R_{127} and R_0 are the measured resistances for the DCP register set to 127d and 0 respectively.
9. Roffset = R_0 / MI, when measuring between R_W and R_L.
   Roffset = R_{127} / MI, when measuring between R_W and R_H.
10. RDNL = $(R_i – R_{i-1}) / MI$, for i = 16 to 127.
11. RINL = $[R_i – (MI • i) – R_0] / MI$, for i = 16 to 127.
12. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$

    for i = 16 to 127d. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.
14. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
15. These are I^2C specific parameters and are not directly tested, however they are used during device testing to validate device specification.

Test Circuit



Equivalent Circuit



Pin Descriptions

Potentiometer Pins

R_H AND R_L

The high (R_H) and low (R_L) terminals of the ISL95711 are equivalent to the fixed terminals of a mechanical potentiometer. R_H and R_H are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 127, the wiper will be closest to R_H, and with the WR set to 00, the wiper is closest to R_L

R_W

R_w is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for the I^2C interface. It receives device address, operation code, wiper register address and data from a I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

SDA requires an external pull-up resistor, since it's an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface.

SCL requires an external pull-up resistor, since it's an open drain input.

DEVICE ADDRESS (A1-A0)

The Address inputs are used to set the least significant 2 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must be made with the Address input pins in order to initiate communication with the ISL95711. A maximum of 4 ISL95711 devices may occupy the I^2C serial bus.

Principles of Operation

The ISL95711 is an integrated circuit incorporating one DCP with it's associated register, non-volatile memory, and the I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a "make before break" mode when the wiper changes tap positions.

When the device is powered-down, the last value stored in the IVR will be maintained in the nonvolatile memory. When power is restored, the contents of the IVR are recalled and the wiper is set to that value.

The ISL95711 has dual supplies, V_{CC} and V-. For proper operation of the chip, it is recommended both power supplies ramp up simultaneously to their final values within 20ms. The chip design gives priority to the V- supply stabilization and then looks at V_{CC} stabilization. As the V- supply goes below -2.5V, the R_W pin goes to the default code of 64. As V_{CC} also exceeds 2.5V (after V- < -2.5V), the R_W pin goes to the code stored in the EEPROM memory value (this is referred as power on recall).

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal is controlled by a 7-bit volatile Wiper Register (WR). When the WR contains all zeroes (00h), the wiper terminal (R_W) is closest to its "Low" terminal (R_L). When the WR contains all ones (7Fh), the wiper terminal (R_W) is closest to its "High" terminal (R_H). As the value of the WR increases from all zeroes (00h) to all ones (7Fh), the wiper moves monotonically from the position closest to R_L to the position closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically.

While the ISL95711 is being powered up, the WR is reset to 40h (64 decimal), which locates the R_W at the center

between R_L and R_H. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading (~ ± 2.5V), the ISL95711 reads the value stored on a non-volatile Initial Value Register (IVR) and loads it into the WR.

The WR and IVR can be read or written directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL95711 contains 1 non-volatile byte know as the Initial Value Register (IVR). It is accessed by the I^2C interface operations with Address 00h. The IVR contains the value which is loaded into the Volatile Wiper Register (WR) at power-up.

The volatile WR, and the non-volatile IVR of a DCP are accessed with the same address.

The Access Control Register (ACR) determines which byte at address 00h is accessed (IVR or WR). The volatile ACR must be set as follows:

When the ACR is all zeroes, which is the default at power-up:

- A read operation to address 0 outputs the value of the non-volatile IVR.
- A write operation to address 0 writes the same value to the WR and IVR of the corresponding DCP.

When the ACR is 80h:

- A read operation to address 0 outputs the value of the volatile WR.
- A write operation to address 0 only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	ACR
1	Reserved	
0	IVR	WR

WR: Wiper Register, IVR: Initial value Register.

The ISL95711 is pre-programmed with 40h in the IVR.

I^2C Serial Interface

The ISL95711 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL95711 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 1). On power-up of the ISL95711 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL95711 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 1). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 1). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 2).

The ISL95711 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL95711 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1, and A0. The LSB is in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation. (See Table 2.)

TABLE 2. IDENTIFICATION BYTE FORMAT

Logic values at pins A1, and A0 respectively

0	1	0	1	0	A1	A0	R/$\overline{\text{W}}$

(MSB) (LSB)

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL95711 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95711 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95711 enters its standby state (See Figure 3).

The byte at address 02h determines if the Data Byte is to be written to volatile or both volatile and non-volatile. (See "Memory Description" on page 8.)

Data Protection

A STOP condition acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 4). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL95711 responds with an ACK; then the ISL95711 transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (See Figure 4).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory. (See "Memory Description".)

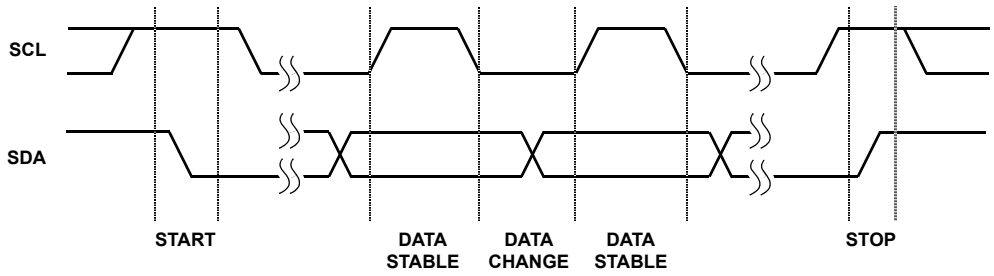


FIGURE 1. VALID DATA CHANGES, START, AND STOP CONDITIONS

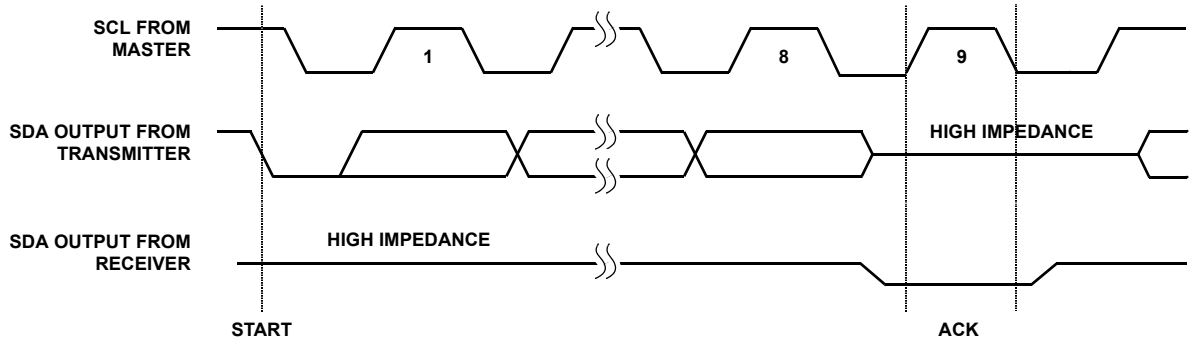


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

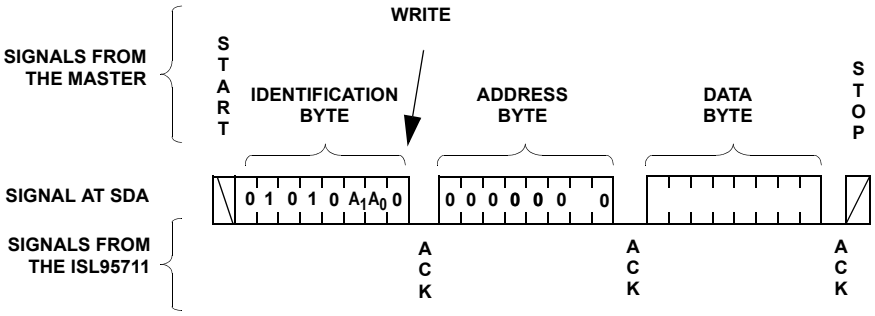


FIGURE 3. BYTE WRITE SEQUENCE

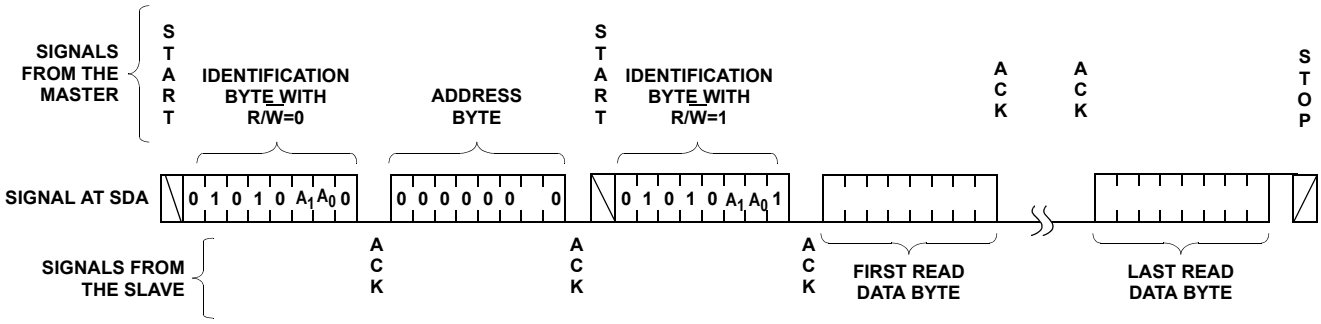


FIGURE 4. READ SEQUENCE

Communicating with the ISL95711

There are 3 register addresses in the ISL95711, of which two can be used. Address 00h and address 02h are used to control the device. Address 01h is reserved and should not be used. Address 00h contains the non-volatile Initial Value Register (IVR), and the volatile Wiper Register (WR). Address 02h contains only a volatile word and is used as a pointer to either the IVR or WR. See Table 1.

Register Descriptions: Access Control

The Access Control Register (ACR) is volatile and is at address 02h. It is 8-bits, and only the MSB is significant, all other bits should be zero (0). The ACR controls which word is accessed at register 00h as follows:

00h = Nonvolatile IVR

80h = Volatile WR

All other bits of the ACR should be written to as zeros. Only the MSB can be either 0 or 1. Power-up default for this address is 00h.

Register Description: IVR and WR

The ISL95711 has a single potentiometer. The wiper of the potentiometer is controlled directly by the WR. Writes and reads can be made directly to this register to control and monitor the wiper position without any non-volatile memory changes. This is done by setting address 02h to data 80h, then writing the data.

The non-volatile IVR stores the power-up value of the wiper. On power-up, the contents of the IVR are transferred to the WR.

To write to the IVR, first address 02h is set to data 00h, then the data is written. Writing a new value to the IVR register will set a new power-up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. So, if a new value is loaded into the IVR, not only will the non-volatile IVR change, but the WR will also contain the same value after the write, and the wiper position will change. Reading from the IVR will not change the WR, if its contents are different.

Example 1

Writing a new value (77h) to the IVR:

Write to ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	

Then, write to IVR

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	0	1	1	1	0	1	1	1	A	

NOTE: The WR will also reflect this new value since both registers get written to at the same time)

Example 2

Reading from the WR:

Write to the ACR first (to index the WR)

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	

Then, Set the WR address

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

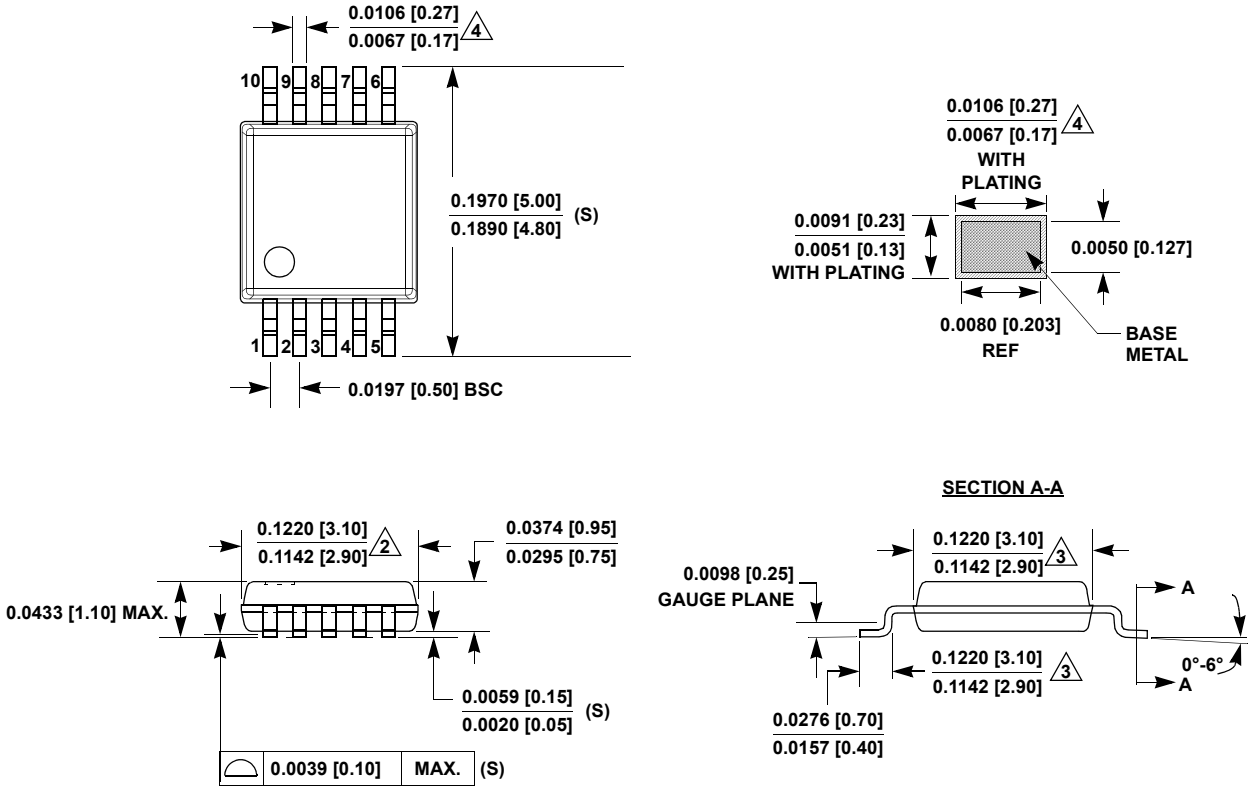
Read from the WR

	0	1	0	1	0	0	0	1	A	x	x	x	x	x	x	x	x	

NOTE: A = acknowledge, x = data bit read

MSOP Packaging Information

10 Lead MSOP, Package Code



NOTES:

1. Package dimensions conform to JEDEC specification MO-187BA.
2. 2 Does not include mold flash, protrusion or gate burrs, mold flash protrusions or gate burrs shall not exceed 0.15 mm per side.
3. 3 Does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. 4 Does not include dambar protrusion. Allowable dambar protrusion shall be 0.8 mm.
5. Lead span/stand-off height/coplanarity are considered as special characteristics.
6. Controlling dimensions in inches [mm].