Data Sheet April 12, 2007 FN6326.1

Precision, Low Noise FGA™ Voltage References

The ISL21007 FGA™ voltage references are extremely low power, high precision, and low noise voltage references fabricated on Intersil's proprietary Floating Gate Analog technology. The ISL21007 features very low noise ($4\mu V_{P-P}$ for 0.1Hz to 10Hz) and very low operating current (150µA, Max). In addition, the ISL21007 family features guaranteed initial accuracy as low as ±0.5mV.

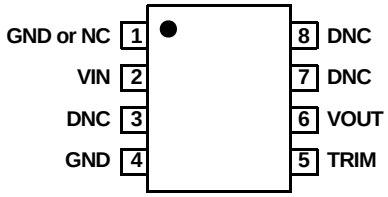
This combination of high initial accuracy, low drift, and low output noise performance of the ISL21007 enables versatile high performance control and data acquisition applications with low power consumption.

Available Options

PART NUMBER	V_{OUT} OPTION (V)	INITIAL ACCURACY (mV)	TEMPCO. (ppm/°C)
ISL21007BFB812Z	1.250	±0.5	3
ISL21007CFB812Z	1.250	±1.0	5
ISL21007DFB812Z	1.250	±2.0	10
ISL21007BFB825Z	2.500	±0.5	3
ISL21007CFB825Z	2.500	±1.0	5
ISL21007DFB825Z	2.500	±2.0	10

Pinout

ISL21007
(8 LD SOIC)
TOP VIEW



Features

- Reference Output Voltage 1.25V, 2.50V
- Initial Accuracy . . . . . .±0.5mV (B grade)
- Input Voltage Range: . . . . . 2.7V to 5.5V
- Low Output Voltage Noise . . . . . $4\mu V_{P-P}$ (0.1Hz to 10Hz)
- Supply Current . . . . . .150µA (Max)
- Temperature Coefficient . . . . . 3ppm/°C (B grade)
- Operating Temperature Range. . . . . .-40°C to +125°C
- Package . . . . . 8 Ld SOIC
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- High Resolution A/Ds and D/As
- Digital Meters
- Bar Code Scanners
- Basestations
- Battery Management/Monitoring
- Industrial/Instrumentation Equipment

Ordering Information

PART NUMBER (Note)	PART MARKING	V_{OUT} OPTION (V)	GRADE	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL21007BFB812Z	21007BF Z12	1.250	±0.5mV, 3ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007CFB812Z	21007CF Z12	1.250	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB812Z	21007DF Z12	1.250	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007BFB825Z	21007BF Z25	2.500	±0.5mV, 3ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007CFB825Z	21007CF Z25	2.500	±1.0mV, 5ppm/°C	-40 to +125	8 Ld SOIC	M8.15
ISL21007DFB825Z	21007DF Z25	2.500	±2.0mV, 10ppm/°C	-40 to +125	8 Ld SOIC	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add “-TK” suffix for tape and reel

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND or NC	Ground Connection
2	VIN	Power Supply Input Connection
4	GND	Voltage Reference Output Connection
5	TRIM	Allows user trim ±2.5%
6	VOUT	Do Not Connect; Internal Connection – Must Be Left Floating
3, 7, 8	DNC	Do Not Connect; Internal Connection - Must Be Left Floating

Typical Application Circuit

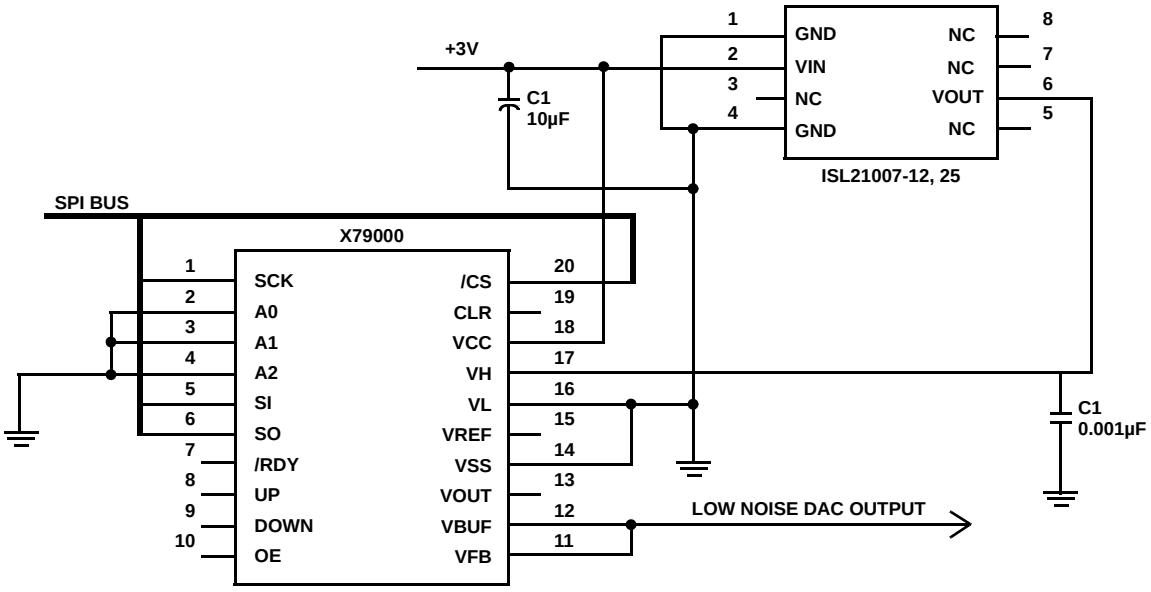


FIGURE 1. TYPICAL APPLICATION PRECISION 12-BIT SUBRANGING DAC

Absolute Voltage Ratings

Storage Temperature Range . . . . . .-65°C to +150°C
Max Voltage V_{IN} to Gnd . . . . . -0.5V to +6.5V
Max Voltage V_{OUT} to Gnd (10s). . . . . .-0.5V to V_{OUT} + 1
Voltage on “DNC” pins . . . . No connections permitted to these pins.
Lead Temperature, soldering (10s) . . . . . .+260°C
ESD Rating
Human Body Model (HBM) 6kV
Machine Model 600V
Charged Device Model (CDM) 2kV

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . .-40°C to +125°C

Thermal Information

Continuous Power Dissipation (T_A = +70°C) (Note 1)
8 Lead SOIC derate 5.88mW/°C above +70°C 471mW
Pb-free reflow profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Common Electrical Specifications (ISL21007-12, -25) T_A = -40°C to +125°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C	ISL21007B	-0.5		+0.5	mV
		ISL21007C	-1.0		+1.0	mV
		ISL21007D	-2.0		+2.0	mV
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 2)	ISL21007B			3	ppm/°C
		ISL21007C			5	ppm/°C
		ISL21007D			10	ppm/°C
I_{IN}	Supply Current			75	150	µA
$\Delta V_{OUT}/\Delta t$	Long Term Stability (Note 4)	T_A = +25°C		TBD		ppm/$\sqrt{1kHrs}$
	Trim Range		±2.0	±2.5		%
t_R	Turn on Settling Time	V_{OUT} = ±0.1%		120		µs
	Ripple Rejection	f = 10kHz		60		dB
e_N	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz		4		μV_{P-P}
V_N	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz		2.2		μV_{RMS}
	Noise Density	f = 1kHz		60		nV/$\sqrt{Hz}$

Electrical Specifications (ISL21007-12, V_{OUT} = 1.250V) V_{IN} = 3.0V, T_A = -40°C to +125°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage			1.250		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	2.7V ≤ V_{IN} ≤ 5.5V		100	700	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 7mA		10	100	µV/mA
		Sinking: -7mA ≤ I_{OUT} ≤ 0mA		20	150	µV/mA
I_{SC}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		40		mA
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 3)	ΔT_A = +165°C		50		ppm

Electrical Specifications (ISL21007-25, V_{OUT} = 2.50V) V_{IN} = 3.0V, T_A = -40°C to +125°C, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage			2.500		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	2.7V ≤ V_{IN} ≤ 5.5V		50	200	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 5mA		10	100	µV/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA		20	150	µV/mA
I_{SC}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		50		mA
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 3)	ΔT_A = +165°C		50		ppm

NOTES:

2. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -40°C to +125°C = +165°C.
3. Thermal Hysteresis is the change of V_{OUT} measured @ T_A = +25°C after temperature cycling over a specified range, ΔT_A. V_{OUT} is read initially at T_A = +25°C for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at +25°C. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For ΔT_A = +165°C, the device under test is cycled from +25°C to +125°C to -40°C to +25°C.
4. FGA voltage reference long term drift is a logarithmic characteristic. Changes that occur after the first few hundred hours of operation are significantly smaller with time, asymptotically approaching zero beyond 1,000 hours. Because of this decreasing characteristics, long term drift is specified in ppm/$\sqrt{1kHrs}$.

Typical Performance Curves (ISL21007-12) (R_{EXT} = 100kΩ)

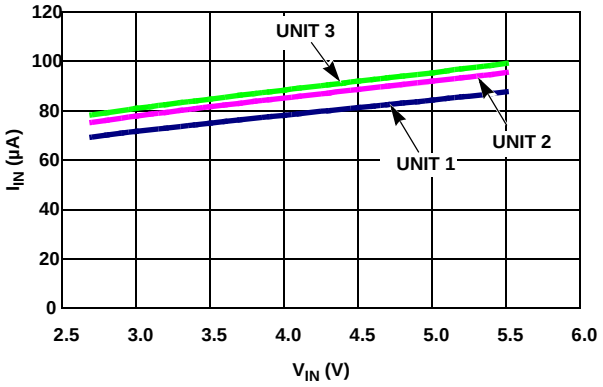


FIGURE 2. I_{IN} vs V_{IN} (3 UNITS)

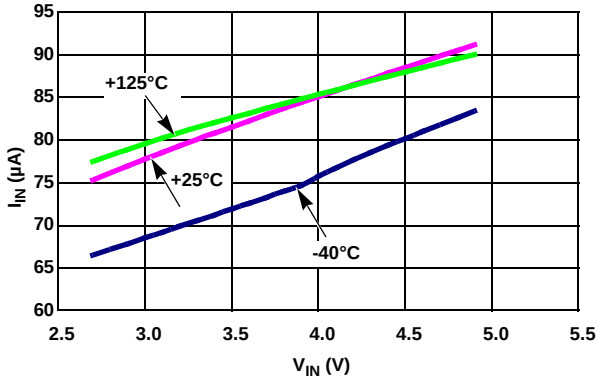


FIGURE 3. I_{IN} vs V_{IN} OVER TEMPERATURE

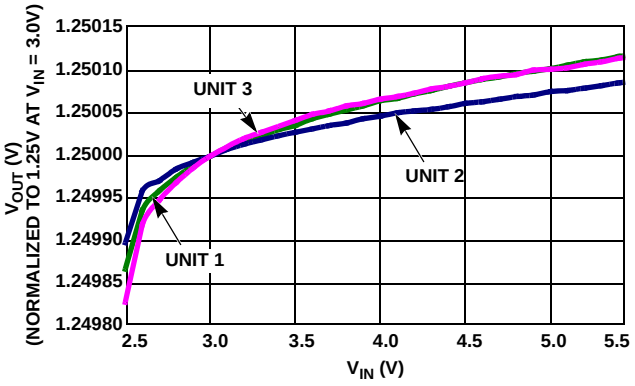


FIGURE 4. LINE REGULATION (3 UNITS)

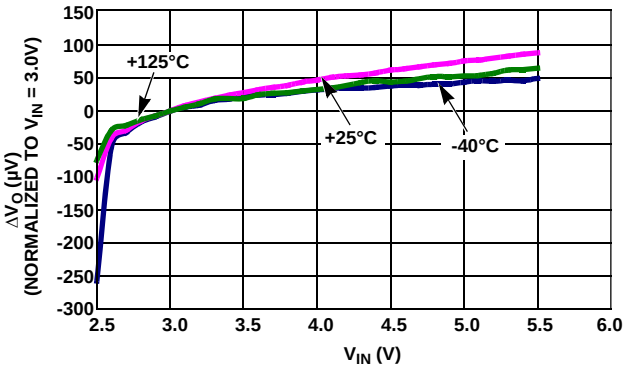


FIGURE 5. LINE REGULATION OVER TEMPERATURE

Typical Performance Curves (ISL21007-12) (R_{EXT} = 100kΩ) (Continued)

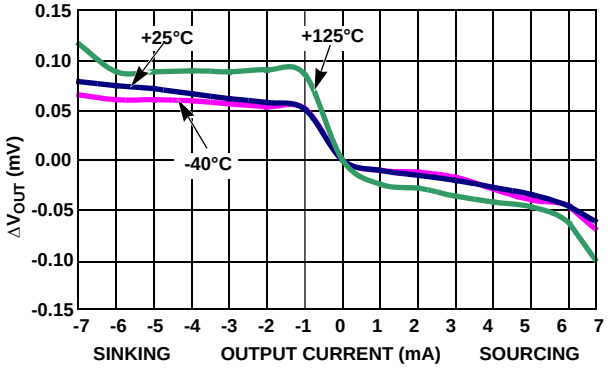


FIGURE 6. LOAD REGULATION OVER TEMPERATURE

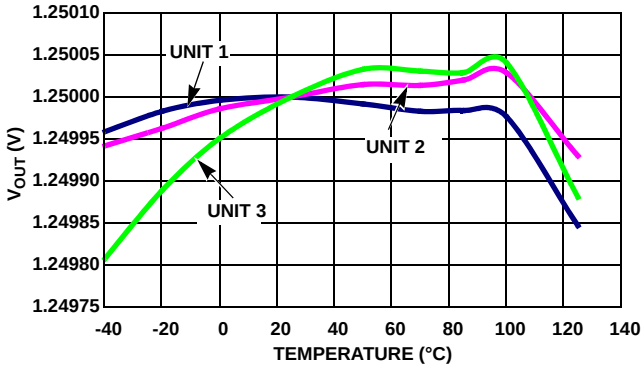


FIGURE 7. V_{OUT} vs TEMPERATURE (3 UNITS)

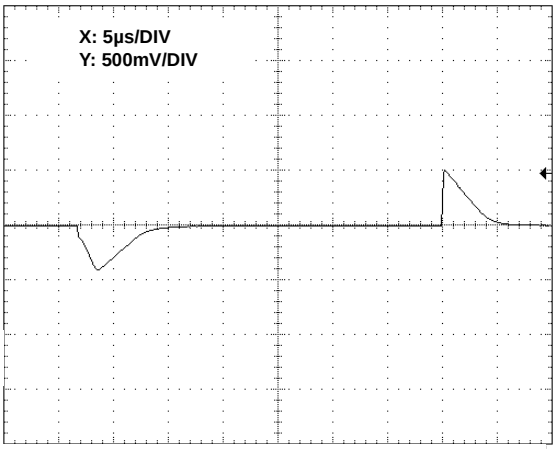


FIGURE 8. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

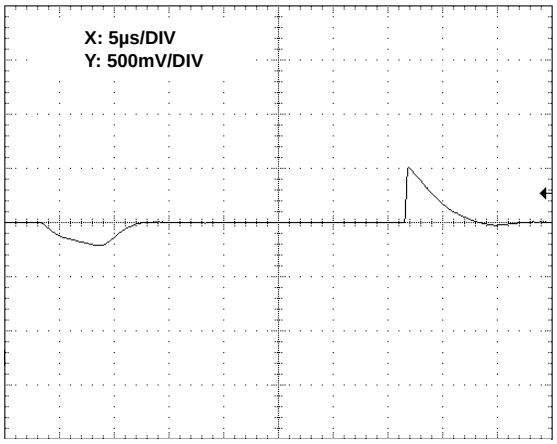


FIGURE 9. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

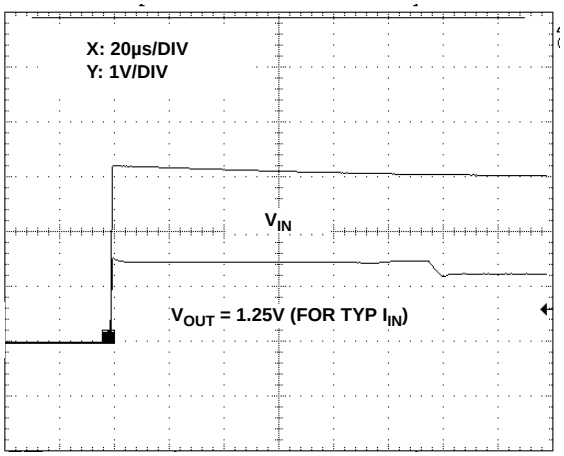


FIGURE 10. TURN ON TIME

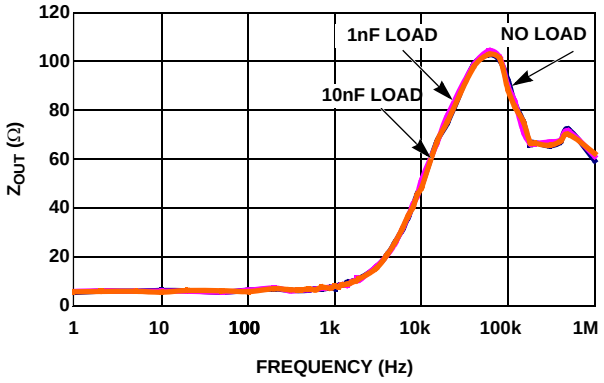


FIGURE 11. Z_{OUT} vs FREQUENCY

Typical Performance Curves (ISL21007-12) (R_{EXT} = 100kΩ) (Continued)

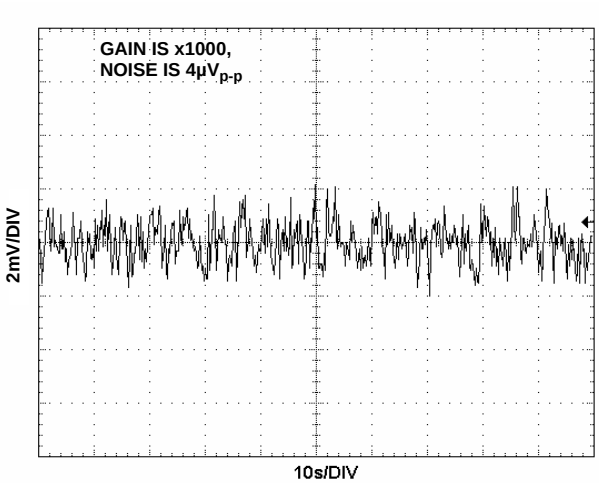


FIGURE 12. V_{OUT} NOISE, 0.1Hz to 10Hz

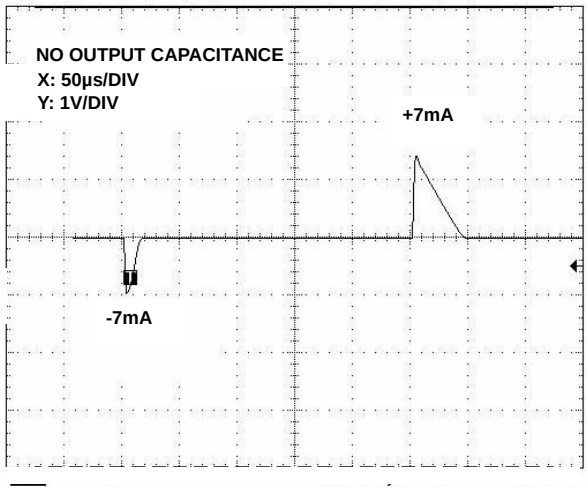


FIGURE 13. LOAD TRANSIENT RESPONSE

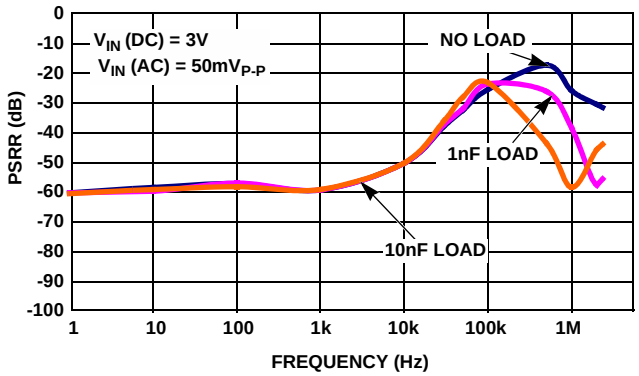


FIGURE 14. PSRR vs CAPACITIVE LOADS

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ)

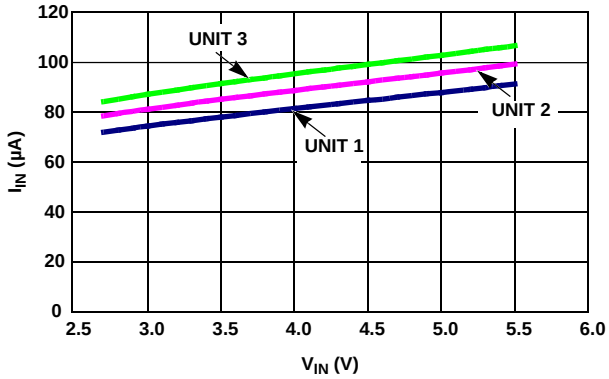


FIGURE 15. I_{IN} vs V_{IN} (3 UNITS)

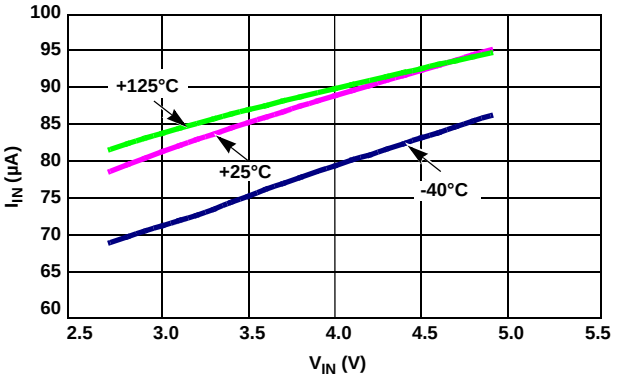


FIGURE 16. I_{IN} vs V_{IN} OVER TEMPERATURE

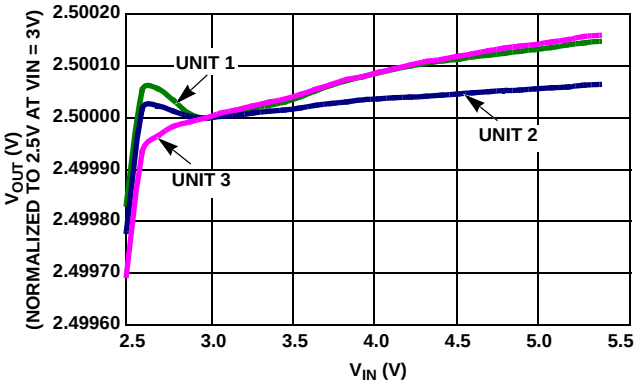


FIGURE 17. LINE REGULATION (3 UNITS)

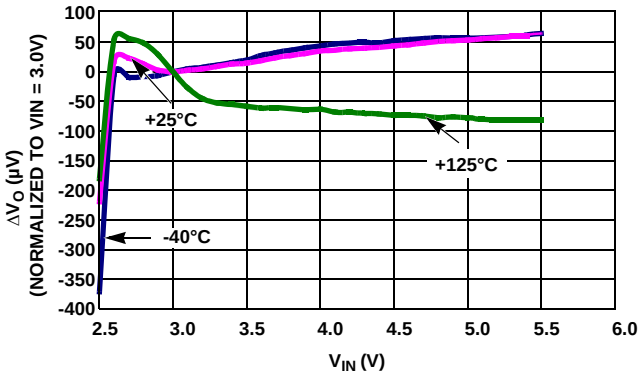


FIGURE 18. LINE REGULATION OVER TEMPERATURE

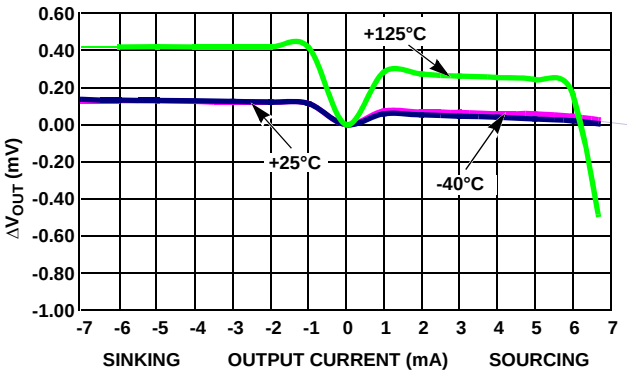


FIGURE 19. LOAD REGULATION OVER TEMPERATURE

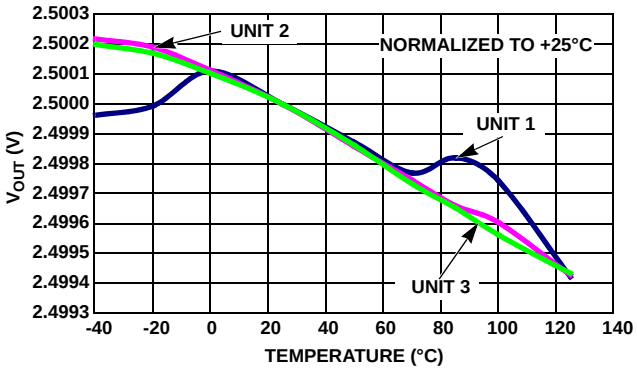


FIGURE 20. V_{OUT} vs TEMPERATURE (3 UNITS)

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ) (Continued)

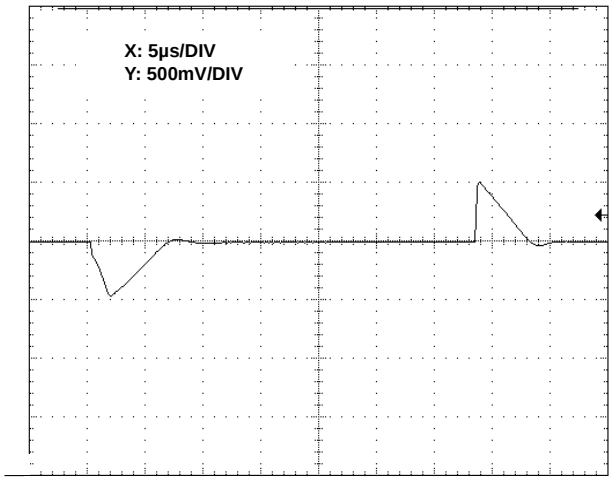


FIGURE 21. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

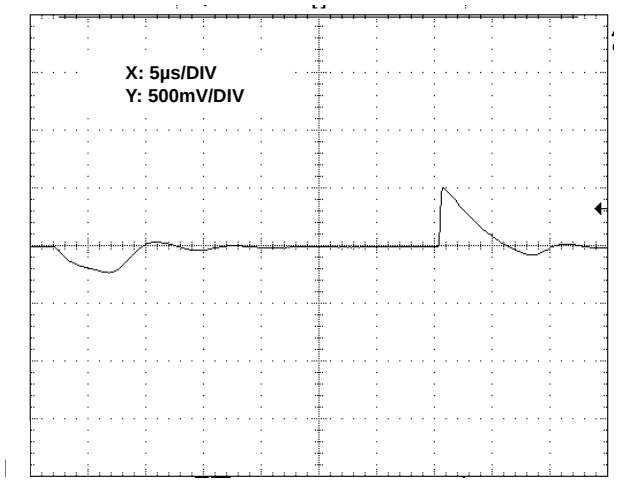


FIGURE 22. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

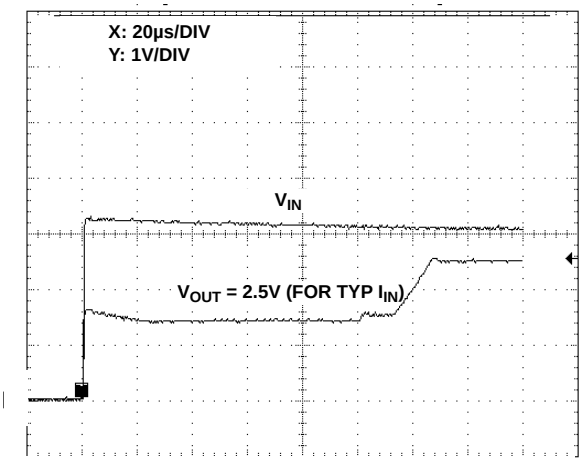


FIGURE 23. TURN ON TIME

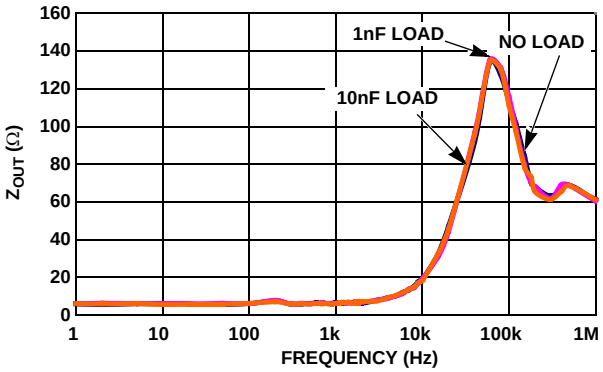


FIGURE 24. Z_{OUT} vs FREQUENCY

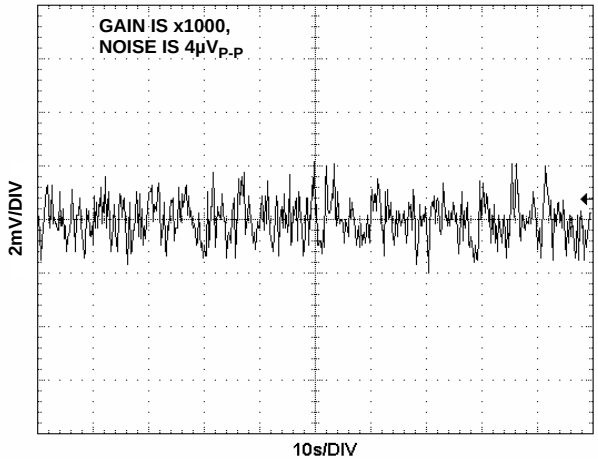


FIGURE 25. V_{OUT} NOISE, 0.1Hz to 10Hz

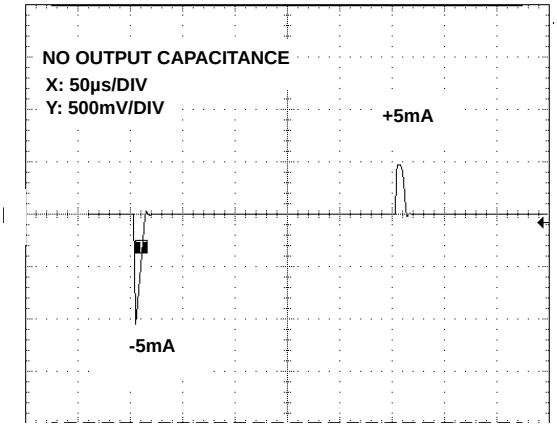


FIGURE 26. LOAD TRANSIENT RESPONSE

Typical Performance Curves (ISL21007-25) (R_{EXT} = 100kΩ) (Continued)

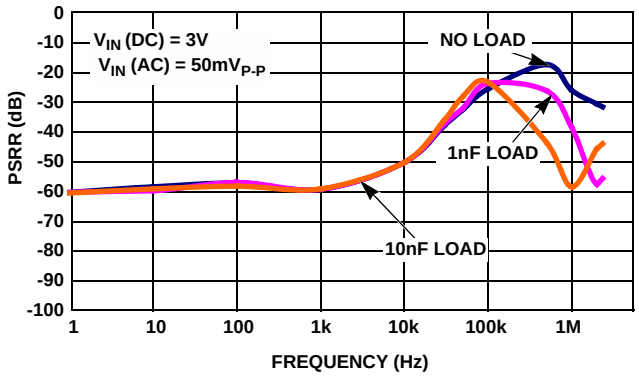


FIGURE 27. PSRR vs CAPACITIVE LOADS

Applications Information

FGA Technology

The ISL21007 voltage reference uses floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Micropower Operation

The ISL21007 consumes extremely low supply current due to the proprietary FGA technology. Low noise performance is achieved using optimized biasing techniques. Supply current is typically 75µA and noise is 4µV_{P-P} benefitting precision, low noise portable applications such as handheld meters and instruments.

Data Converters in particular can utilized the ISL21007 as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a plastic SOIC package which will subject the die to mild stresses when the PC board is heated and cooled and slightly changes shape. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to these die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Mounting the device in a cutout also minimizes flex. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 4µV_{P-P}. The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately 40µV_{P-P} with no capacitance on the output. This noise measurement is made with a 2 decade bandpass filter made of a 1 pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10 times the center frequency. Load capacitance up to 1000pF can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21007 is not designed to drive heavily capactive loads, so for load capacitances above 0.001µF the noise reduction network shown in Figure 28 is recommended. This network reduces noise significantly over the full bandwidth. Noise is reduced to less than 20µV_{P-P} from 1Hz to 1MHz using this network with a 0.01µF capacitor and a 2kΩ resistor in series with a 10µF capacitor. Also, transient response is improved with higher value output capacitor. The

0.01µF value can be increased for better load transient response with little sacrifice in output stability.

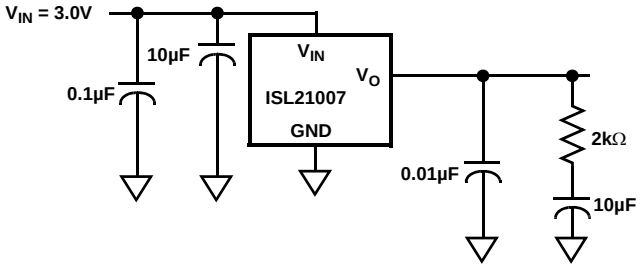


FIGURE 28. HANDLING HIGH LOAD CAPACITANCE

Turn-On Time

The ISL21007 devices have low supply current and thus the time to bias up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically 120µs. This is shown in Figure 10. Circuit design must take this into account when looking at power up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} – V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} – T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted up or down by 2.5% by placing a potentiometer from Vout to ground, and connecting the wiper to the TRIM pin. The TRIM input is high impedance, so no series resistance is needed. The resistor in the potentiometer should be a low tempco (<50ppm/°C) and the resulting voltage divider should have very low tempco <5ppm/°C. A digital potentiometer such as the ISL95810 provides a low tempco resistance and excellent resistor and tempco matching for trim applications.

Typical Application Circuits

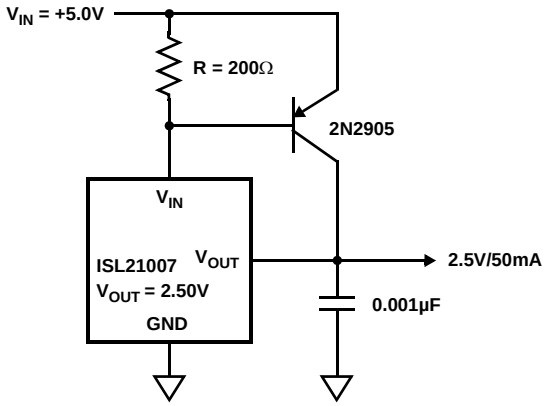


FIGURE 29. PRECISION 2.5V 50mA REFERENCE

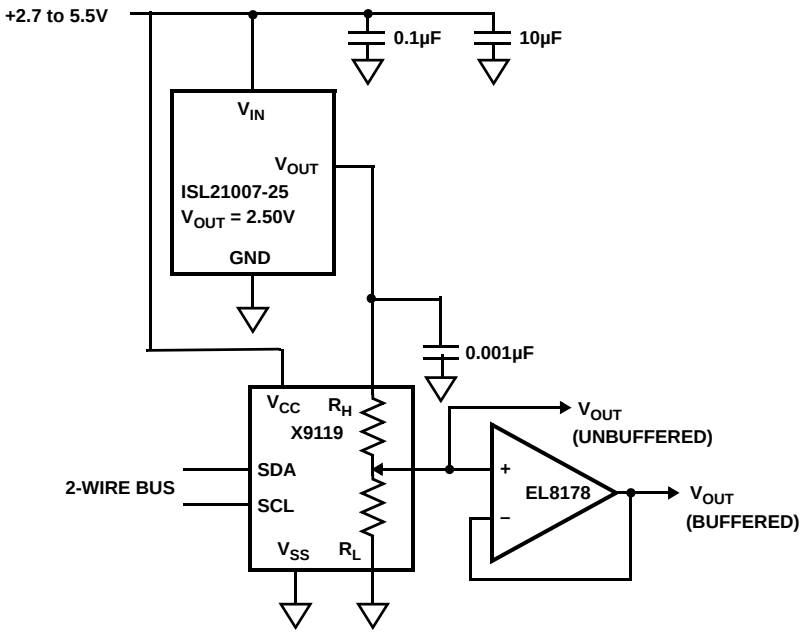


FIGURE 30. 2.5V FULL SCALE LOW-DRIFT, LOW NOISE, 10-BIT ADJUSTABLE VOLTAGE SOURCE

Typical Application Circuits

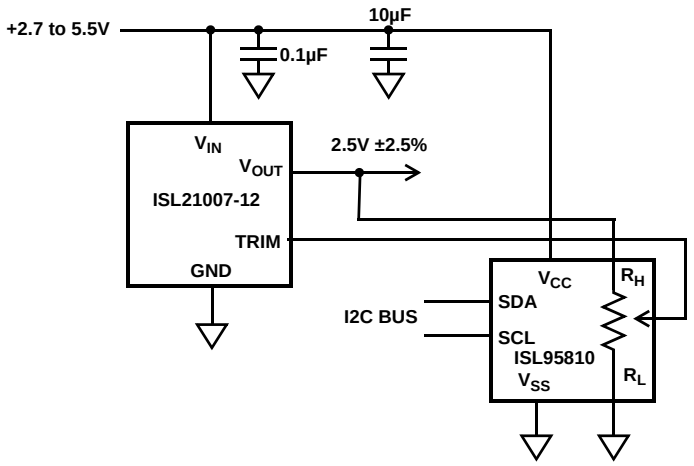


FIGURE 31. OUTPUT ADJUSTMENT USING THE TRIM PIN

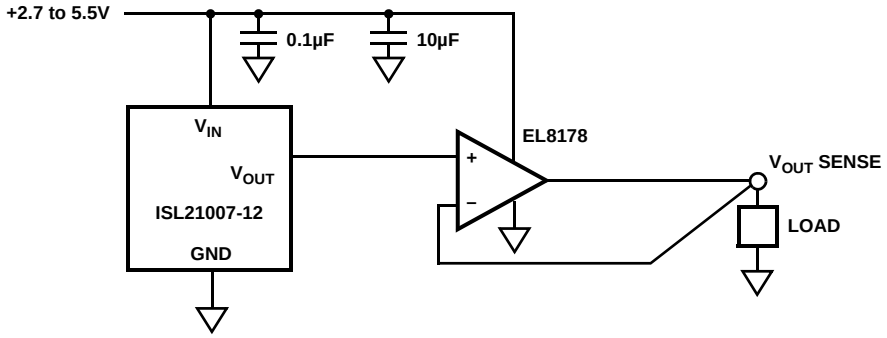
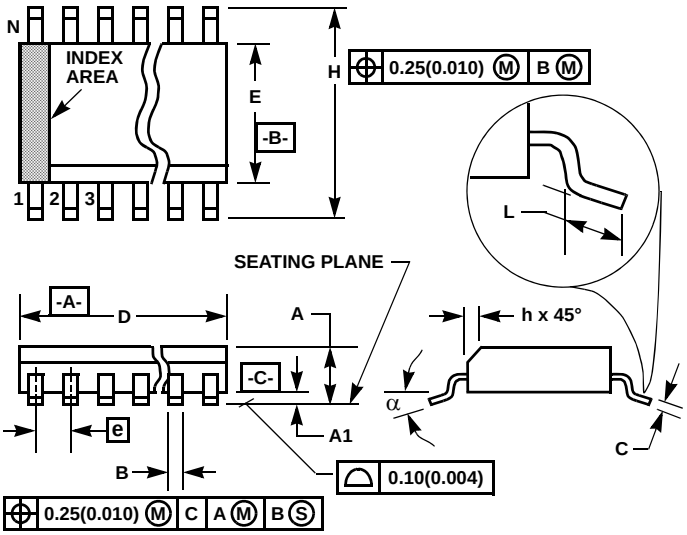


FIGURE 32. KELVIN SENSED LOAD

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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