PRELIMINARY | Data Sheet | February 21, 2006 | FN6113.0

-52V Dual Channel Differential DSL Line Driver

The ISL1540 is a -52V dual channel differential amplifier designed for driving full rate ADSL signals at very low power dissipation. The high supply voltage allows operation from a single standard -52V negative battery supply. It contains two pairs of wideband, high voltage, current mode feedback amplifiers optimized for lower power consumption and highest performance in ADSL and ADSL2+ systems. The line drivers have fixed gain A_V = 48 with integrated feedback and gain resistors. Its output clamping circuit eliminates the requirement for the Zener protection diodes.

These drivers achieve an MTPR distortion measurement of better than 70dB while consuming typically 3mA per DSL channel of total supply current.

The ISL1540 is supplied in a thermally-enhanced 8mm x 8mm 32-pin QFN package and is specified for operating over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
ISL1540IR	1540IR	32-Pin QFN (8mm x 8mm)	-	MDP0046
ISL1540IR-T7	1540IR	32-Pin QFN (8mm x 8mm)	7”	MDP0046
ISL1540IR-T13	1540IR	32-Pin QFN (8mm x 8mm)	13”	MDP0046
ISL1540IRZ (See Note)	1540IRZ	32-Pin QFN (8mm x 8mm) (Pb-Free)	-	MDP0046
ISL1540IRZ-T7 (See Note)	1540IRZ	32-Pin QFN (8mm x 8mm) (Pb-Free)	7”	MDP0046
ISL1540IRZ-T13 (See Note)	1540IRZ	32-Pin QFN (8mm x 8mm) (Pb-Free)	13”	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

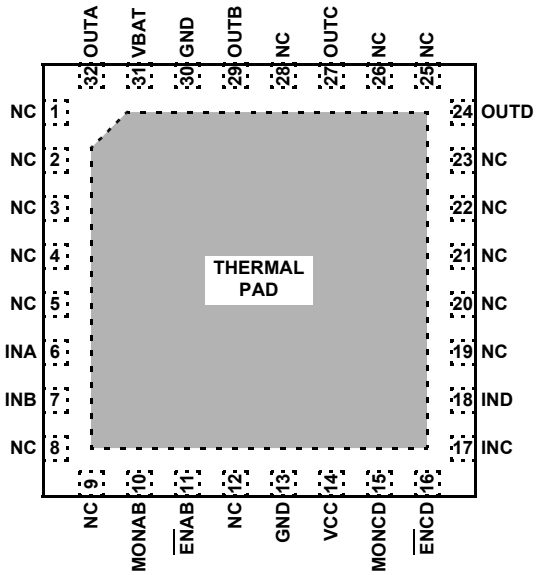
- 200mA output current driving capability
- Operates from a single -40V to -60V power supply
- 800mW per channel total power dissipation
- MTPR of -70dB
- 96V_{P-P} differential output swing
- Fixed gain, integrated gain resistors
- Current control pins
- Output clamp for lightning and surge protection
- Channel separation
  - 75dB @ 1MHz
- Pb-free plus anneal available (RoHS compliant)

Applications

- Dual port ADSL and ADSL2+ line drivers
- HDSL, HDSL2, HDSL 4 and SHDSL line drivers
- DSLAM, DLC, MDU/MTU line drivers
- Performance upgrade to Le87213 and Le87213A

Pinout

ISL1540
[32-PIN QFN (8mm x 8mm)]
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Voltage to GND . . . . . -0.3V to 6.0V
V_{BAT} Voltage to GND. . . . . -65V to 0.3V
Driver V_{IN}+ Voltage . . . . . V_{BAT} to 0.0V
ENA Voltage to GND . . . . . -0.3V to V_{CC}
I_{ADJ} Voltage to GND . . . . . -0.3V to V_{CC}-2V

Current into any Input 8mA
Output Current from Driver (Static) 50mA
Power Dissipation . . . . . See Curves
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Specifications

V_{BAT} = -52V, R_F = 10kΩ, R_L = 300Ω, V_{CC} = 3.3V, I_{ADJ} = $\overline{EN}$ = 0V, T_A = 25°C. Amplifiers tested separately.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{BAT} (Full I_S)	Negative Supply Current per Amplifier	All outputs at 0V, $\overline{EN}$ = 0V		-3		mA
I_{BAT} (Power-down)	Negative Supply Current per Amplifier	All outputs at 0V, $\overline{EN}$ = 3.3V		50		µA
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-50	+10	+50	mV
ΔV_{OS}	V_{OS} Mismatch		-5	1	+5	mV
I_B+	Non-Inverting Input Bias Current		-15		+14	µA
I_B-	Inverting Input Bias Current		-30		+30	µA
ΔI_B-	I_B- Mismatch		-25	0	+25	µA
R_{OL}	Transimpedance		TBD	TBD	TBD	MΩ
e_N	Input Noise Voltage			TBD		nV/√Hz
i_N	-Input Noise Current			TBD		pA/√Hz
V_{IH}	Input High Voltage	$\overline{EN}$ & MON inputs, with signal	2			V
V_{IL}	Input Low Voltage	$\overline{EN}$ & MON inputs			0.8	V
I_{IH1}	Input High Current for MON	MON = 3.3V	0.05	0.25	5	µA
I_{IH0}	Input High Current for $\overline{EN}$	$\overline{EN}$ = 3.3V	0.05	0.5	5	µA
I_{IL}	Input Low Current for C_0 or MON	$\overline{EN}$ = 0V, MON = 0V	-0.3	0	+0.3	µA
OUTPUT CHARACTERISTICS						
$V_{OUT\text{-}Headroom}$	Loaded Output Headroom (R_L Single-ended to GND) V_{BAT} - V_{OUT}	R_L = 300Ω		1.5		V
		R_L = 100Ω (+)		2.3		V
		R_L = 100Ω (-)		3.4		V
I_{OL}	Linear Output Current	A_V = 5, R_L = 100Ω, f = 100kHz, THD = -60dBc (10Ω single-ended)		200		mA
I_{OUT}	Output Current	V_{OUT} = 1V, R_L = 1Ω		1		A
DYNAMIC PERFORMANCE						
A_V	Gain 25kHz to 4MHz			48		V/V
BW	-3dB Bandwidth	A_V = +48		14		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 300Ω, V_{OUT} = $2V_{P\text{-}P}$		TBD		dBc
		f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{P\text{-}P}$		TBD		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 300Ω, V_{OUT} = $2V_{P\text{-}P}$		TBD		dBc
		f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{P\text{-}P}$		TBD		dBc

Electrical Specifications

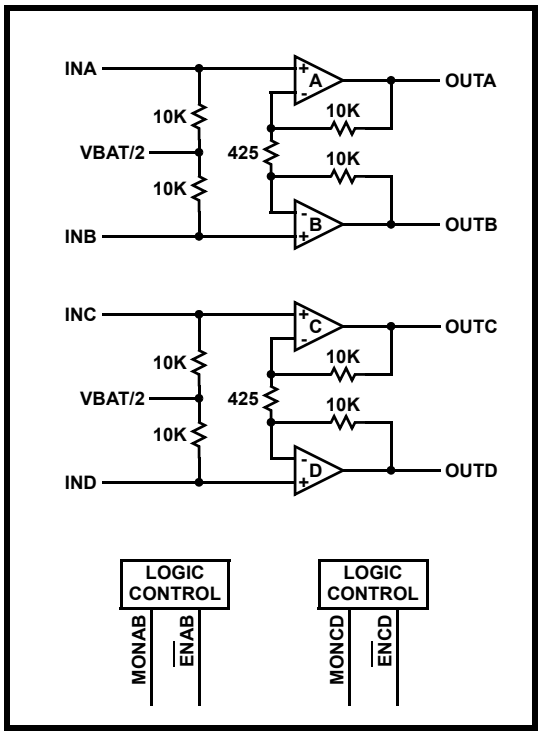
V_{BAT} = -52V, R_F = 10kΩ, R_L = 300Ω, V_{CC} = 3.3V, I_{ADJ} = $\overline{EN}$ = 0V, T_A = 25°C. Amplifiers tested separately.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
MTPR	Multi-Tone Power Ratio	26kHz to 1.1MHz, R_{LINE} = 600Ω, P_{LINE} = 20.4dBM		-70		dBc
SR	Slewrate (single-ended)	V_{OUT} from -24V to +24V measured at ±12V		750		V/µs

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1, 2, 3, 4, 5, 8, 9, 12, 19, 20, 21, 22, 23, 25, 26, 28	NC	Not connected
6	INA	Input A
7	INB	Input B
10	MONAB	Full bias/half bias current control for AB amps
11	$\overline{EN}$AB	Enable/disable for AB amps
13, 30	GND	Ground
14	VCC	3.3V supply for bias and logic
15	MONCD	Full bias/half bias current control for CD amps
16	$\overline{EN}$CD	Enable/disable for CD amps
17	INC	Input C
18	IND	Input D
24	OUTD	Output D
27	OUTC	Output C
29	OUTB	Output B
31	VBAT	-52 battery voltage
32	OUTA	Output A

Block Diagram



Typical Performance Curves

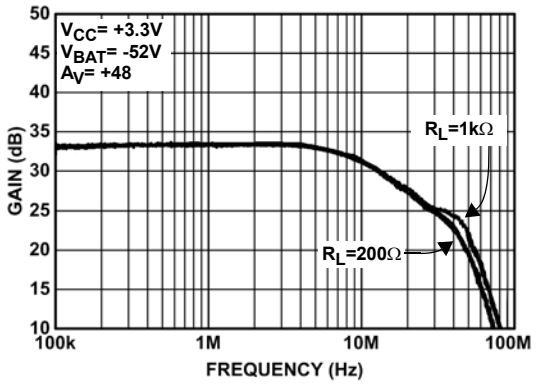


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_L

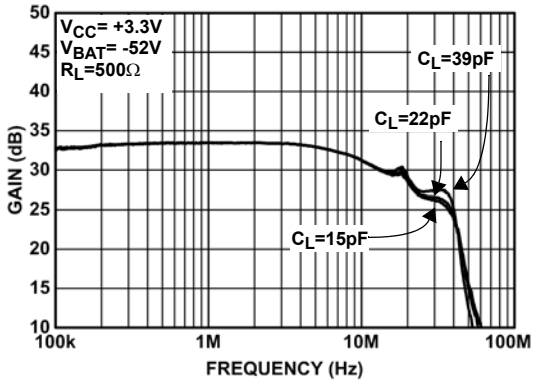


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_L (EACH OUTPUTS TO GROUND)

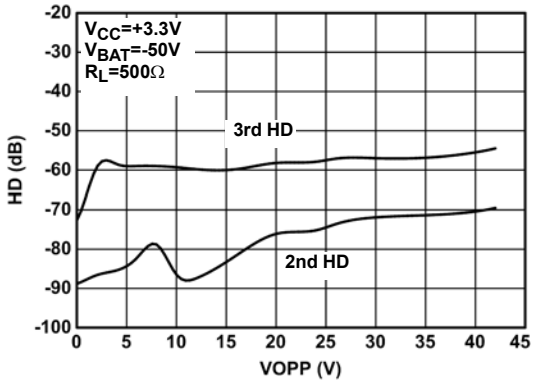


FIGURE 3. 1MHz 2nd & 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE

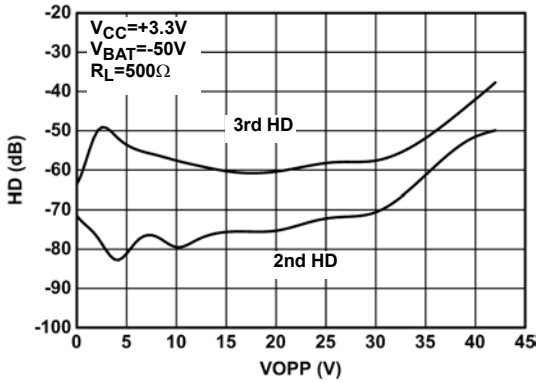


FIGURE 4. 2.2MHz 2nd & 3rd HARMONIC DISTORTION vs OUPUT VOLTAGE

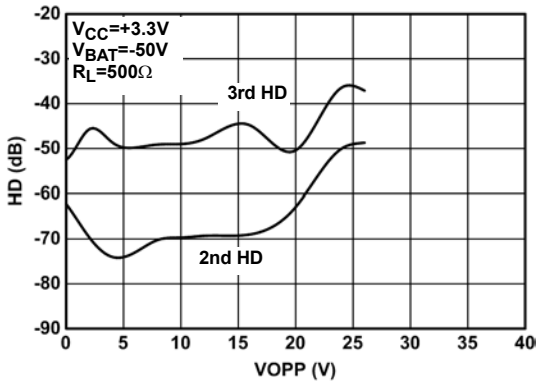


FIGURE 5. 3.75MHz 2nd & 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE

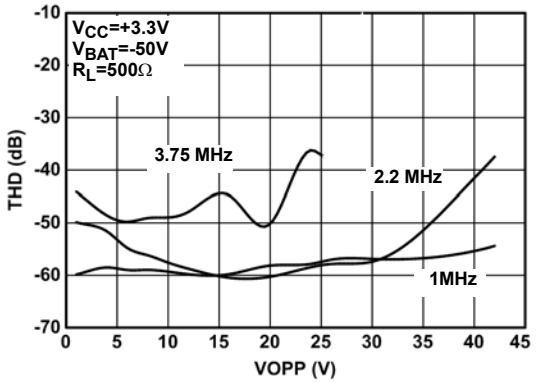


FIGURE 6. TOTAL HARMONIC DISTORTION FOR VARIOUS FREQUENCIES

Typical Performance Curves (Continued)

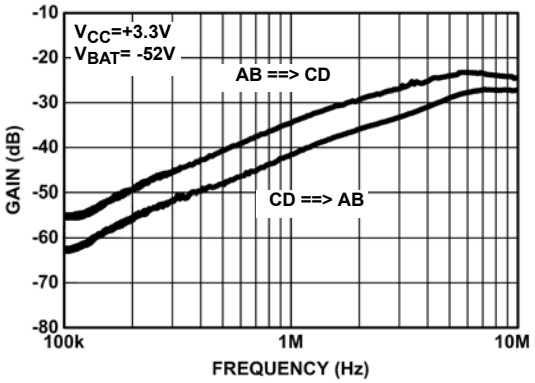


FIGURE 7. CROSSTALK vs FREQUENCY

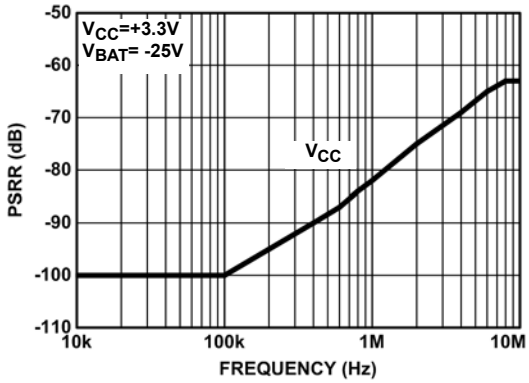


FIGURE 8. PSRR vs FREQUENCY

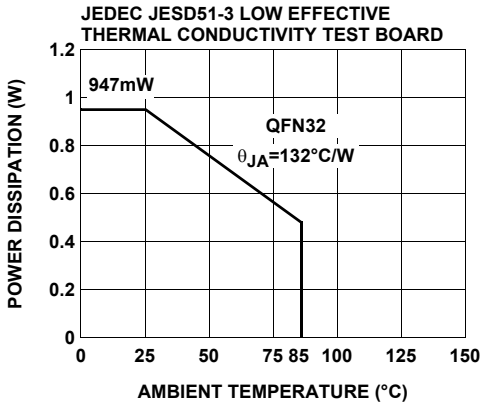


FIGURE 9. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

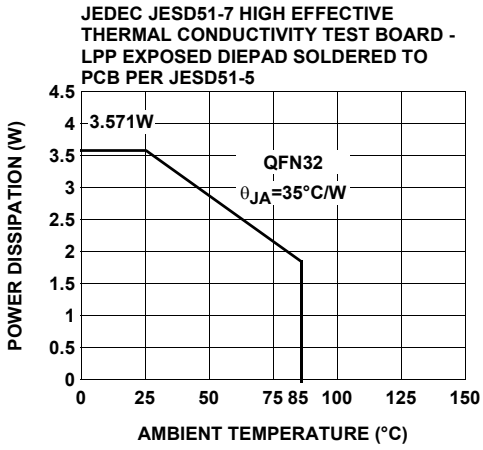


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Application Information

PCB Layout Considerations for QFN Package

The ISL1540 die is packaged in a thermally efficient 32-pins QFN leadless plastic package (8mm x 8mm). A thermal pad is underneath the package and can use PCB surface metal vias areas and internal ground planes to spread heat away from the package. The larger the PCB area, the lower the junction temperature of the device will be. In ADSL applications, multiple layer circuit boards with internal ground plane are generally used. 13 mil vias are recommended to connect the metal area under the device with internal ground plane.

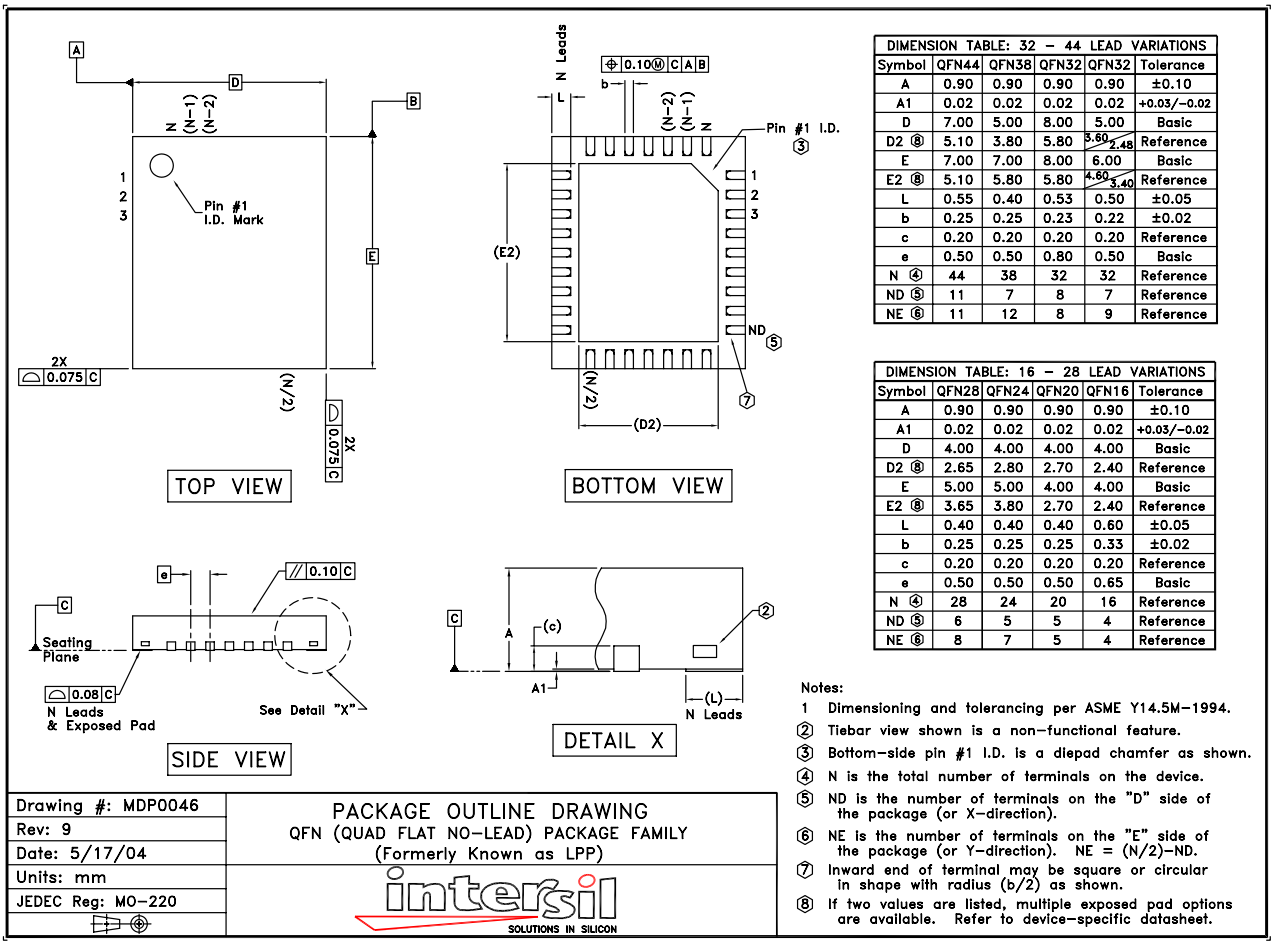
Power Control Function

The ISL1540 contains four forms of power control operation. The two inputs, MON1 and MON2, can be used to control the supply current of the ISL1540 drive amplifiers. ENAB and ENCD can be used to enable and disable the device. Below is the table showing the power modes.

TABLE 1. POWER MODES FOR ISL1541

MON1	MON2	ENAB	ENCD	OPERATION
0	0	0	0	I_S Full Power Mode
1	1	0	0	1/2-I_S Power Mode
X	X	1	1	Power Down

Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32	QFN32	Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (5)	11	7	8	7	Reference
NE (6)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS					
Symbol	QFN28	QFN24	QFN20	QFN16	Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	2.70	2.40	Reference
E	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	2.70	2.40	Reference
L	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.50	0.65	Basic
N (4)	28	24	20	16	Reference
ND (5)	6	5	5	4	Reference
NE (6)	8	7	5	4	Reference

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. ND is the number of terminals on the "D" side of the package (or X–direction).
6. NE is the number of terminals on the "E" side of the package (or Y–direction). NE = (N/2)–ND.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING
Rev: 9	QFN (QUAD FLAT NO–LEAD) PACKAGE FAMILY
Date: 5/17/04	(Formerly Known as LPP)
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO–220	