

## Radiation Hardened Quad Differential Line Receiver

The Intersil HS-26C32RH is a differential line receiver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26C32RH has an input sensitivity typically of 200mV over the common mode input voltage range of  $\pm 7V$ . The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four receivers.

**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.**

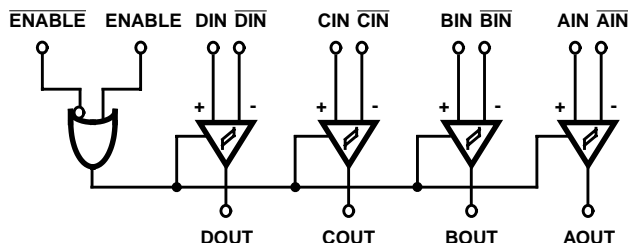
Detailed Electrical Specifications for these devices are contained in SMD 5962-95689. A "hot-link" is provided on our homepage for downloading.

[www.intersil.com/spacedefense/space.asp](http://www.intersil.com/spacedefense/space.asp)

## Ordering Information

ORDERING NO.	INTERNAL MKT. NO.	TEMP. RANGE (°C)
5962F9568901QEC	HS1-26C32RH-8	-55 to 125
5962F9568901QXC	HS9-26C32RH-8	-55 to 125
5962F9568901V9A	HS0-26C32RH-Q	25
5962F9568901VEC	HS1-26C32RH-Q	-55 to 125
5962F9568901VXC	HS9-26C32RH-Q	-55 to 125
HS1-26C32RH/PROTO	HS1-26C32RH/PROTO	-55 to 125
HS9-26C32RH/PROTO	HS9-26C32RH/PROTO	-55 to 125

## Logic Diagram

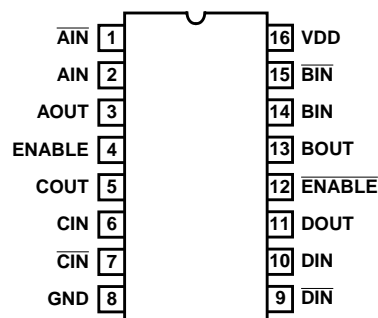


## Features

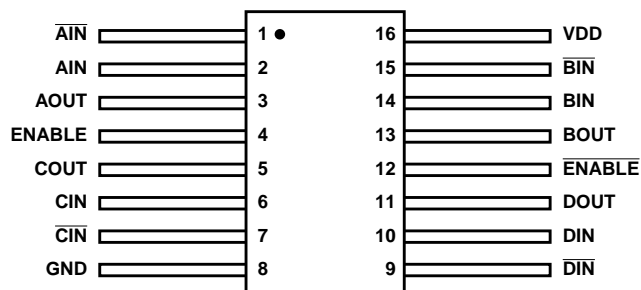
- Electrically Screened to SMD # 5962-95689
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
  - Total Dose . . . . . 300 krad(Si) (Max)
- Latchup Free
- EIA RS-422 Compatible Inputs
- CMOS Compatible Outputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to 125°C Military Temperature Range

## Pinouts

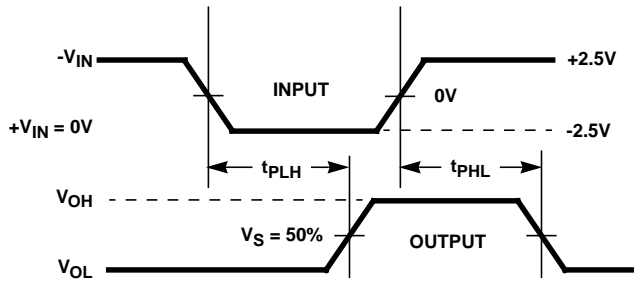
HS1-26C32RH 16 LEAD CERAMIC SIDEBRAZE DIP  
MIL-STD-1835: CDIP2-T16  
TOP VIEW



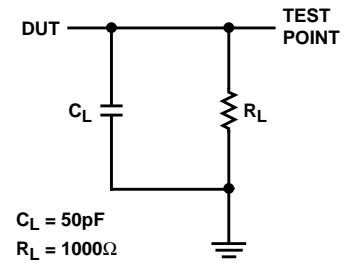
HS9-26C32RH 16 LEAD FLATPACK  
MIL-STD-1835: CDFP4-F16  
TOP VIEW



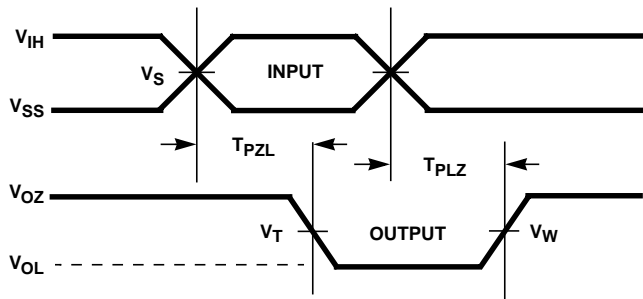
### Propagation Delay Timing Diagram



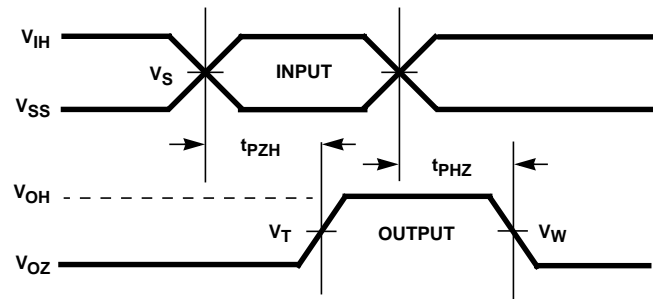
### Propagation Delay Load Circuit



### Three-State Low Timing Diagram



### Three-State High Timing Diagrams



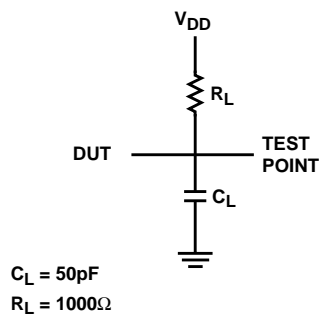
THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26C32RH	UNITS
$V_{DD}$	4.50	V
$V_{IH}$	4.50	V
$V_S$	2.25	V
$V_T$	50	%
$V_W$	$V_{OL} + 0.5$	V
GND	0	V

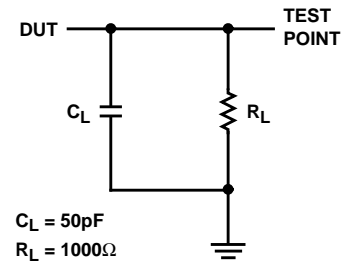
THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26C32RH	UNITS
$V_{DD}$	4.50	V
$V_{IH}$	4.50	V
$V_S$	2.25	V
$V_T$	50	%
$V_W$	$V_{OH} - 0.5$	V
GND	0	V

### Three-State Low Load Circuit



### Three-State High Load Circuit



## Die Characteristics

### DIE DIMENSIONS:

84 mils x 130 mils  
(2140 $\mu$ m x 3290 $\mu$ m)

### INTERFACE MATERIALS:

#### Glassivation:

Type: SiO<sub>2</sub>  
Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

### Top Metallization:

M1: Mo/TiW  
Thickness: 5800 $\text{\AA}$   
M2: Al/Si/Cu  
Thickness: 5800 $\text{\AA}$

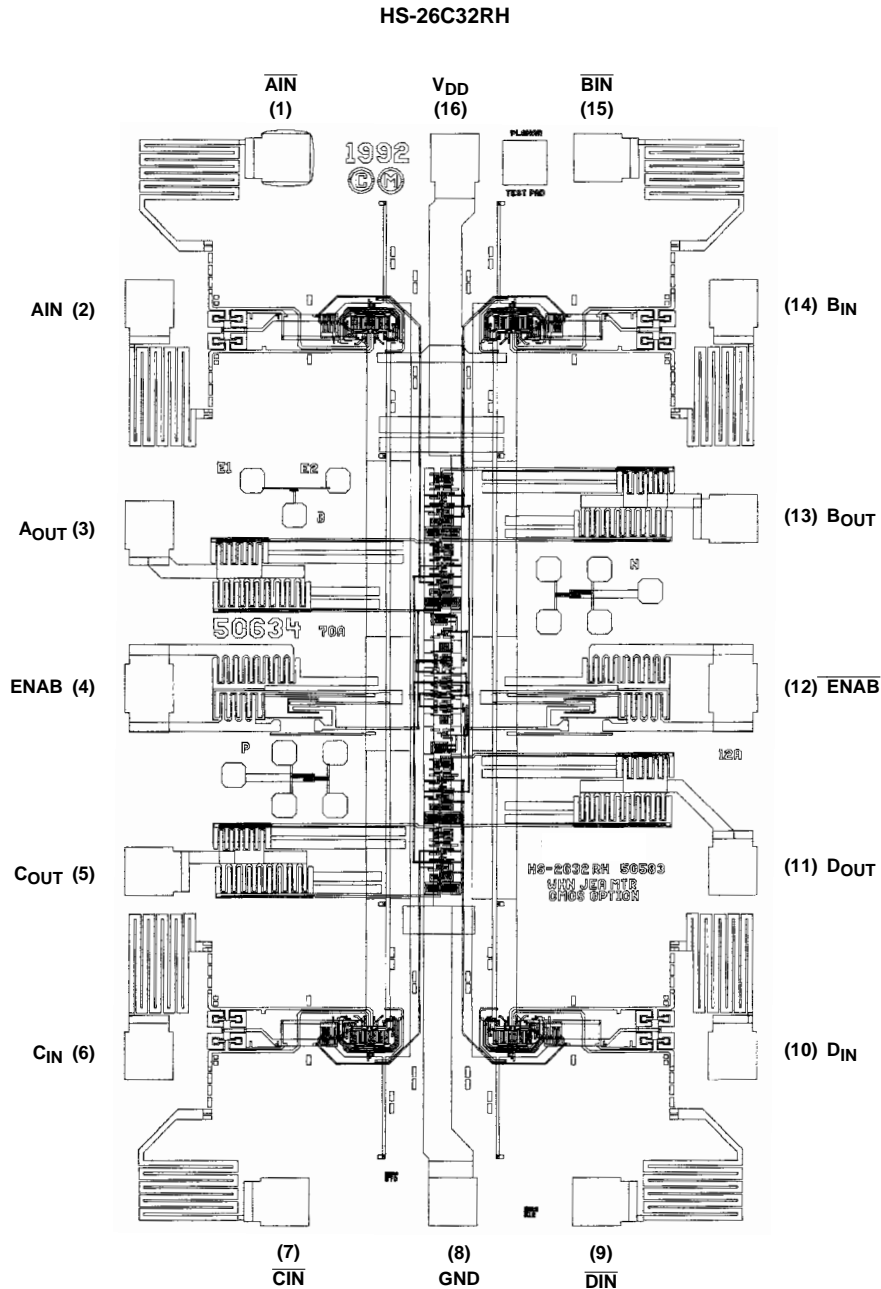
### Worst Case Current Density:

$<2.0 \times 10^5 \text{A/cm}^2$

### Bond Pad Size:

110 $\mu$ m x 100 $\mu$ m

## Metallization Mask Layout



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