

September 1995

## Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm<sup>2</sup>/mg
- Single Event Upset (SEU) Immunity < 2 x 10<sup>-9</sup> Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10<sup>12</sup> RAD (Si)/s
- Dose Rate Upset >10<sup>10</sup> RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

## Description

The Intersil HCTS193MS is a Radiation Hardened 4-bit binary UP/DOWN synchronous counter.

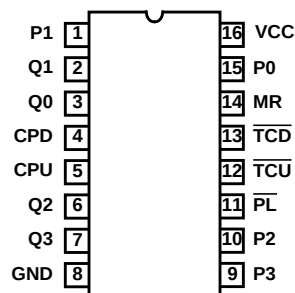
Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the asynchronous parallel load input (PL). The counter is incremented on the low to high transition of the clock-up input (high on the clock-down), decremented on the low to high transition of the clock-down input (high on the clock-up). A high level on the MR input overrides any other input to clear the counter to zero. The Terminal Count Up goes low half a clock period before the zero count is reached and returns high at the maximum count. The Terminal Count Down mode goes low half a clock period before the maximum count and returns high at the maximum count.

The HCTS193MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

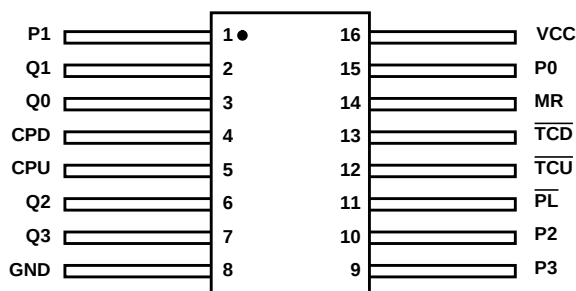
The HCTS193MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

## Pinouts

16 LEAD CERAMIC DUAL-IN-LINE  
METAL SEAL PACKAGE (SBDIP)  
MIL-STD-1835 CDIP2-T16  
TOP VIEW



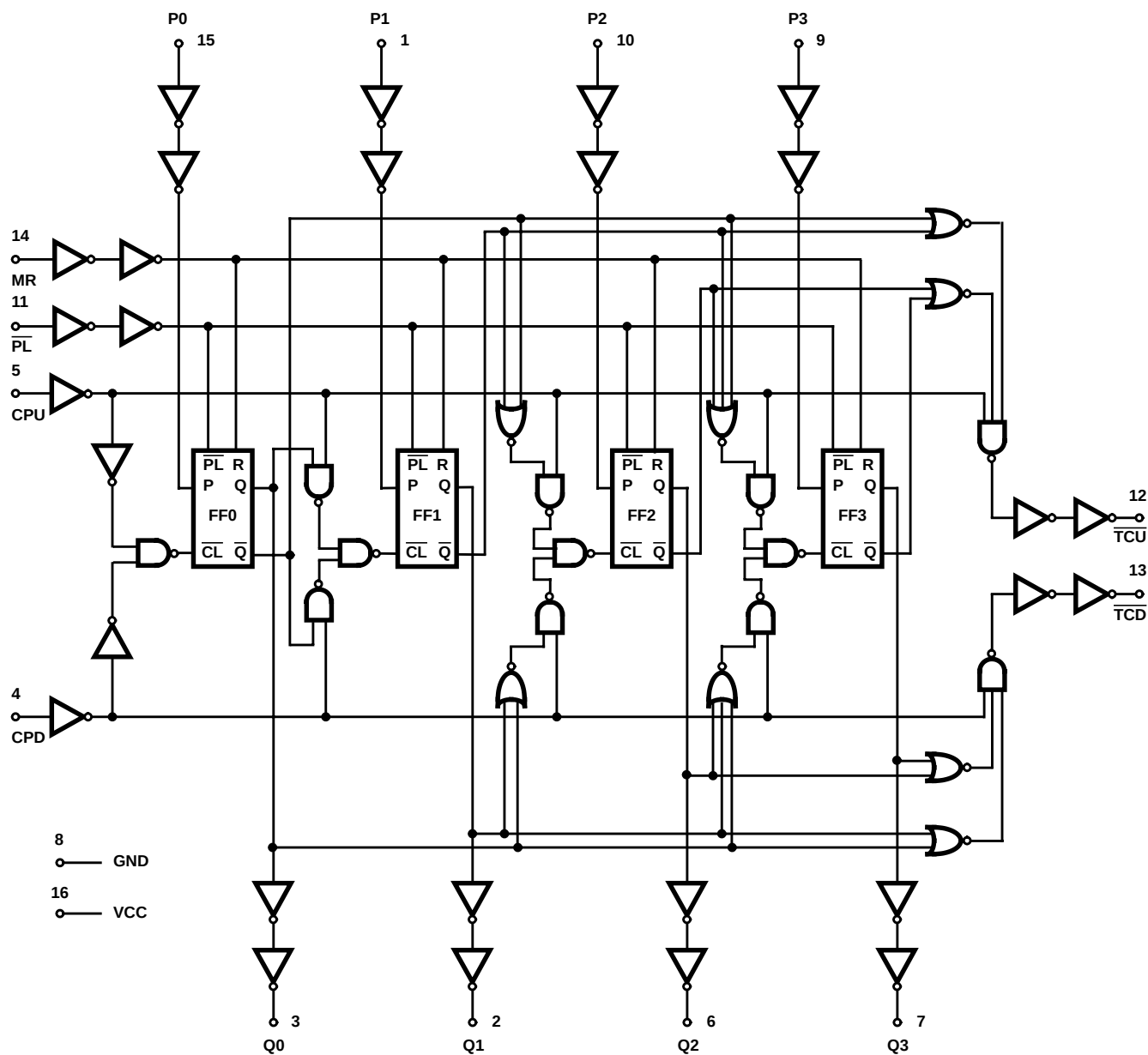
16 LEAD CERAMIC METAL SEAL  
FLATPACK PACKAGE (FLATPACK)  
MIL-STD-1835 CDFP4-F16  
TOP VIEW



## Ordering Information

| PART NUMBER     | TEMPERATURE RANGE | SCREENING LEVEL             | PACKAGE                  |
|-----------------|-------------------|-----------------------------|--------------------------|
| HCTS193DMSR     | -55°C to +125°C   | Intersil Class S Equivalent | 16 Lead SBDIP            |
| HCTS193KMSR     | -55°C to +125°C   | Intersil Class S Equivalent | 16 Lead Ceramic Flatpack |
| HCTS193D/Sample | +25°C             | Sample                      | 16 Lead SBDIP            |
| HCTS193K/Sample | +25°C             | Sample                      | 16 Lead Ceramic Flatpack |
| HCTS193HMSR     | +25°C             | Die                         | Die                      |

Functional Diagram



TRUTH TABLE

| FUNCTION           | CLOCK UP | CLOCK DOWN | RESET | PARALLEL LOAD |
|--------------------|----------|------------|-------|---------------|
| Count Up           |          | H          | L     | H             |
| Count Down         | H        |            | L     | H             |
| Reset              | X        | X          | H     | X             |
| Load Preset Inputs | X        | X          | L     | L             |

H = High Level, L = Low Level, X = Immaterial, = Transition from low to high

## Specifications HCTS193MS

### Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V  
 Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V  
 DC Input Current, Any One Input . . . . . ±10mA  
 DC Drain Current, Any One Output . . . . . ±25mA  
 (All Voltage Reference to the VSS Terminal)  
 Storage Temperature Range (TSTG) . . . . . -65°C to +150°C  
 Lead Temperature (Soldering 10sec) . . . . . +265°C  
 Junction Temperature (TJ) . . . . . +175°C  
 ESD Classification . . . . . Class 1

### Reliability Information

Thermal Resistance  $\theta_{JA}$   $\theta_{JC}$   
 SBDIP Package . . . . . 73°C/W 24°C/W  
 Ceramic Flatpack Package . . . . . 114°C/W 29°C/W  
 Maximum Package Power Dissipation at +125°C Ambient  
 SBDIP Package . . . . . 0.68W  
 Ceramic Flatpack Package . . . . . 0.44W  
 If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:  
 SBDIP Package . . . . . 13.7mW/°C  
 Ceramic Flatpack Package . . . . . 8.8mW/°C

*CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..*

### Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V  
 Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max.  
 Operating Temperature Range (TA) . . . . . -55°C to +125°C  
 Input Low Voltage (VIL) . . . . . 0.0V to 0.8V  
 Input High Voltage (VIH) . . . . . VCC/2 to VCC

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER                         | SYMBOL | (NOTE 1)<br>CONDITIONS                                   | GROUP<br>A SUB-<br>GROUPS | TEMPERATURE          | LIMITS      |      | UNITS |
|-----------------------------------|--------|----------------------------------------------------------|---------------------------|----------------------|-------------|------|-------|
|                                   |        |                                                          |                           |                      | MIN         | MAX  |       |
| Quiescent Current                 | ICC    | VCC = 5.5V,<br>VIN = VCC or GND                          | 1                         | +25°C                | -           | 40   | μA    |
|                                   |        |                                                          | 2, 3                      | +125°C, -55°C        | -           | 750  | μA    |
| Output Current<br>(Sink)          | IOL    | VCC = 4.5V, VIH = 4.5V,<br>VOUT = 0.4V, VIL = 0V         | 1                         | +25°C                | 4.8         | -    | mA    |
|                                   |        |                                                          | 2, 3                      | +125°C, -55°C        | 4.0         | -    | mA    |
| Output Current<br>(Source)        | IOH    | VCC = 4.5V, VIH = 4.5V,<br>VOUT = VCC -0.4V,<br>VIL = 0V | 1                         | +25°C                | -4.8        | -    | mA    |
|                                   |        |                                                          | 2, 3                      | +125°C, -55°C        | -4.0        | -    | mA    |
| Output Voltage Low                | VOL    | VCC = 4.5V, VIH = 2.25V,<br>IOL = 50μA, VIL = 0.80V      | 1, 2, 3                   | +25°C, +125°C, -55°C | -           | 0.1  | V     |
|                                   |        | VCC = 5.5V, VIH = 2.75V,<br>IOL = 50μA, VIL = 0.8V       | 1, 2, 3                   | +25°C, +125°C, -55°C | -           | 0.1  | V     |
| Output Voltage High               | VOH    | VCC = 4.5V, VIH = 2.25V,<br>IOL = -50μA, VIL = 0.80V     | 1, 2, 3                   | +25°C, +125°C, -55°C | VCC<br>-0.1 | -    | V     |
|                                   |        | VCC = 5.5V, VIH = 2.75V,<br>IOL = -50μA, VIL = 0.8V      | 1, 2, 3                   | +25°C, +125°C, -55°C | VCC<br>-0.1 | -    | V     |
| Input Leakage<br>Current          | IIN    | VCC = 5.5V, VIN = VCC or<br>GND                          | 1                         | +25°C                | -           | ±0.5 | μA    |
|                                   |        |                                                          | 2, 3                      | +125°C, -55°C        | -           | ±5.0 | μA    |
| Noise Immunity<br>Functional Test | FN     | VCC = 4.5V, VIH = 2.25V,<br>VIL = 0.8V (Note 2)          | 7, 8A, 8B                 | +25°C, +125°C, -55°C | -           | -    | -     |

**NOTES:**

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

## Specifications HCTS193MS

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | (NOTES 1, 2)<br>CONDITIONS | GROUP<br>A SUB-<br>GROUPS | TEMPERATURE   | LIMITS |     | UNITS |
|-----------|--------|----------------------------|---------------------------|---------------|--------|-----|-------|
|           |        |                            |                           |               | MIN    | MAX |       |
| CPU to Qn | TPLH   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 29  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 34  | ns    |
|           | TPHL   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 35  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 41  | ns    |
| CPD to Qn | TPLH   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 31  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 36  | ns    |
|           | TPHL   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 36  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 42  | ns    |
| PL to Qn  | TPLH   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 32  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 36  | ns    |
|           | TPHL   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 45  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 53  | ns    |
| MR to Qn  | TPHL   | VCC = 4.5V                 | 9                         | +25°C         | 2      | 37  | ns    |
|           |        |                            | 10, 11                    | +125°C, -55°C | 2      | 44  | ns    |

**NOTES:**

1. All voltages referenced to device GND.
2. AC measurements assume  $R_L = 500\Omega$ ,  $C_L = 50\text{pF}$ , Input  $T_R = T_F = 3\text{ns}$ ,  $V_{IL} = \text{GND}$ ,  $V_{IH} = 3\text{V}$ .

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER                              | SYMBOL       | CONDITIONS                    | NOTES | TEMPERATURE   | LIMITS |     | UNITS |
|----------------------------------------|--------------|-------------------------------|-------|---------------|--------|-----|-------|
|                                        |              |                               |       |               | MIN    | MAX |       |
| Capacitance Power Dissipation          | CPD          | VCC = 5.0V, $f = 1\text{MHz}$ | 1     | +25°C         | -      | 53  | pF    |
|                                        |              |                               | 1     | +125°C, -55°C | -      | 75  | pF    |
| Input Capacitance                      | CIN          | VCC = 5.0V, $f = 1\text{MHz}$ | 1     | +25°C         | -      | 10  | pF    |
|                                        |              |                               | 1     | +125°C        | -      | 10  | pF    |
| Output Transition Time                 | TTHL<br>TTLH | VCC = 4.5V                    | 1     | +25°C         | -      | 15  | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | -      | 22  | ns    |
| Maximum Operating Frequency (CPU, CPD) | FMAX         | VCC = 4.5V                    | 1     | +25°C         | -      | 25  | MHz   |
|                                        |              |                               | 1     | +125°C, -55°C | -      | 15  | MHz   |
| Setup Time<br>Pn to PL                 | TSU          | VCC = 4.5V                    | 1     | +25°C         | 15     | -   | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | 22     | -   | ns    |
| Hold Time<br>Pn to PL                  | TH           | VCC = 4.5V                    | 1     | +25°C         | 0      | -   | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | 0      | -   | ns    |
| Hold Time CPD to<br>CPU or CPU to CPD  | TH           | VCC = 4.5V                    | 1     | +25°C         | 16     | -   | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | 24     | -   | ns    |
| Pulse Width<br>CPU to CPD              | TW           | VCC = 4.5V                    | 1     | +25°C         | 23     | -   | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | 35     | -   | ns    |
| Pulse Width PL                         | TW           | VCC = 4.5V                    | 1     | +25°C         | 16     | -   | ns    |
|                                        |              |                               | 1     | +125°C, -55°C | 24     | -   | ns    |

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**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

| PARAMETER                       | SYMBOL | CONDITIONS | NOTES | TEMPERATURE  | LIMITS |     | UNITS |
|---------------------------------|--------|------------|-------|--------------|--------|-----|-------|
|                                 |        |            |       |              | MIN    | MAX |       |
| Pulse Width MR                  | TW     | VCC = 4.5V | 1     | +25°C        | 20     | -   | ns    |
|                                 |        |            | 1     | +125°C, 55°C | 30     | -   | ns    |
| Recovery Time<br>PL to CPU, CPD | TREC   | VCC = 4.5V | 1     | +25°C        | 15     | -   | ns    |
|                                 |        |            | 1     | +125°C, 55°C | 22     | -   | ns    |
| Recovery Time<br>MR to CPU, CPD | TREC   | VCC = 4.5V | 1     | +25°C        | 5      | -   | ns    |
|                                 |        |            | 1     | +125°C, 55°C | 5      | -   | ns    |

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

**TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER                         | SYMBOL | (NOTES 1, 2)<br>CONDITIONS                                  | TEMPERATURE | 200K RAD<br>LIMITS |      | UNITS |
|-----------------------------------|--------|-------------------------------------------------------------|-------------|--------------------|------|-------|
|                                   |        |                                                             |             | MIN                | MAX  |       |
| Quiescent Current                 | ICC    | VCC = 5.5V, VIN = VCC or GND                                | +25°C       | -                  | 0.75 | mA    |
| Output Current (Sink)             | IOL    | VCC = 4.5V, VIN = VCC or GND,<br>VOUT = 0.4V                | +25°C       | 4.0                | -    | mA    |
| Output Current<br>(Source)        | IOH    | VCC = 4.5V, VIN = VCC or GND,<br>VOUT = VCC - 0.4V          | +25°C       | -4.0               | -    | mA    |
| Output Voltage Low                | VOL    | VCC = 4.5V or 5.5V, VIH = VCC/2,<br>VIL = 0.8V, IOL = 50μA  | +25°C       | -                  | 0.1  | V     |
| Output Voltage High               | VOH    | VCC = 4.5V or 5.5V, VIH = VCC/2,<br>VIL = 0.8V, IOL = -50μA | +25°C       | VCC<br>-0.1        | -    | V     |
| Input Leakage Current             | IIN    | VCC = 5.5V, VIN = VCC or GND                                | +25°C       | -                  | ±5   | μA    |
| Noise Immunity<br>Functional Test | FN     | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V,<br>(Note 3)            | +25°C       | -                  | -    | -     |
| CPU to Qn                         | TPLH   | VCC = 4.5V                                                  | +25°C       | 2                  | 34   | ns    |
|                                   | TPHL   | VCC = 4.5V                                                  | +25°C       | 2                  | 41   | ns    |
| CPD to Qn                         | TPLH   | VCC = 4.5V                                                  | +25°C       | 2                  | 36   | ns    |
|                                   | TPHL   | VCC = 4.5V                                                  | +25°C       | 2                  | 42   | ns    |
| PL to Qn                          | TPLH   | VCC = 4.5V                                                  | +25°C       | 2                  | 36   | ns    |
|                                   | TPHL   | VCC = 4.5V                                                  | +25°C       | 2                  | 53   | ns    |
| MR to Qn                          | TPHL   | VCC = 4.5V                                                  | +25°C       | 2                  | 44   | ns    |

NOTES:

- All voltages referenced to device GND.
- AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
- For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

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**TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)**

| PARAMETER | GROUP B SUBGROUP | DELTA LIMIT    |
|-----------|------------------|----------------|
| ICC       | 5                | 12 $\mu$ A     |
| IOL/IOH   | 5                | -15% of 0 Hour |

**TABLE 6. APPLICABLE SUBGROUPS**

| CONFORMANCE GROUPS             | METHOD       | GROUP A SUBGROUPS             | READ AND RECORD                       |
|--------------------------------|--------------|-------------------------------|---------------------------------------|
| Initial Test (Preburn-In)      | 100%/5004    | 1, 7, 9                       | ICC, IOL/H                            |
| Interim Test I (Postburn-In)   | 100%/5004    | 1, 7, 9                       | ICC, IOL/H                            |
| Interim Test II (Postburn-In)  | 100%/5004    | 1, 7, 9                       | ICC, IOL/H                            |
| PDA                            | 100%/5004    | 1, 7, 9, Deltas               |                                       |
| Interim Test III (Postburn-In) | 100%/5004    | 1, 7, 9                       | ICC, IOL/H                            |
| PDA                            | 100%/5004    | 1, 7, 9, Deltas               |                                       |
| Final Test                     | 100%/5004    | 2, 3, 8A, 8B, 10, 11          |                                       |
| Group A (Note 1)               | Sample/5005  | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 |                                       |
| Group B                        | Subgroup B-5 | Sample/5005                   | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas |
|                                | Subgroup B-6 | Sample/5005                   | 1, 7, 9                               |
| Group D                        | Sample/5005  | 1, 7, 9                       |                                       |

NOTE: 1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

**TABLE 7. TOTAL DOSE IRRADIATION**

| CONFORMANCE GROUPS | METHOD | TEST    |          | READ AND RECORD |                  |
|--------------------|--------|---------|----------|-----------------|------------------|
|                    |        | PRE RAD | POST RAD | PRE RAD         | POST RAD         |
| Group E Subgroup 2 | 5005   | 1, 7, 9 | Table 4  | 1, 9            | Table 4 (Note 1) |

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

**TABLE 8. DYNAMIC BURN-IN TEST CONNECTIONS**

| OPEN                                        | GROUND                  | 1/2 VCC = 3V ± 0.5V | VCC = 6V ± 0.5V          | OSCILLATOR |       |
|---------------------------------------------|-------------------------|---------------------|--------------------------|------------|-------|
|                                             |                         |                     |                          | 50kHz      | 25kHz |
| STATIC BURN-IN I TEST CONNECTIONS (Note 1)  |                         |                     |                          |            |       |
| 2, 3, 6, 7, 12, 13                          | 1, 4, 5, 8 - 11, 14, 15 | -                   | 16                       | -          | -     |
| STATIC BURN-IN II TEST CONNECTIONS (Note 1) |                         |                     |                          |            |       |
| 2, 3, 6, 7, 12, 13                          | 8                       | -                   | 1, 4, 5, 9 - 11, 14 - 16 | -          | -     |
| DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)   |                         |                     |                          |            |       |
| -                                           | 1, 8 - 10, 14, 15       | 2, 3, 6, 7, 12, 13  | 4, 11, 16                | 5          | -     |

NOTES:

- Each pin except VCC and GND will have a resistor of 10K $\Omega$   $\pm$  5% for static burn-in.
- Each pin except VCC and GND will have a resistor of 1K $\Omega$   $\pm$  5% for dynamic burn-in.

**TABLE 9. IRRADIATION TEST CONNECTIONS**

| OPEN               | GROUND | VCC = 5V $\pm$ 0.5V      |
|--------------------|--------|--------------------------|
| 2, 3, 6, 7, 12, 13 | 8      | 1, 4, 5, 9 - 11, 14 - 16 |

NOTE: Each pin except VCC and GND will have a resistor of 47K $\Omega$   $\pm$  5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

**Intersil Space Level Product Flow - 'MS'**

|                                                                                      |                                                                                    |
|--------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| Wafer Lot Acceptance (All Lots) Method 5007<br>(Includes SEM)                        | 100% Interim Electrical Test 1 (T1)                                                |
| GAMMA Radiation Verification (Each Wafer) Method 1019,<br>4 Samples/Wafer, 0 Rejects | 100% Delta Calculation (T0-T1)                                                     |
| 100% Nondestructive Bond Pull, Method 2023                                           | 100% Static Burn-In 2, Condition A or B, 24 hrs. min.,<br>+125°C min., Method 1015 |
| Sample - Wire Bond Pull Monitor, Method 2011                                         | 100% Interim Electrical Test 2 (T2)                                                |
| Sample - Die Shear Monitor, Method 2019 or 2027                                      | 100% Delta Calculation (T0-T2)                                                     |
| 100% Internal Visual Inspection, Method 2010, Condition A                            | 100% PDA 1, Method 5004 (Notes 1 and 2)                                            |
| 100% Temperature Cycle, Method 1010, Condition C,<br>10 Cycles                       | 100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or<br>Equivalent, Method 1015  |
| 100% Constant Acceleration, Method 2001, Condition per<br>Method 5004                | 100% Interim Electrical Test 3 (T3)                                                |
| 100% PIND, Method 2020, Condition A                                                  | 100% Delta Calculation (T0-T3)                                                     |
| 100% External Visual                                                                 | 100% PDA 2, Method 5004 (Note 2)                                                   |
| 100% Serialization                                                                   | 100% Final Electrical Test                                                         |
| 100% Initial Electrical Test (T0)                                                    | 100% Fine/Gross Leak, Method 1014                                                  |
| 100% Static Burn-In 1, Condition A or B, 24 hrs. min.,<br>+125°C min., Method 1015   | 100% Radiographic, Method 2012 (Note 3)                                            |
|                                                                                      | 100% External Visual, Method 2009                                                  |
|                                                                                      | Sample - Group A, Method 5005 (Note 4)                                             |
|                                                                                      | 100% Data Package Generation (Note 5)                                              |

**NOTES:**

- Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
- Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
- Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
- Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
- Data Package Contents:
  - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
  - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
  - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
  - X-Ray report and film. Includes penetrometer measurements.
  - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
  - Lot Serial Number Sheet (Good units serial number and lot number).
  - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
  - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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**Sales Office Headquarters**

**NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (321) 724-7000  
FAX: (321) 724-7240

**EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**

Intersil (Taiwan) Ltd.  
Taiwan Limited  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029

## AC Timing Diagrams

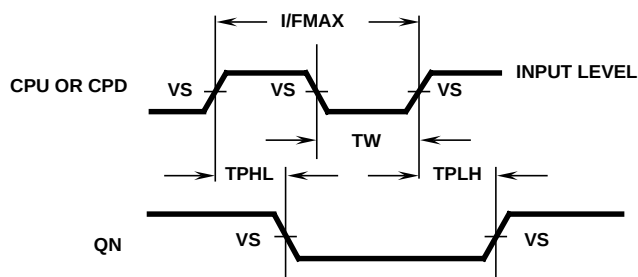


FIGURE 1. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

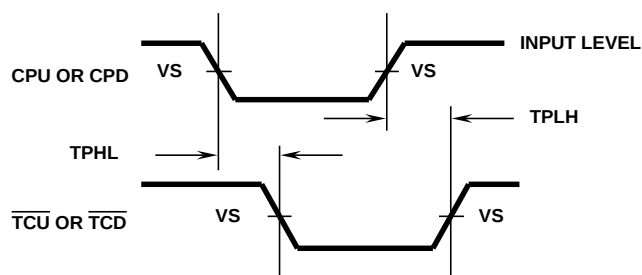


FIGURE 2. CLOCK TO TERMINAL COUNT DELAYS

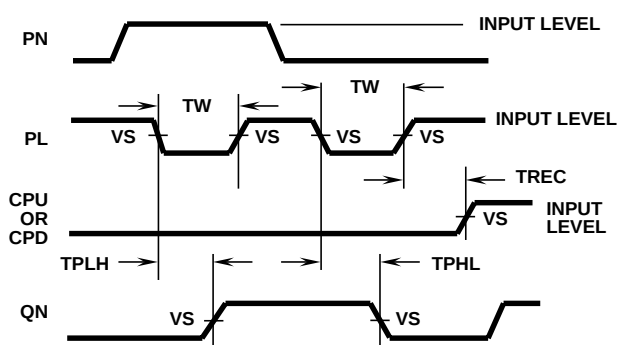


FIGURE 3. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

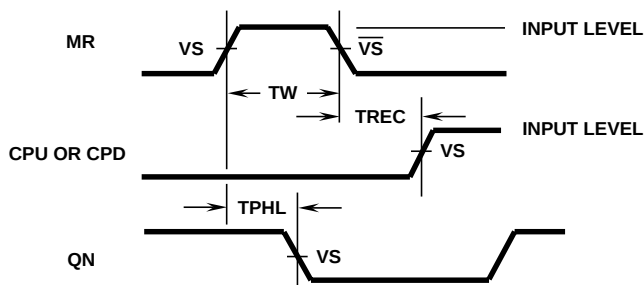


FIGURE 4. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

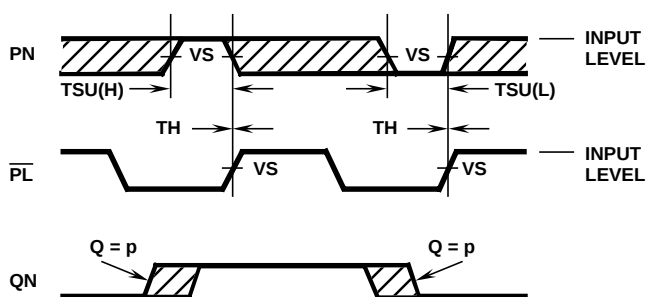


FIGURE 5. SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

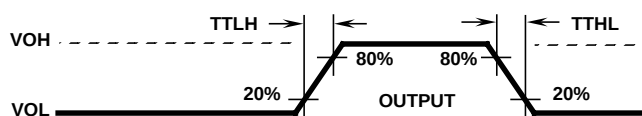


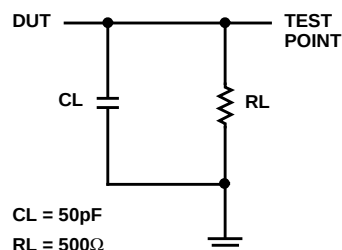
FIGURE 6. OUTPUT TRANSITION TIME

## AC Timing Diagrams

## AC VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC       | 4.50 | V     |
| VIH       | 3.00 | V     |
| VS        | 1.30 | V     |
| VIL       | 0    | V     |
| GND       | 0    | V     |

## AC Load Circuit



## HCTS193MS

### Die Characteristics

#### DIE DIMENSIONS:

104 x 86 mils

#### METALLIZATION:

Type: AlSi

Metal Thickness:  $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

#### GLASSIVATION:

Type:  $\text{SiO}_2$

Thickness:  $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

#### WORST CASE CURRENT DENSITY:

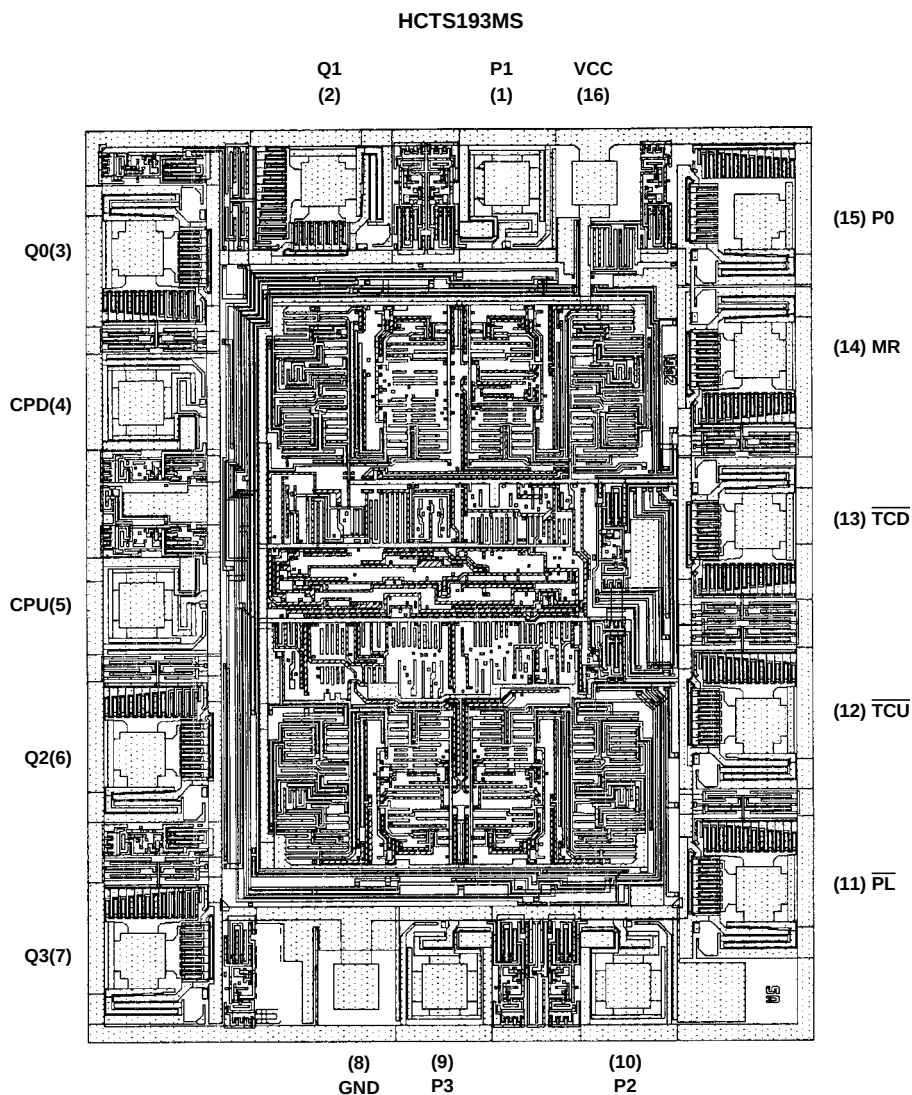
$< 2.0 \times 10^5 \text{A/cm}^2$

#### BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$

4 mils x 4 mils

### Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location.  
The mask series for the HCTS193 is TA14451A.