Micropower, Single Supply, Rail-to-Rail Input-Output Instrumentation Amplifiers

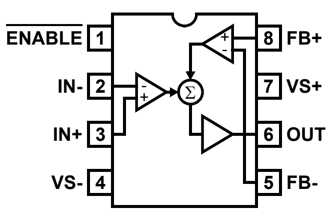
The EL8171 and EL8172 are micropower instrumentation amplifiers optimized for operation at 2.9V to 5V single supplies. Inputs and outputs can operate rail-to-rail. As with all instrumentation amplifiers, a pair of inputs provide very high common-mode rejection and are completely independent from a pair of feedback terminals. The feedback terminals allow zero input to be translated to any output offset, including ground. A feedback divider controls the overall gain of the amplifier.

The EL8172 is compensated for a gain of 100 or more, and the EL8171 is compensated for a gain of 10 or more. The EL8171 and EL8172 have PMOS input devices that provide sub-nA input bias currents.

The amplifiers can be operated from one lithium cell or two Ni-Cd batteries. The EL8171 and EL8172 input range goes from below ground to slightly above positive rail. The output stage swings completely to ground or positive supply - no pull-up or pull-down resistors are needed.

Pinout

EL8171, EL8172
(8 LD SO)
TOP VIEW



Features

- 78µA maximum supply current
- Maximum input offset voltage
  - 300µV (EL8172)
  - 1000µV (EL8171)
- 200pA maximum input bias current
- 3µV/°C offset voltage drift
- 450kHz -3dB bandwidth (G = 10)
- 170kHz -3dB bandwidth (G = 100)
- 0.5V/µs slew rate
- Single supply operation
  - Input voltage range is rail-to-rail
  - Output swings rail-to-rail
- Output sources and sinks ±29mA load current
- 0.2% gain accuracy
- Pb-free plus anneal available (RoHS compliant)

Applications

- Battery- or solar-powered systems
- Strain gauges
- Current monitors
- Thermocouple amplifiers

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8171IS	8171IS	-	8 Ld SO	MDP0027
EL8171IS-T7	8171IS	7”	8 Ld SO	MDP0027
EL8171IS-T13	8171IS	13”	8 Ld SO	MDP0027
EL8171ISZ (See Note)	8171ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL8171ISZ-T7 (See Note)	8171ISZ	7”	8 Ld SO (Pb-free)	MDP0027
EL8171ISZ-T13 (See Note)	8171ISZ	13”	8 Ld SO (Pb-free)	MDP0027

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8172IS	8172IS	-	8 Ld SO	MDP0027
EL8172IS-T7	8172IS	7”	8 Ld SO	MDP0027
EL8172IS-T13	8172IS	13”	8 Ld SO	MDP0027
EL8172ISZ (See Note)	8172ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL8172ISZ-T7 (See Note)	8172ISZ	7”	8 Ld SO (Pb-free)	MDP0027
EL8172ISZ-T13 (See Note)	8172ISZ	13”	8 Ld SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Description

EL8171/EL8172	PIN NAME	PIN FUNCTION
1	$\overline{\text{ENABLE}}$	Active Low. When pulled up above 2V, the in-amp conserves 3µA disabled supply current and the output is in a high impedance state. An internal pull down defines the $\overline{\text{ENABLE}}$ low when left floating.
2	IN-	Inverting (IN-) and non-inverting (IN+) high impedance input terminals. The input terminals are equivalent to the gate of PMOS transistor.
3	IN+	
5	FB-	High impedance feedback terminals. The feedback terminals have a very similar equivalent circuit as the input terminals. The negative feedback (FB-) pin connects to an external resistive network to set the gain of the in-amp. The positive feedback (FB+) pin can be used to shift the DC level of the output or as an output offset.
8	FB+	
7	VS+	Positive supply terminal.
4	VS-	Negative supply terminal.
6	VOUT	Output Voltage.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage, V_S 5.5V
Differential Input Current 5mA
Differential Input Voltage 5V
V_{EN} . . . . .0.5V to V_S+ + 0.5V
ESD 3kV

Output Short-Circuit Duration . . . . .Indefinite
Ambient Operating Temperature . . . .-40°C to +85°C
Storage Temperature . . . .-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = GND, VCM = 1/2V_S+ T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	EL8171			400	1000	µV
		EL8172			150	300	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	Temperature = -40°C to 85°C			3		µV/°C
I_{OS}	Input Offset Current				10	200	pA
I_B	Input Bias Current				10	200	pA
e_N	Input Noise Voltage	EL8171	f = 0.1Hz to 10Hz		10		$µV_{P-P}$
		EL8172			4		$µV_{P-P}$
	Input Noise Voltage Density	f_o = 1kHz			50		nV/√Hz
R_{IN}	Input Resistance				25		GΩ
V_{IN}	Input Voltage Range	Guaranteed by CMRR test		0		5	V
CMRR	Common Mode Rejection Ratio	EL8172, V_{CM} = 0V to +5V		80	108		dB
		EL8171, V_{CM} = 0V to +5V		80	104		dB
PSRR	Power Supply Rejection Ratio	EL8172, V_S = 2.4V to 5V		80	104		dB
		EL8171, V_S = 2.4V to 5V		70	90		dB
E_G	Gain Error	EL8172, R_L = 100kΩ to 2.5V		-1.5	+0.3	+1.5	%
		EL8171, R_L = 100kΩ to 2.5V		-0.8	+0.2	+0.8	%
V_{OUT}	Maximum Voltage Swing	Output low, 100kΩ to 2.5V		0	4	10	mV
		Output low, 1kΩ to 2.5V			0.13	0.25	V
		Output high, 100kΩ to 2.5V		4.990	4.996		V
		Output high, 1kΩ to GND		4.75	4.88		V
SR	Slew Rate	R_L = 1kΩ to GND		0.3	0.5	0.7	V/µs
-3dB BW	-3dB Bandwidth	EL8171	Gain = 10V/V		450		kHz
			Gain = 20		210		kHz
			Gain = 50		66		kHz
			Gain = 100		33		kHz
		EL8172	Gain = 100		172		kHz
			Gain = 200		70		kHz
			Gain = 500		25		kHz
			Gain = 1000		12		kHz
$I_{S,EN}$	Supply Current, Enabled			40	60	78	µA

Electrical Specifications V_S+ = +5V, V_{S}- = GND, VCM = 1/2V_S+ T_A = 25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{S,DIS}$	Supply Current, Disabled	$\overline{EN}$ = V_S+	1.5	2.9	5	µA
V_{ENH}	$\overline{\text{Enable}}$ Pin for Shut-down		2			V
V_{ENL}	$\overline{\text{Enable}}$ Pin for Power-on				0.8	V
V_S	Minimum Supply Voltage			2.2	2.4	V
I_O	Output Current into 10Ω to V_S/2	V_S = 5V	±18	±29		mA
		V_S = 2.9V	±4	±7.5		mA

Typical Performance Curves

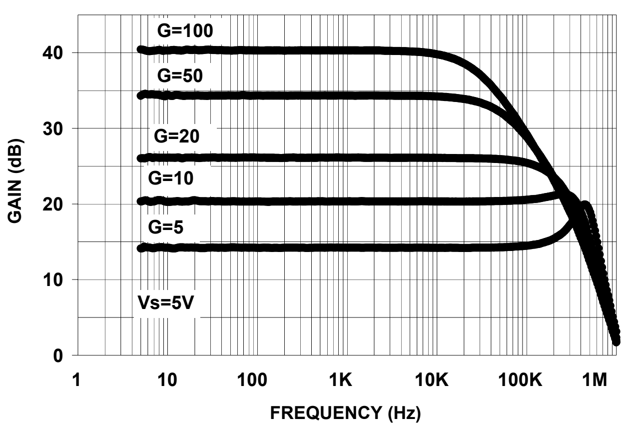


FIGURE 1. EL8171 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

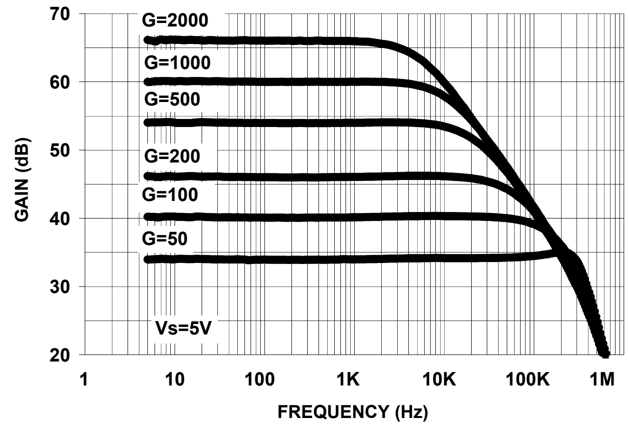


FIGURE 2. EL8172 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

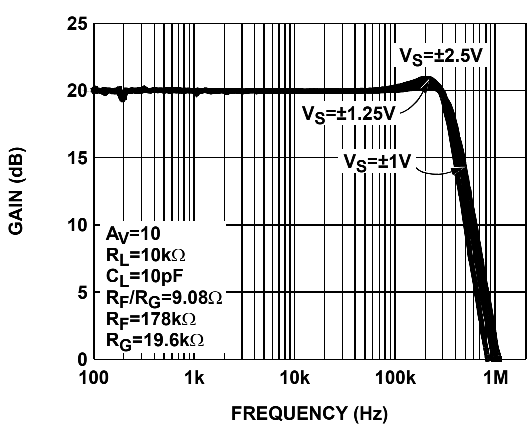


FIGURE 3. EL8171 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

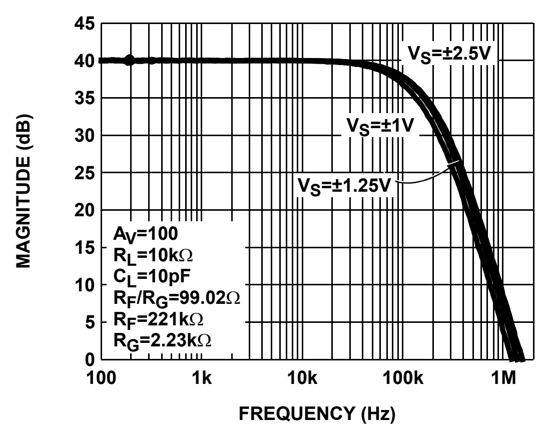


FIGURE 4. EL8172 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

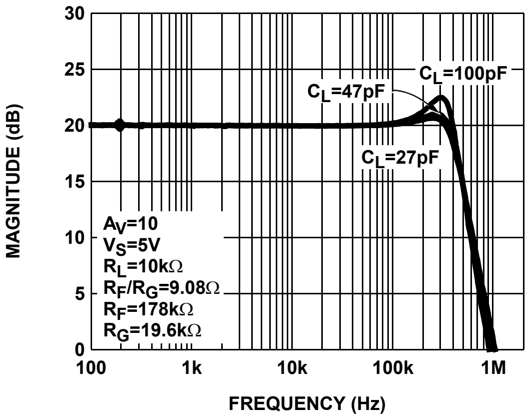


FIGURE 5. EL8171 FREQUENCY RESPONSE vs C_{LOAD}

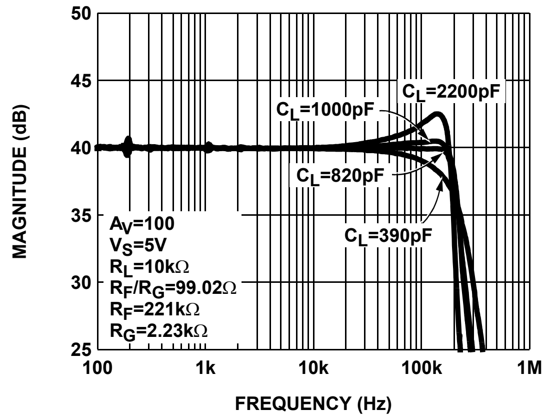


FIGURE 6. EL8172 FREQUENCY RESPONSE vs C_{LOAD}

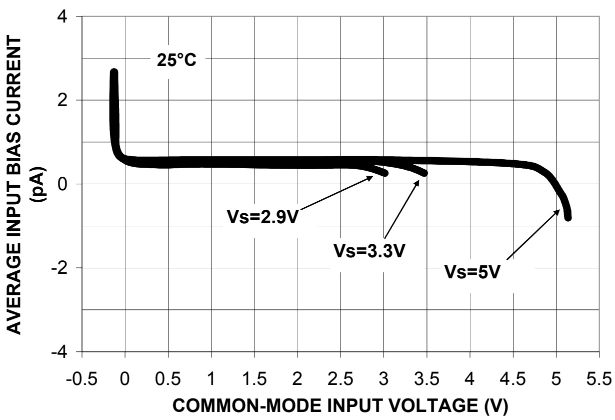


FIGURE 7. EL8171 AND EL8172 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ 25°C

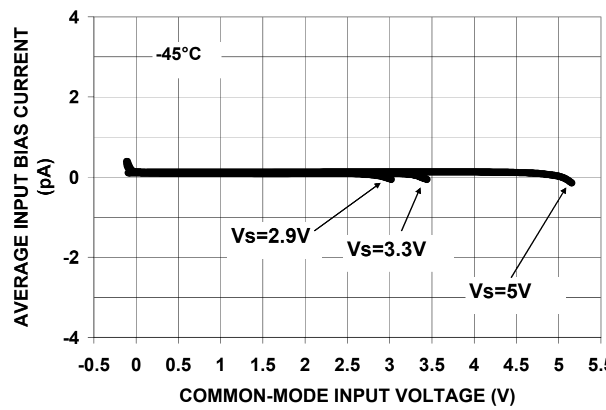


FIGURE 8. EL8171 AND EL8172 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ -45°C

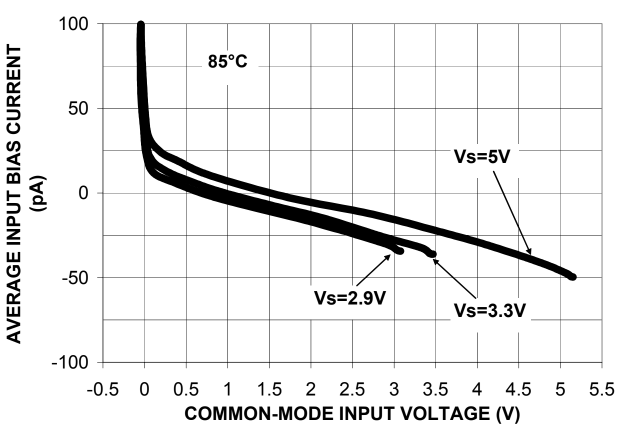


FIGURE 9. EL8171 AND EL8172 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ 85°C

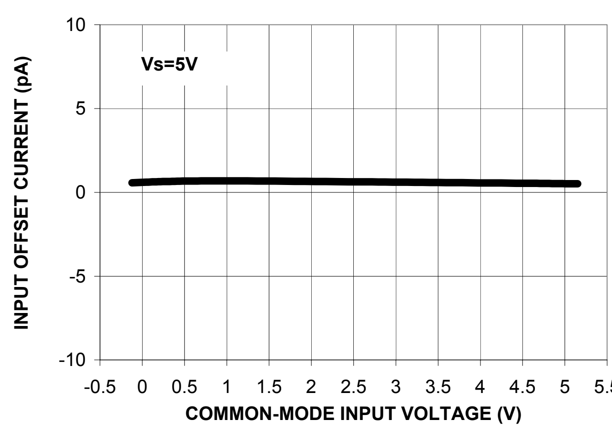


FIGURE 10. EL8171 AND EL8172 INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

Typical Performance Curves (Continued)

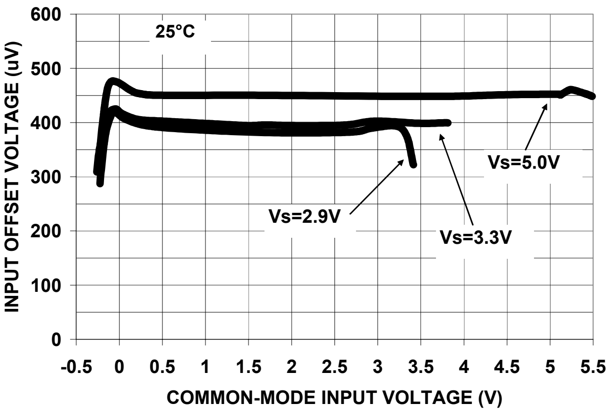


FIGURE 11. EL8171 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ 25°C

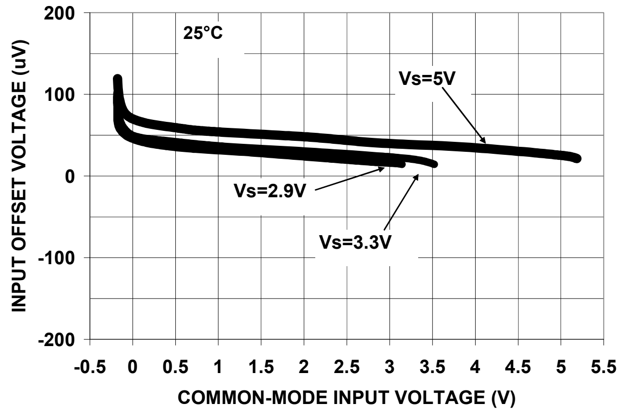


FIGURE 12. EL8172 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ 25°C

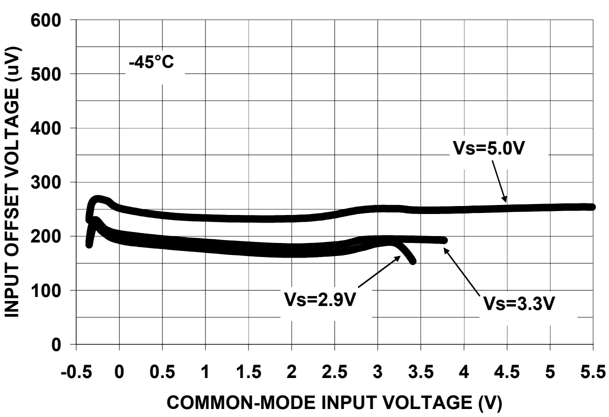


FIGURE 13. EL8171 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ -45°C

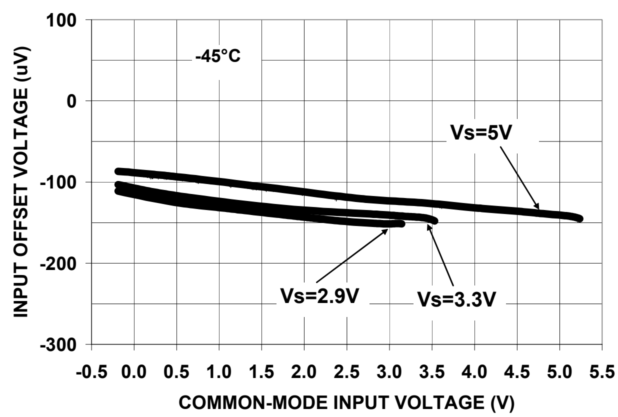


FIGURE 14. EL8172 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ -45°C

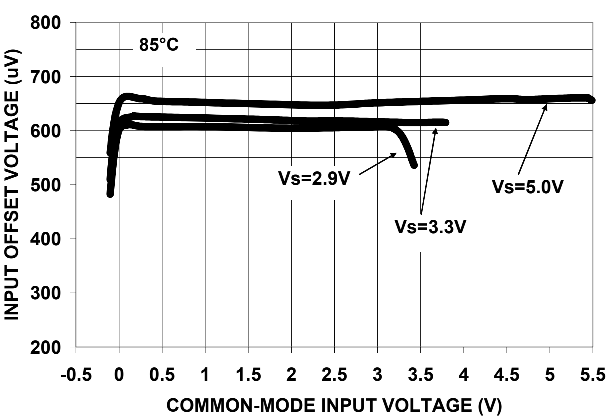


FIGURE 15. EL8171 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ 85°C

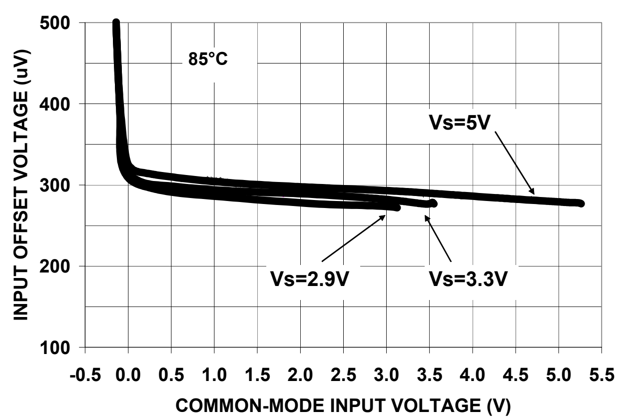


FIGURE 16. EL8172 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ 85°C

Typical Performance Curves (Continued)

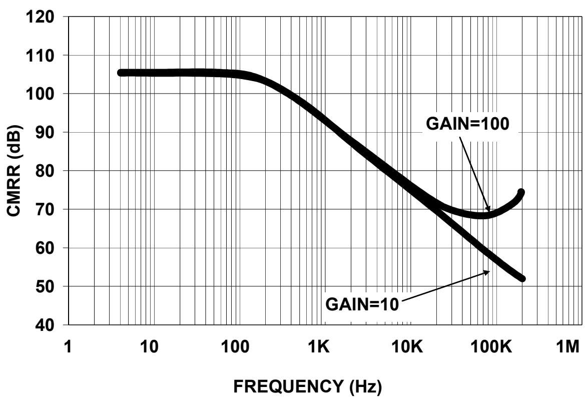


FIGURE 17. EL8171 CMRR vs FREQUENCY

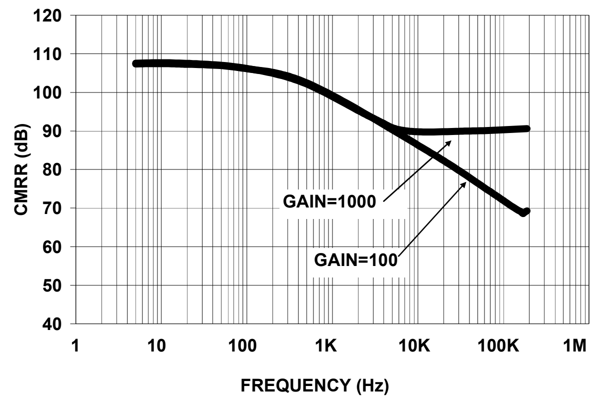


FIGURE 18. EL8172 CMRR vs FREQUENCY

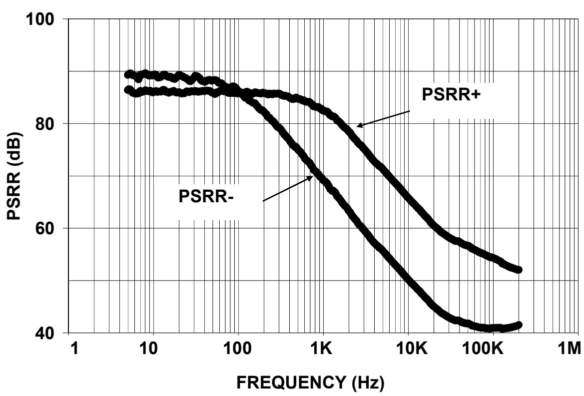


FIGURE 19. EL8171 PSRR vs FREQUENCY

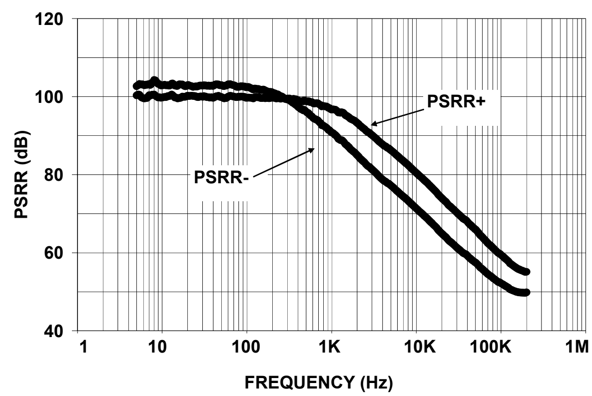


FIGURE 20. EL8172 PSRR vs FREQUENCY

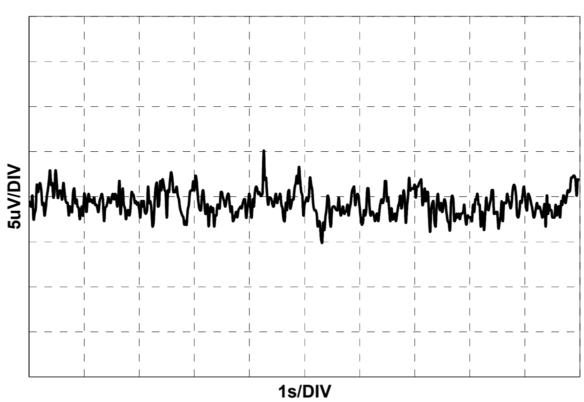


FIGURE 21. EL8171 0.1Hz to 10Hz INPUT VOLTAGE NOISE (GAIN = 10)

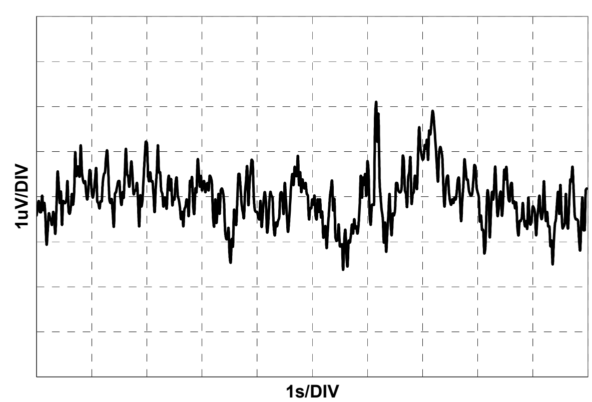


FIGURE 22. EL8172 0.1Hz to 10Hz INPUT VOLTAGE NOISE (GAIN = 100)

Typical Performance Curves (Continued)

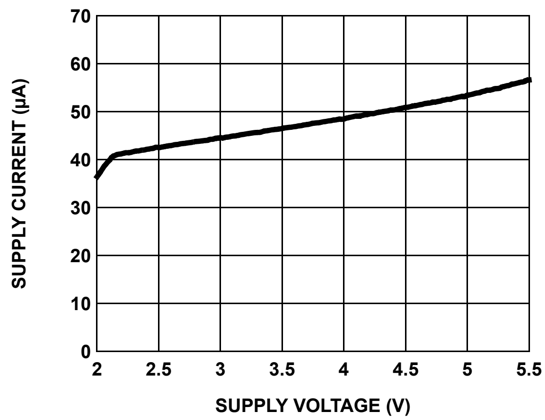


FIGURE 23. EL8171 AND EL8172 SUPPLY CURRENT vs SUPPLY VOLTAGE

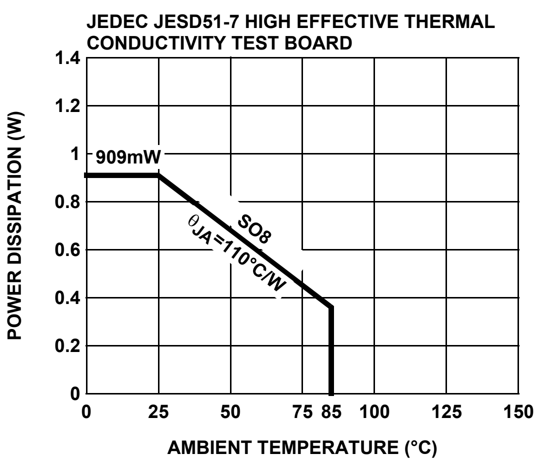


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

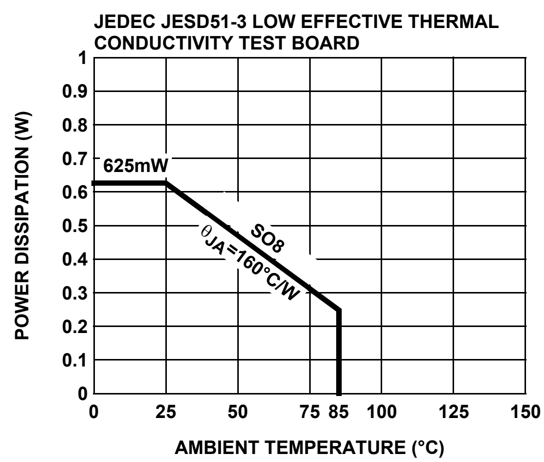


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Application Information

Product Description

The EL8171 and EL8172 are micropower instrumentation amplifiers (in-amps) which deliver rail-to-rail input amplification and rail-to-rail output swing on a single 2.4V to 5V supply. The EL8171 and EL8172 also deliver excellent DC and AC specifications while consuming only 60µA typical supply current. Because EL8171 and EL8172 provide an independent pair of feedback terminals to set the gain and to adjust the output level, these in-amps achieve high common-mode rejection ratio regardless of the tolerance of the gain setting resistors. The EL8171 is internally compensated for a minimum closed loop gain of 10 or greater, well suited for moderate to high gains. For higher gains, the EL8172 is internally compensated for a minimum gain of 100. An $\overline{\text{ENABLE}}$ pin is used to reduce power consumption, typically 2.9µA, while the instrumentation amplifier is disabled.

Input Protection

All input and feedback terminals of the EL8171 and EL8172 have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode drop beyond the supply rails. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistor may be used as a protection to limit excessive external voltage and current from damaging the inputs.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of the EL8171 and EL8172 are single differential pair P-MOSFET devices aided by an Input Range Enhancement Circuit to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) also have a similar topology. As a result, the input common-mode voltage range of both the EL8171 and EL8172 is rail-to-rail. These in-amps are able to handle input voltages that are at or slightly beyond the supply and ground making these in-amps well suited for single 5V or 3.3V low voltage supply systems. There is no need then to move the common-mode input of the in-amps to achieve symmetrical input voltage.

Output Stage and Output Voltage Range

A pair of complementary MOSFET devices drives the output VOUT to within a few mV of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply, while the NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability of the EL8171 and EL8172 are internally limited to 29mA.

Gain Setting

VIN, the potential difference across IN+ and IN-, is replicated (less the input offset voltage) across FB+ and FB-. The obsession of the EL8171 and EL8172 in-amp is to maintain the differential voltage across FB+ and FB- equal to IN+ and IN-; (FB+ - FB-) = (IN+ - IN-). Consequently, the transfer function can be derived. The gain of the EL8171 and EL8172 is set by two external resistors, the feedback resistor RF, and the gain resistor RG.

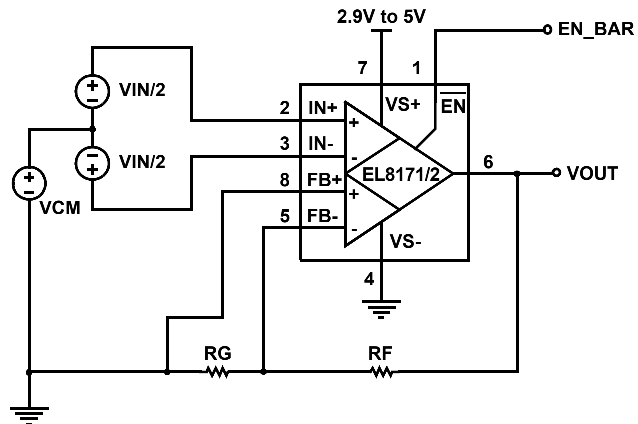


FIGURE 26. CIRCUIT 1 - GAIN IS BY EXTERNAL RESISTORS R_F AND R_G

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)VIN$$

In Figure 26, the FB+ pin and one end of resistor RG are connected to GND. With this configuration, the above gain equation is only true for a positive swing in VIN; negative input swings will be ignored and the output will be at ground.

Reference Connection

Unlike a three-opamp instrumentation amplifier, a finite series resistance seen at the REF terminal does not degrade the EL8171 and EL8172's high CMRR performance eliminating the need for an additional external buffer amplifier. Circuit 2 (Figure 27) uses the FB+ pin to provide a high impedance REF terminal.

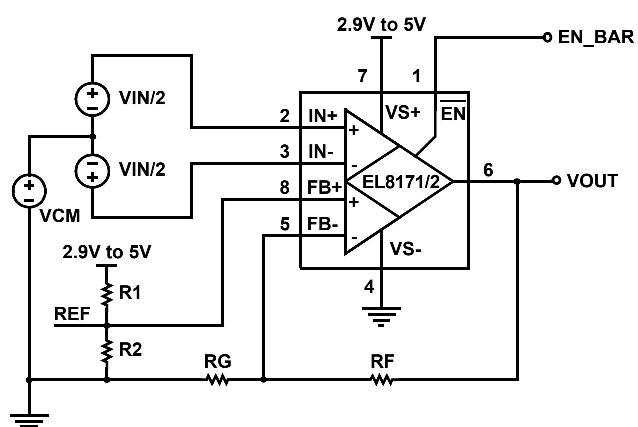


FIGURE 27. CIRCUIT 2 - GAIN SETTING AND REFERENCE CONNECTION

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + \left(1 + \frac{R_F}{R_G}\right)(VREF)$$

The FB+ pin is used as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift VOUT by VREF times the closed loop gain, which is set by resistors RF and RG. See Circuit 2 (Figure 27).

The FB+ pin can also be connected to the other end of resistor, RG. See Circuit 3 (Figure 28). Keeping the basic concept that the EL8171 and EL8172 in-amps maintain constant differential voltage across the input terminals and feedback terminals (IN+ - IN- = FB+ - FB-), the transfer function of Circuit 3 can be derived.

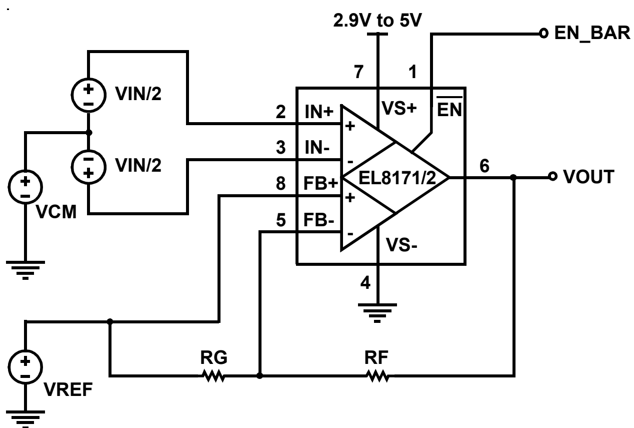


FIGURE 28. CIRCUIT 3 - REFERENCE CONNECTION WITH AN AVAILABLE VREF

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + (VREF)$$

A finite resistance Rs in series with the VREF source, adds an output offset of VIN*(RS/RG). As the series resistance Rs approaches zero, the gain equation is simplified to the above equation for Circuit 3. VOUT is simply shifted by an amount VREF.

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the EL8171 and EL8172, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three opamp and especially a two opamp in-amp, the EL8171 and EL8172 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The EL8171 and EL8172 CMRR will be 108dB regardless of the tolerance of the resistors used.

Gain Error and Accuracy

The EL8172 has a Gain Error, EG, of 0.2% typical. The EL8171 has an EG of 0.3% typical. The gain error indicated in the electrical specifications table is the inherent gain error of the EL8171 and EL8172 and does not include the gain error contributed by the resistors. There is an additional gain error due to the tolerance of the resistors used. The resulting non-ideal transfer function effectively becomes:

$$VOUT = \left(1 + \frac{R_F}{R_G}\right) \times [1 - (E_{RG} + E_{RF} + E_G)] \times VIN$$

Where:

ERG = Tolerance of RG

ERF = Tolerance of RF

EG = Gain Error of the EL8171 or EL8172

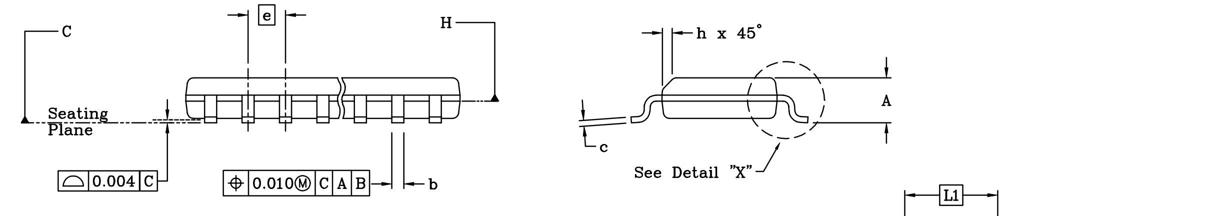
The term [1-(ERG +ERF +EG)] is the deviation from the theoretical gain. Thus, (ERG +ERF +EG) is the total gain error. For example, if 1% resistors are used for the EL8171, the total gain error would be:

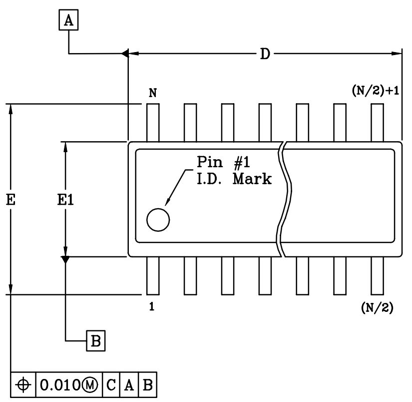
$$= \pm(E_{RG} + E_{RF} + E_G(\text{typical}))$$
$$= \pm(0.01 + 0.01 + 0.003)$$
$$= \pm 2.3\%$$

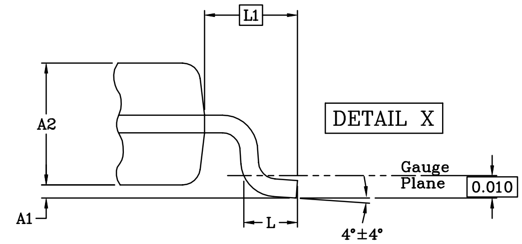
Disable/Power-Down

The EL8171 and EL8172 can be powered down reducing the supply current to typically 2.9µA. When disabled, the output is in a high impedance state. The active low $\overline{\text{ENABLE}}$ bar pin has an internal pull down and hence can be left floating and the in-amp enabled by default. When the $\overline{\text{ENABLE}}$ bar is connected to an external logic, the in-amp will power down when $\overline{\text{ENABLE}}$ bar is pulled above 2V, and will power on when $\overline{\text{ENABLE}}$ bar is pulled below 0.8V.

Package Outline Drawing







DIMENSION TABLE

Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027
Rev: L
Date: 2/15/01
Units: Inches
JEDEC Reg: MS-012/013

PACKAGE OUTLINE DRAWING
SMALL OUTLINE (SO) PACKAGE FAMILY

élantec Semiconductor, Inc.
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Notes:

(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp