查询EL4543供应商

Data Sheet October 26, 2005 FN7325.5

Triple Differential Twisted-Pair Driver with Common-Mode Sync Encoding

The EL4543 is a high bandwidth triple differential amplifier with integrated encoding of video sync signals. The inputs are suitable for handling high speed video or other communications signals in either single-ended or differential form, and the common-mode input range extends all the way to the negative rail enabling ground-referenced signalling in single supply applications. The high bandwidth enables differential signalling onto standard twisted-pair or coax with very low harmonic distortion, while internal feedback ensures balanced gain and phase at the outputs reducing radiated EMI and harmonics.

Embedded logic encodes standard video horizontal and vertical sync signals onto the common mode of the twisted pair(s), transmitting this additional information without the requirement for additional buffers or transmission lines. The EL4543 enables significant system cost savings when compared with discrete line driver alternatives.

The EL4543 is available in a 24 Ld QSOP package and is specified for operation over the -40°C to +85°C temperature range.

TABLE 1. SYNC SIGNAL ENCODING

H	V	COMMON MODE A (RED)	COMMON MODE B (GREEN)	COMMON MODE C (BLUE)
Low	High	3.0	2.0	2.5
Low	Low	2.5	3.0	2.0
High	Low	2.0	3.0	2.5
High	High	2.5	2.0	3.0

TABLE 2. INPUT LOGIC THRESHOLD (+5V SUPPLY)

V_{LO}, max	0.8V
V_{HI}, min	2V

Features

- Fully differential inputs, outputs, and feedback
- 350MHz -3dB bandwidth
- 1200V/µs slew rate
- -75dB distortion at 5MHz
- Single 5V to 12V operation
- 50mA minimum output current
- Low power - 36mA total typical supply current
- Pb-free plus anneal available (RoHS compliant)

Applications

- Twisted-pair drivers
- Differential line drivers
- VGA over twisted-pair
- Transmission of analog signals in a noisy environment

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL4543IU	EL4543IU	-	24 Ld QSOP	MDP0040
EL4543IU-T7	EL4543IU	7”	24 Ld QSOP	MDP0040
EL4543IU-T13	EL4543IU	13”	24 Ld QSOP	MDP0040
EL4543IUZ (See Note)	EL4543IUZ	-	24 Ld QSOP (Pb-Free)	MDP0040
EL4543IUZ-T7 (See Note)	EL4543IUZ	7”	24 Ld QSOP (Pb-Free)	MDP0040
EL4543IUZ-T13 (See Note)	EL4543IUZ	13”	24 Ld QSOP (Pb-Free)	MDP0040
EL4543IL	4543IL	-	20 Ld 4x4 QFN*	MDP0046
EL4543IL-T7	4543IL	7”	20 Ld 4x4 QFN*	MDP0046
EL4543IL-T13	4543IL	13”	20 Ld 4x4 QFN*	MDP0046
EL4543ILZ (See Note)	4543ILZ	-	20 Ld 4x4 QFN* (Pb-Free)	MDP0046
EL4543ILZ-T7 (See Note)	4543ILZ	7”	20 Ld 4x4 QFN* (Pb-Free)	MDP0046
EL4543ILZ-T13 (See Note)	4543ILZ	13”	20 Ld 4x4 QFN* (Pb-Free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*20 Ld 4x4 QFN, exposed pad 2.7 x 2.7mm

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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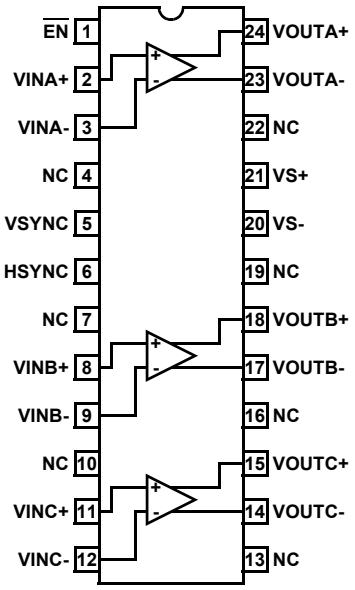
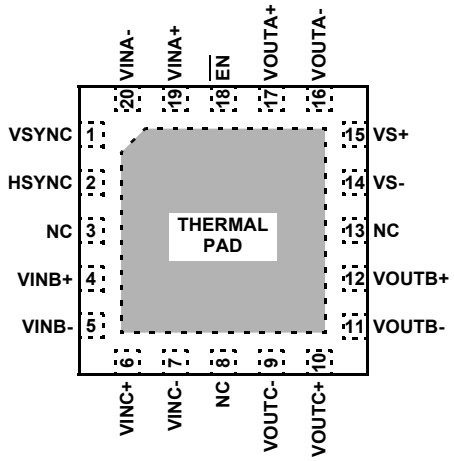
Pinouts

EL4543
(24 LD QSOP)
TOP VIEW



EL4543
(20 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ & V_S-) . . . . . +12V
Maximum Output Continuous Current . . . . . ±70mA
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +135°C
Ambient Operating Temperature . . . . . -40°C to +85°C
V_{IN}+, V_{INB} . . . . . V_S- + 0.8V (min) to V_S+ - 0.8V (max)
V_{IN}- - V_{INB} . . . . . ±5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

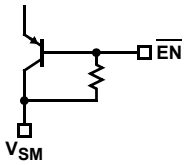
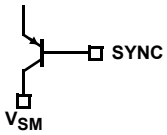
IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = 0V, T_A = 25°C, V_{IN} = 0V, R_L = 150Ω, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW (-3dB)	-3dB Bandwidth	$V_{OUT} = 2V_{P-P}$		350		MHz
SR	Differential Slew Rate	R_L = 200Ω	600	1000		V/µs
T_{STL}	Settling Time to 0.1%			13.6		ns
GBW	Gain Bandwidth Product			700		MHz
HD2	2nd Harmonic Distortion	f = 20MHz, R_L = 200Ω		-70		dBc
HD3	3rd Harmonic Distortion	f = 20MHz, R_L = 200Ω		-70		dBc
dP	Differential Phase @ 3.58MHz			0.01		°
dG	Differential Gain @ 3.58MHz			0.01		%
INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage		-10	2	10	mV
I_{IN}	Input Bias Current (V_{IN}+, V_{IN}+)		-30	-15	-10	µA
Z_{IN}	Differential Input Impedance			180		kΩ
V_{DIFF}	Differential Input Range			±0.75		V
V_{CM}	Input Common Mode Voltage Range		0		2.3	V
V_N	Input Referred Voltage Noise			27		nV/√Hz
CMRR	Input Common Mode Rejection Ratio	V_{CM} = 0 to 2V	60	80		dB
$\overline{EN}$	Threshold			1.4		V
OUTPUT CHARACTERISTICS						
I_{OUT}	Output Peak Current		40	60		mA
DC PERFORMANCE						
A_V	Voltage Gain	$V_{IN} = 0.8V_{P-P}$	1.82	1.96	2.05	V/V
SUPPLY CHARACTERISTICS						
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	5		12	V
I_S	Power Supply Current (per Channel)		12.3	14.5	16.2	mA
PSRR	Power Supply Rejection Ratio		70	80		dB

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION	EQUIVALENT CIRCUIT
1	$\overline{EN}$	Disables video inputs and outputs	 CIRCUIT 1
2	VINA+	Non-inventing input	
3	VINA-	Inverting input	
4, 7, 10, 13, 16, 19, 22	NC	Not connected	
5	VSYNC	Vertical sync logic input	 CIRCUIT 2
6	HSYNC	Horizontal sync logic input	Reference Circuit 2
8	VINB+	Non-inventing input	
9	VINB-	Inverting input	
11	VINC+	Non-inverting input	
12	VINC-	Inverting input	
14	VOUTC-	Inverting output	
15	VOUTC+	Non-inverting output	
17	VOUTB-	Inverting output	
18	VOUTB+	Non-inverting output	
20	VS-	Negative supply	
21	VS+	Positive supply	
23	VOUTA-	Non-inverting output	
24	VOUTA+	Inverting output	

Typical Performance Curves

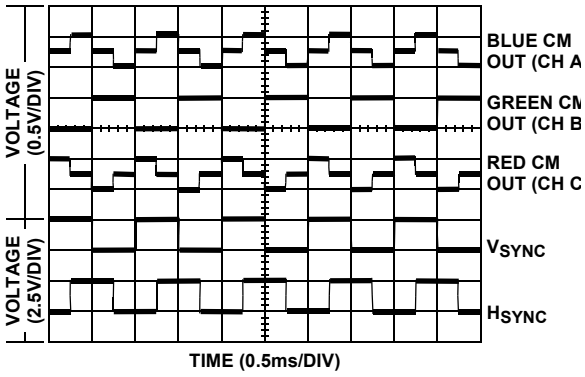


FIGURE 1. COMMON MODE OUTPUT

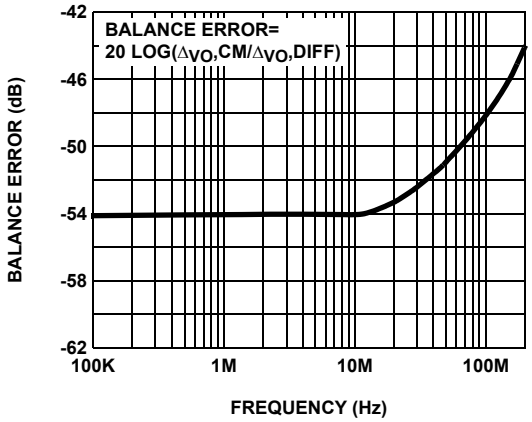


FIGURE 2. BALANCE ERROR

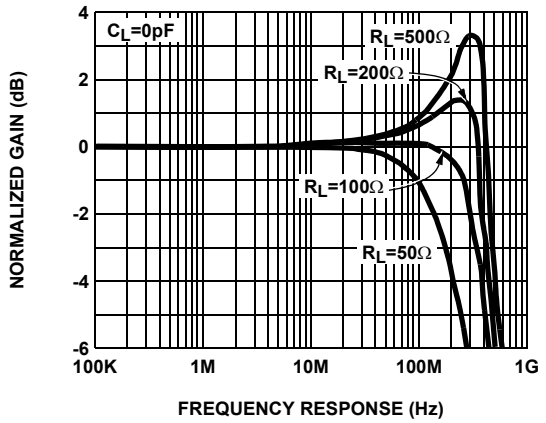


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS R_L - DIFF

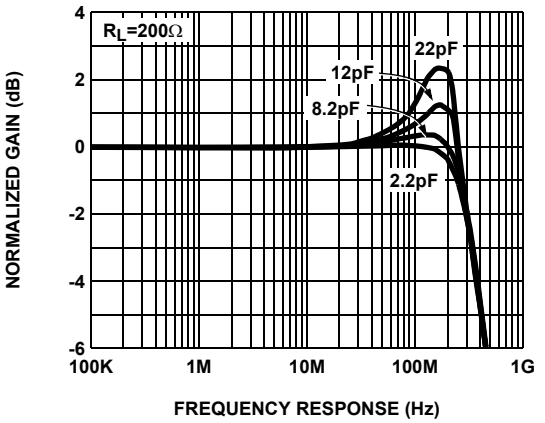


FIGURE 4. DIFFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS C_L - DIFF

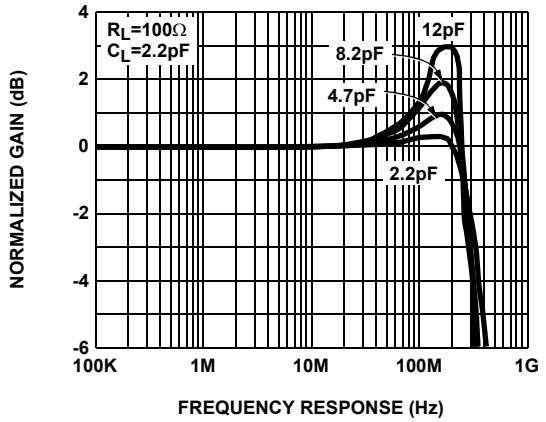


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS C_L - DIFF

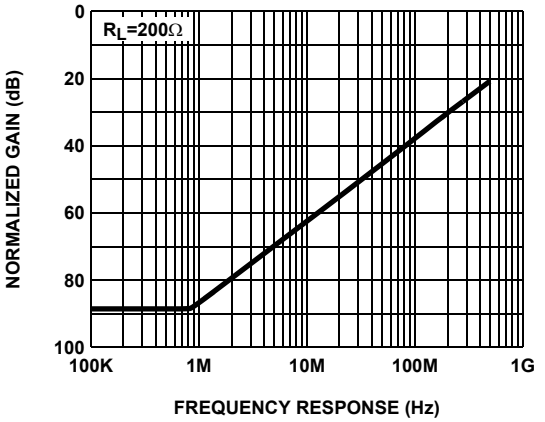


FIGURE 6. CMRR

Typical Performance Curves (Continued)

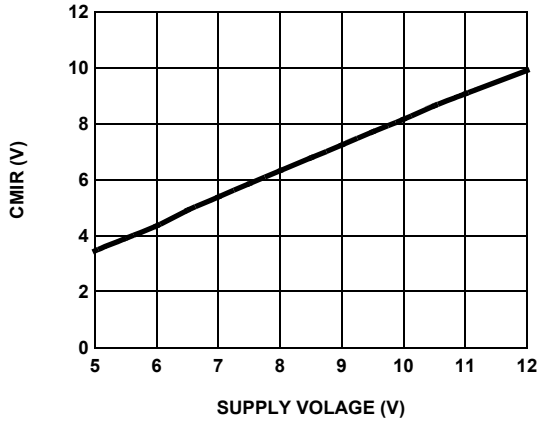


FIGURE 7. COMMON MODE INPUT RANGE vs SUPPLY VOLTAGE

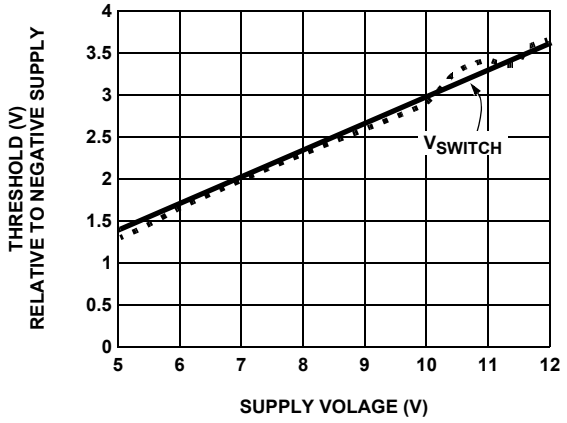


FIGURE 8. H_{SYNC} & V_{SYNC} THRESHOLD vs SUPPLY VOLTAGE

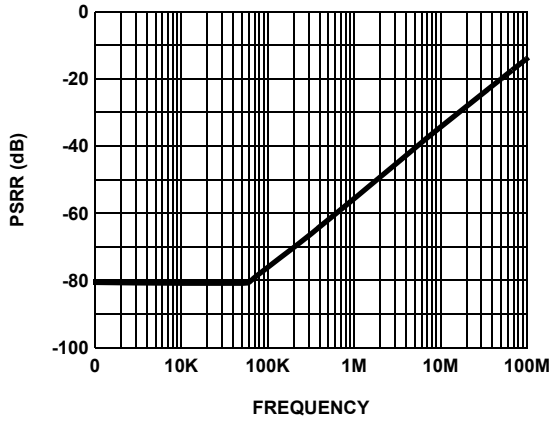


FIGURE 9. PSRR vs FREQUENCY

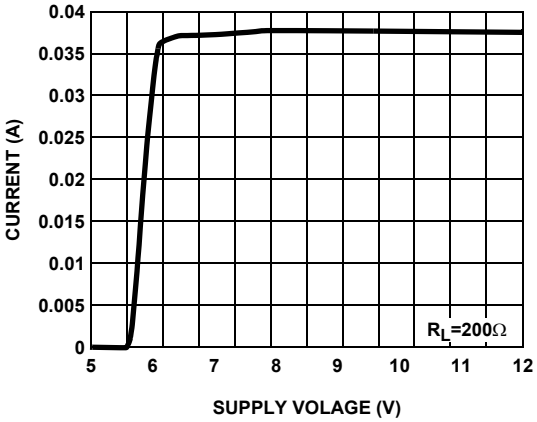


FIGURE 10. I_{SUPPLY} vs V_{SUPPLY}

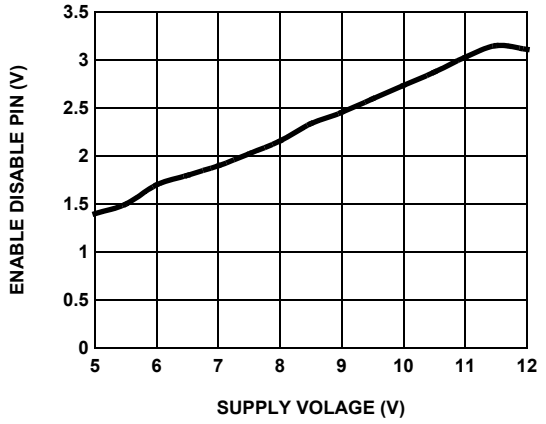


FIGURE 11. ENABLE DISABLE vs SUPPLY VOLTAGE

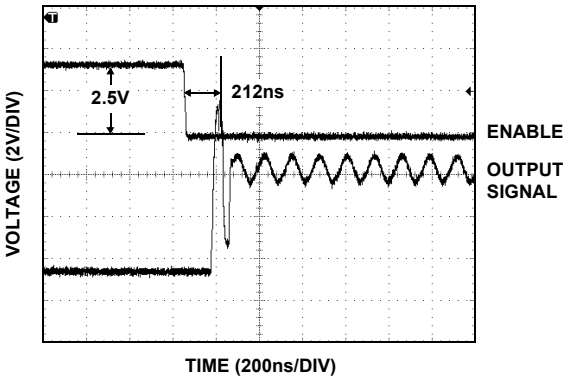


FIGURE 12. ENABLE RESPONSE

Typical Performance Curves (Continued)

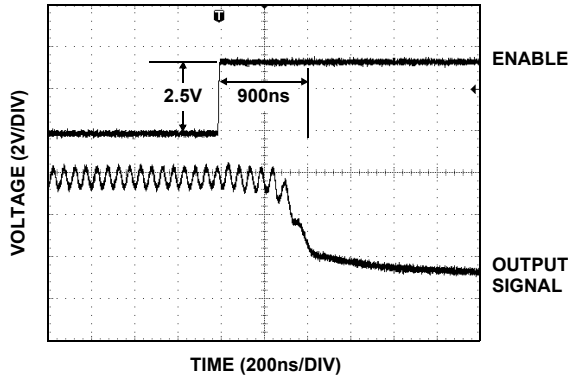


FIGURE 13. DISABLE RESPONSE

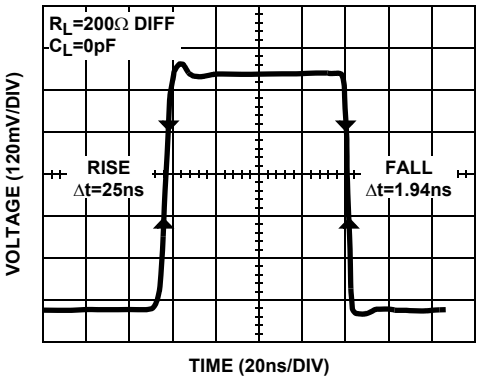


FIGURE 14. DIFFERENTIAL SMALL SIGNAL TRANSIENT RESPONSE

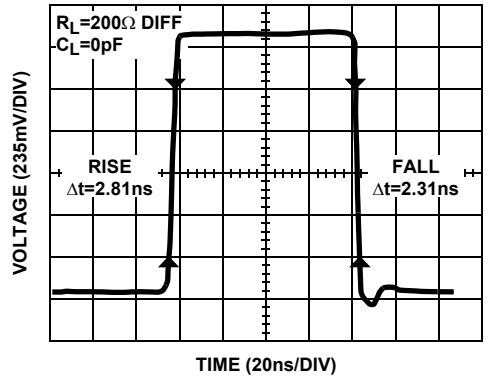


FIGURE 15. DIFFERENTIAL LARGE SIGNAL TRANSIENT RESPONSE

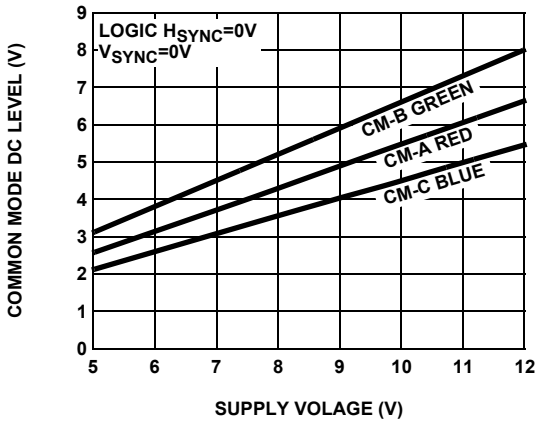


FIGURE 16. COMMON MODE DC LEVEL vs SUPPLY VOLTAGE

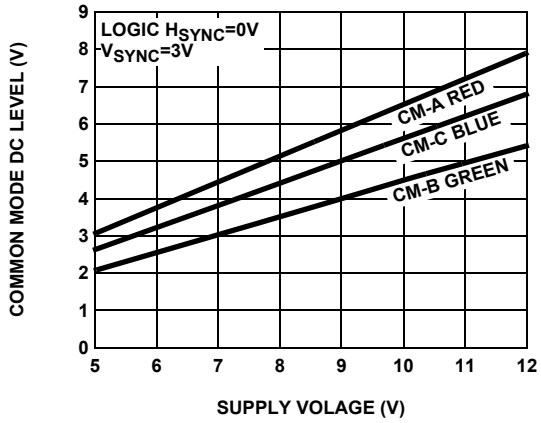


FIGURE 17. COMMON MODE DC LEVEL vs SUPPLY VOLTAGE

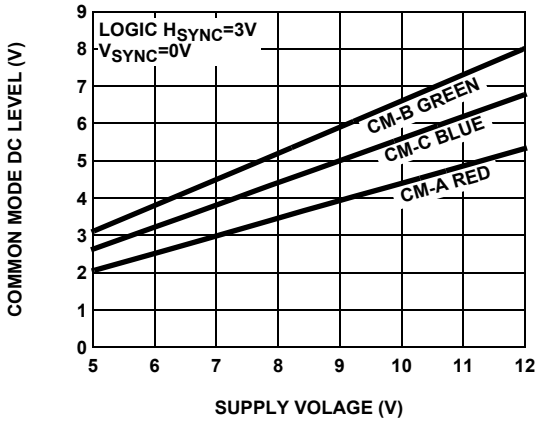


FIGURE 18. COMMON MODE DC LEVEL vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

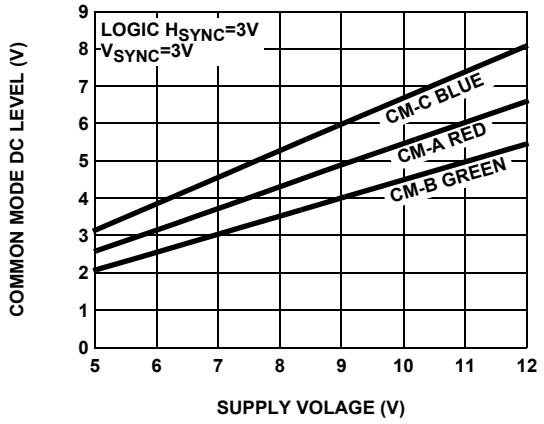


FIGURE 19. COMMON MODE DC LEVEL vs SUPPLY VOLTAGE

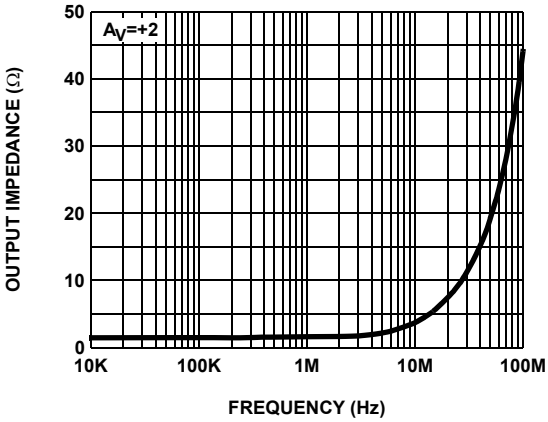


FIGURE 20. OUTPUT IMPEDANCE

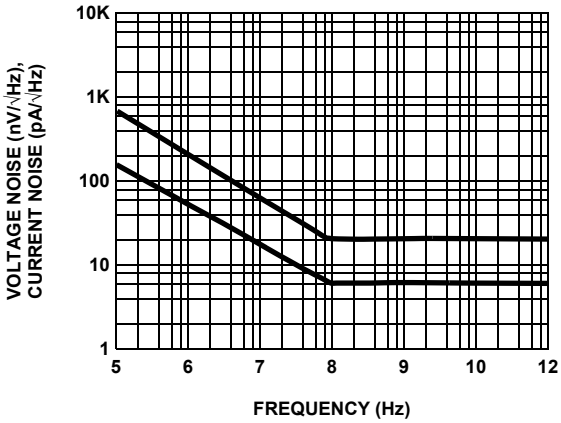


FIGURE 21. INPUT VOLTAGE AND CURRENT NOISE

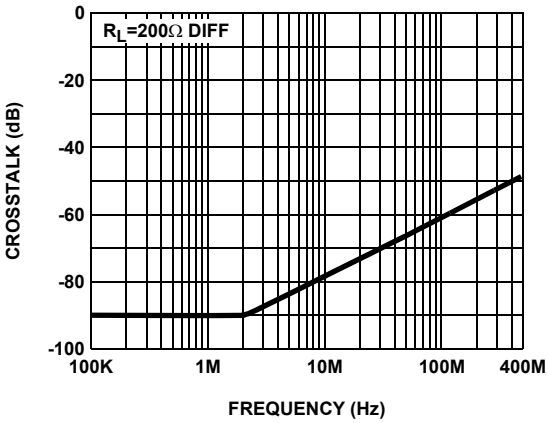


FIGURE 22. CHANNEL ISOLATION vs FREQUENCY

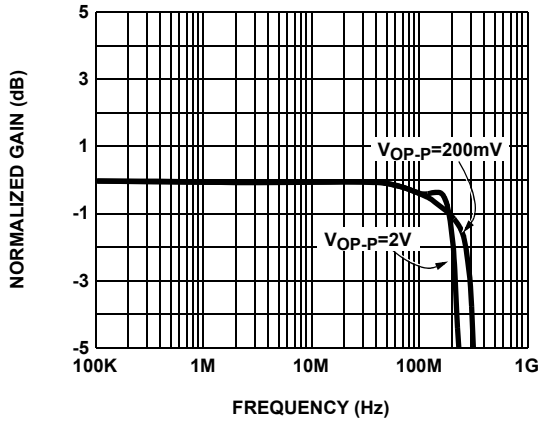


FIGURE 23. FREQUENCY RESPONSE vs OUTPUT AMPLITUDE

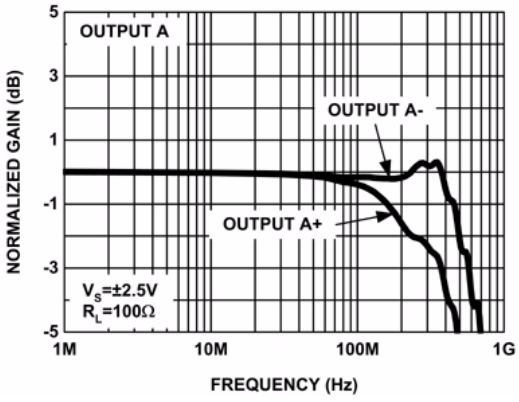


FIGURE 24. GAIN vs FREQUENCY - 2 CHANNELS

Typical Performance Curves (Continued)

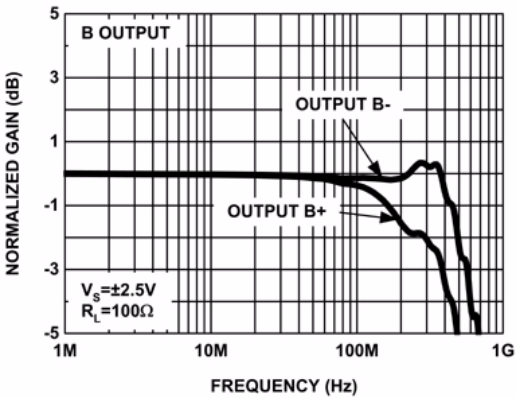


FIGURE 25. GAIN vs FREQUENCY - 2 CHANNELS

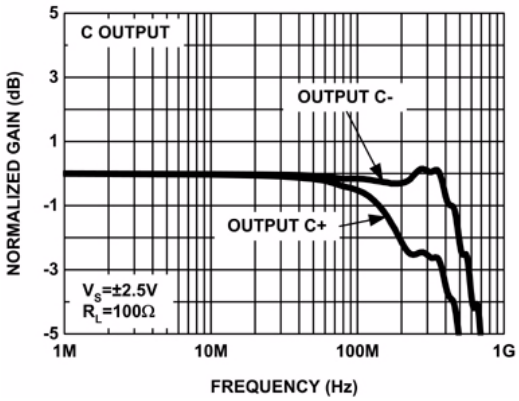


FIGURE 26. GAIN vs FREQUENCY - 2 CHANNELS

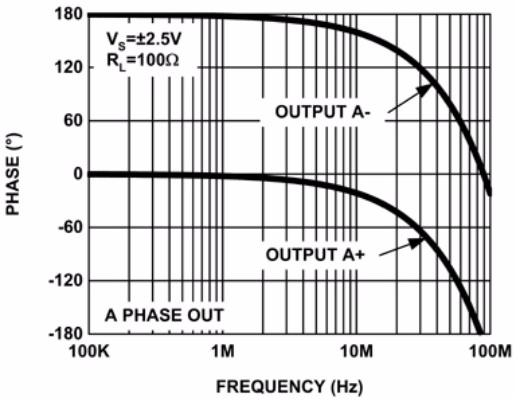


FIGURE 27. PHASE vs FREQUENCY - 2 CHANNELS

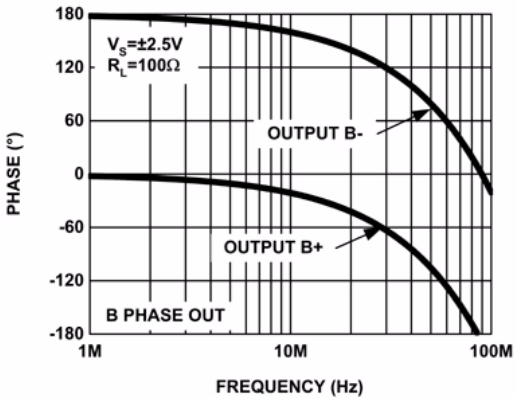


FIGURE 28. PHASE vs FREQUENCY - 2 CHANNELS

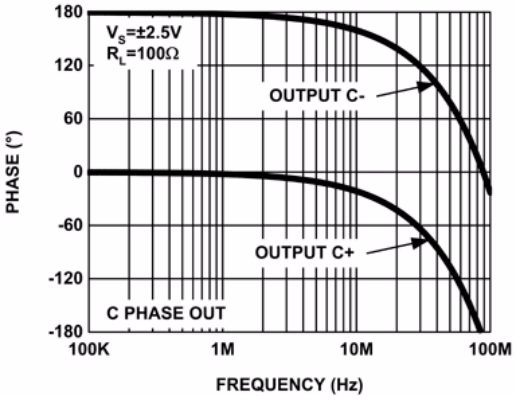


FIGURE 29. PHASE vs FREQUENCY - 2 CHANNELS

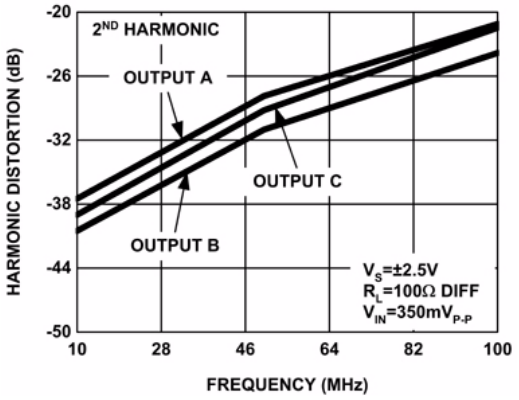


FIGURE 30. HARMONIC DISTORTION

Typical Performance Curves (Continued)

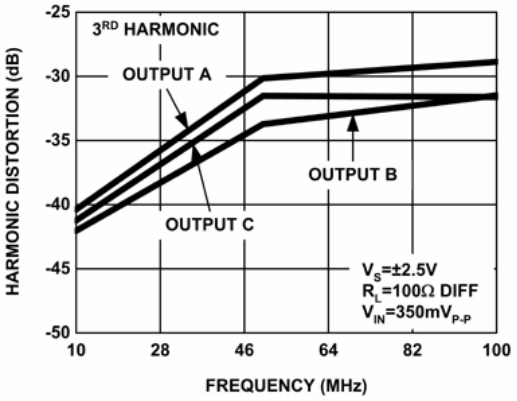


FIGURE 31. HARMONIC DISTORTION

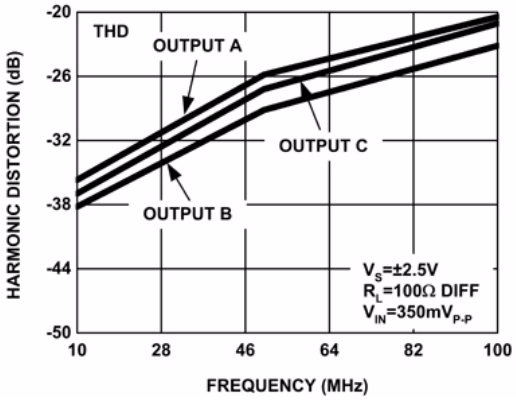


FIGURE 32. HARMONIC DISTORTION

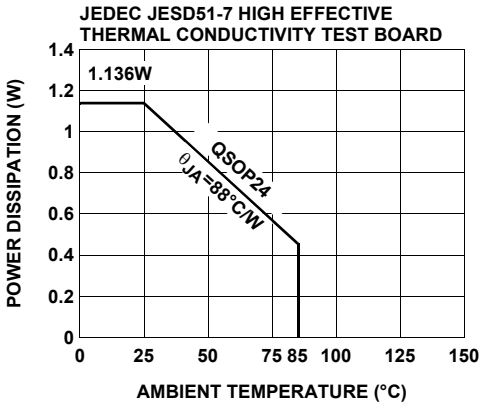


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

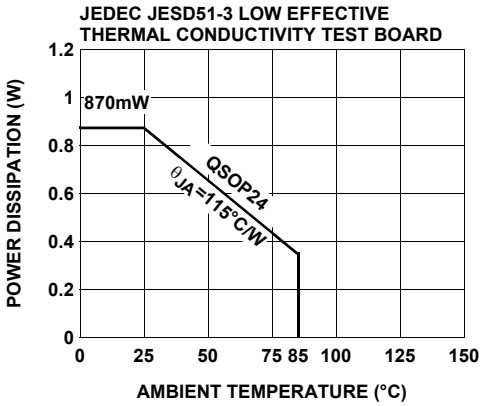


FIGURE 34. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

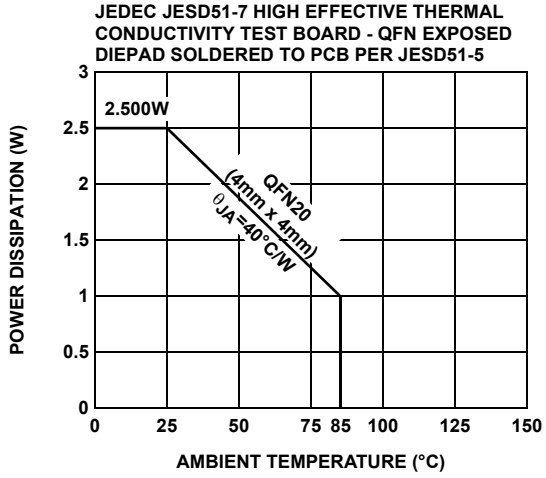


FIGURE 35. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

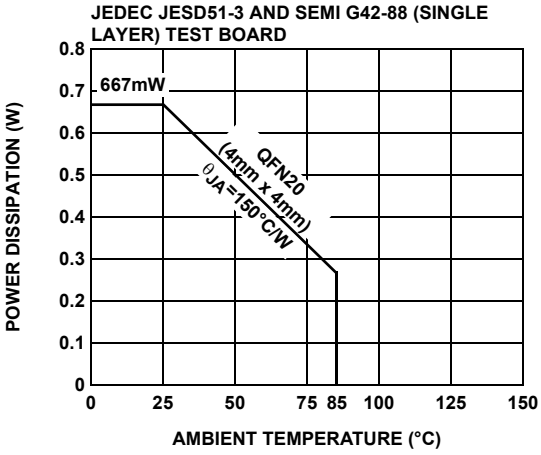


FIGURE 36. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Operational Description and Application Information

Introduction

The EL4543 is designed to differentially drive composite RGB video signals onto twisted pair lines, while simultaneously encoding horizontal and vertical sync signals as common mode output. The entire video signal plus sync can therefore be transmitted on 3 twisted pairs of wire. When utilizing CAT-5 cable, the 4th available twisted pair can be used for transmission of audio, data or control information. The distribution of composite video over standard CAT-5 cable enables enormous cost and labor savings compared with traditional coaxial cable, when considering both the relative low price and ease of pulling CAT-5 cable.

Functional Description

The EL4543 provides three fully differential high-speed amplifiers, suitable for driving high-resolution composite video signals onto twisted pair or standard coaxial cable. The input common-mode range extends to the negative rail, allowing simple ground-referenced input termination to be used with a single supply. The amplifiers provide a fixed gain of +2 to compensate for standard video cable termination schemes. Horizontal and Vertical sync signals (H_{SYNC} and V_{SYNC}) are passed to an internal Logic Encoding Block to encode the sync information as three discrete signals of different voltage levels. Generally, in differential amplifiers an external V_{REF} pin is used to control the common mode level of the differential output; in the case of the EL4543 the V_{REF} of each of the three internal amplifier channels receives a signal from the Logic Encoding Block with encoded H_{SYNC} and V_{SYNC} information. The final output consists of three fully differential video signals, with sync encoded on the common mode of each of the three RGB differential signals. H_{SYNC} and V_{SYNC} can easily be separated from the differential output signals, decoded and transmitted along with the RGB video signals to the video monitor.

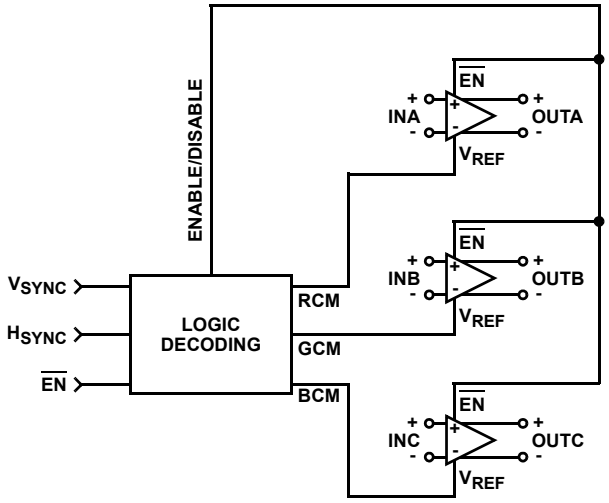


FIGURE 37. BLOCK DIAGRAM EL4543

Sync Transmission

The EL4543 encodes H_{SYNC} and V_{SYNC} signals on the common mode output of the differential video signals; Red, Green and Blue respectively. Data Sheet Figure 16, 17 and 18 clearly illustrate that the sum of the common mode voltages results in a fixed average DC level with no AC content and illustrates the logic levels. This eliminates EMI radiation into any common mode signal along the twisted pairs of CAT 5 cable.

Extract Common Mode Sync and Decode H_{SYNC} & V_{SYNC}

H_{SYNC} and V_{SYNC} can be regenerated from the Common Mode sync output voltages. The relationships between H_{SYNC}, V_{SYNC} and the 3 common mode levels are given by Table 1. The common mode levels are easily separated from the differential outputs of the EL4543 using this simple resistor network at the cable receiver input of each differential channel; see Figure 38.

Twisted Pair Termination

The schematic in Figure 38 illustrates a termination scheme for 50Ω series termination and a 100Ω twisted pair cable. Note RCM is the common mode termination to allow measurement of V_{CM} and should not be too small since it loads the EL4543; a little over a 100Ω is recommended for RCM.

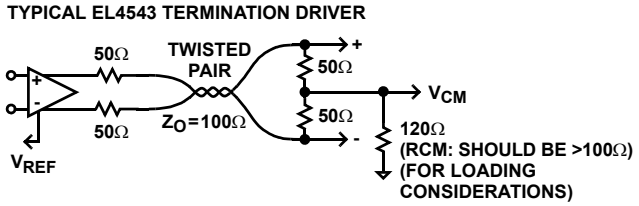


FIGURE 38. TWISTED PAIR TERMINATION EL4543

Video Transmission

The EL4543 is a twisted pair differential line driver directed at the transmission of Video Signals through cables up to 100 feet; however, as signal losses increase with transmission line length the EL4543 will need additional support to equalize video signals along longer twisted pair transmission lines. A full solution to accomplish this is the SXGA Video Transmission System presented in the EL4543 Data Sheet. Note the inclusion of the EL9110 for signal equalization of up to 1000ft of CAT-5 cable and common mode extraction; see Data Sheet for additional information on the EL9110.

Long Distance Video Transmission

The SXGA Video Transmission System makes it possible to transmit Red, Green and Blue (RGB) video plus sync up to 1000 feet through CAT-5 cable. The input to the SXGA Video Transmission System is the output of a video source transmitting RGB video signals plus sync. The signals are received initially by the EL4543; which converts the single

ended input RGB signals to three fully differential waveforms with sync encoded on the discrete common modes of each color channel and then drives the signals through a length of CAT-5 cable. The signal is received by the EL9110, which can provide 6-pole equalization for both high and low frequency signal transmission line losses. Then the EL9110 converts the differential RGB video signals back into single ended format while extracting the common mode component for decoding. The single ended RGB signal is taken directly from the output of the El9110 and is ready for the output device. The Common Mode Decoder Circuit receives the common mode signals directly from each of the three EL9110's common mode output pin, decodes and transmits H_{SYNC} and V_{SYNC} to the output device.

Sync Transmission

The EL4543 encodes H_{SYNC} and V_{SYNC} signals onto the common mode output of the differential video signals; Red, Green and Blue respectively. Data Sheet Figure 8 clearly illustrates that the sum of the common mode voltages results in a fixed DC level with no AC content; thus eliminating EMI interference.

Output Drive Protection

The EL4543 has internal short circuit protection set typically at 60mA. if the output is shorted for extended periods of time the increased power dissipation will eventually destroy the part. To realize maximum reliability the output current should never exceed 60mA. The 50Ω series back load matching resistor provides additional protection.

Supply Voltage

While the EL4543 can be operated on ±5V split rails, single supply 0V to 5V is the most common usage. It is very important to note that the input logic thresholds are relative to the negative supply pin, and therefore single supply, ground referenced logic will not work when driving the EL4543 on split rails. The amplifiers have an input common mode range from 0V to 3.5V with a 0V to 5V supply. The common mode output DC level range is a linear function of the power supply, see Data Sheet Figures 15, 16, 17 &18. The common mode input switching threshold as well as the Enable/Disable input is a linear function of the supply voltage, see Data Sheet Figure 1.

Disable and Power Down

The EL4543 provides an enable disable function which powers down, logic input high, in 900ns and powers up, logic input low, in 212ns. Disabled the amplifiers supply current is reduced to 1.8mA (Positive Supply) and 0mA (Negative Supply). Note that Enable/Disable threshold is a linear function of the supply voltage levels. The Enable/Disable threshold voltage level is compatible with standard TTL/CMOS and referenced to the lowest supply potential.

Proper Layout Technique

A critical concern with any PCB layout is the establishment of a “healthy” ground plane. It is imperative to provide ground planes terminated close to inputs to minimize input capacitance. Additionally, the ground plane can be selectively removed from inputs to prevent load and supply currents from flowing near the input nodes.

In general the following guidelines apply to all PCB layout:

- Keep all traces as short as possible.
- Keep power supply bypass components as close to the chip as possible - extremely close.
- Create a healthy ground with low impedance and continuous ground pathways available to all grounded components board-wide.
- In high frequency applications on multi-level boards try to keep one level of board with continuous ground plane and minimum via cutouts - providing it is affordable.
- Provide extremely short loops from power pin to ground.
- If it is affordable, a ferrite bead is always of benefit to isolate device from Power Supply noise and the rest of the circuit from the noise of the device.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL4543 drive capability is ultimately limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting package type. Power dissipation may be calculated:

$$PD = (V_S \times I_S) \times \sum_{1}^{4}(C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

- V_S is the total power supply to the EL4543 (from V_S+ to V_S-)
- V_{OUT} is the swing on the output (V_H - V_L)
- C_L is the load capacitance
- C_{INT} is the internal load capacitance (80pF max)
- I_S is the quiescent supply current (40mA max)
- f is frequency

Having obtained the application's power dissipation, the maximum junction temperature can be calculated:

$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times PD$$

where:

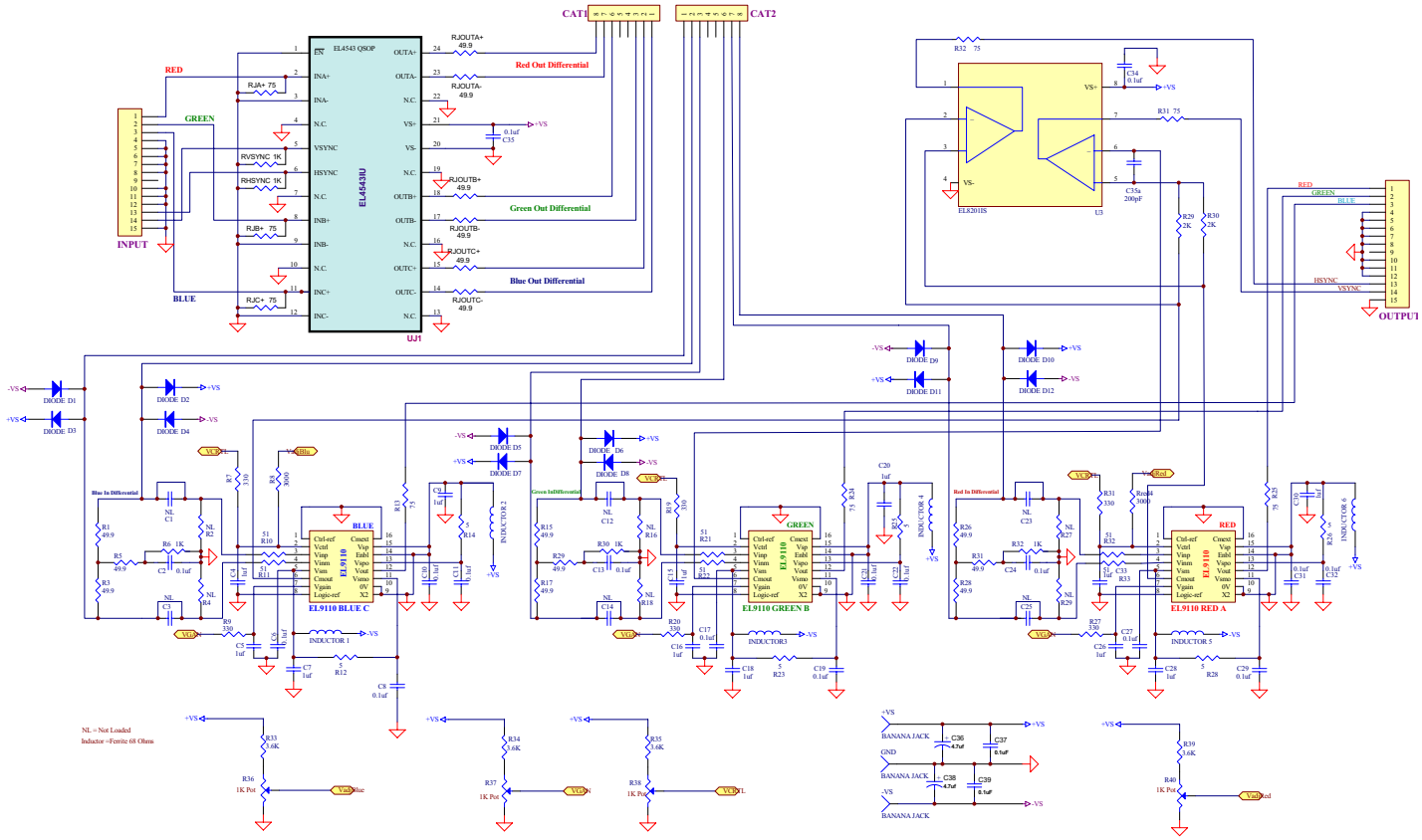
- T_{JMAX} is the maximum junction temperature (125°C)
- T_{MAX} is the maximum ambient operating temperature
- PD is the power dissipation calculated above
- θ_{JA} is the thermal resistance, junction to ambient, of the application (package + PCB combination). Refer to the Package Power Dissipation curves.

Application Circuit

Video Transmission Along CAT-5 Cable

VGA input RGB plus sync is connected with 75Ω termination to the inputs of the EL4543. Single-ended RGB video is converted to differential mode signals with H_{SYNC} and V_{SYNC} encoded on the common-mode of the three differential signals, respectively. The 50Ω output-terminated EL4543 drives the differential RGB with sync encoded common-mode to CAT-5 twisted pair cables. Note this system, without signal frequency equalization, will satisfactorily transmit along up to 200 feet of CAT-5 twisted-pair. For longer cable lengths, frequency and gain equalization to compensate for signal degradation is recommended (EL9110) and a delay line technology (EL9115) to adjust for phase mismatch between signals at the receiving end.

EL4543 & EL9110 Sync Extraction



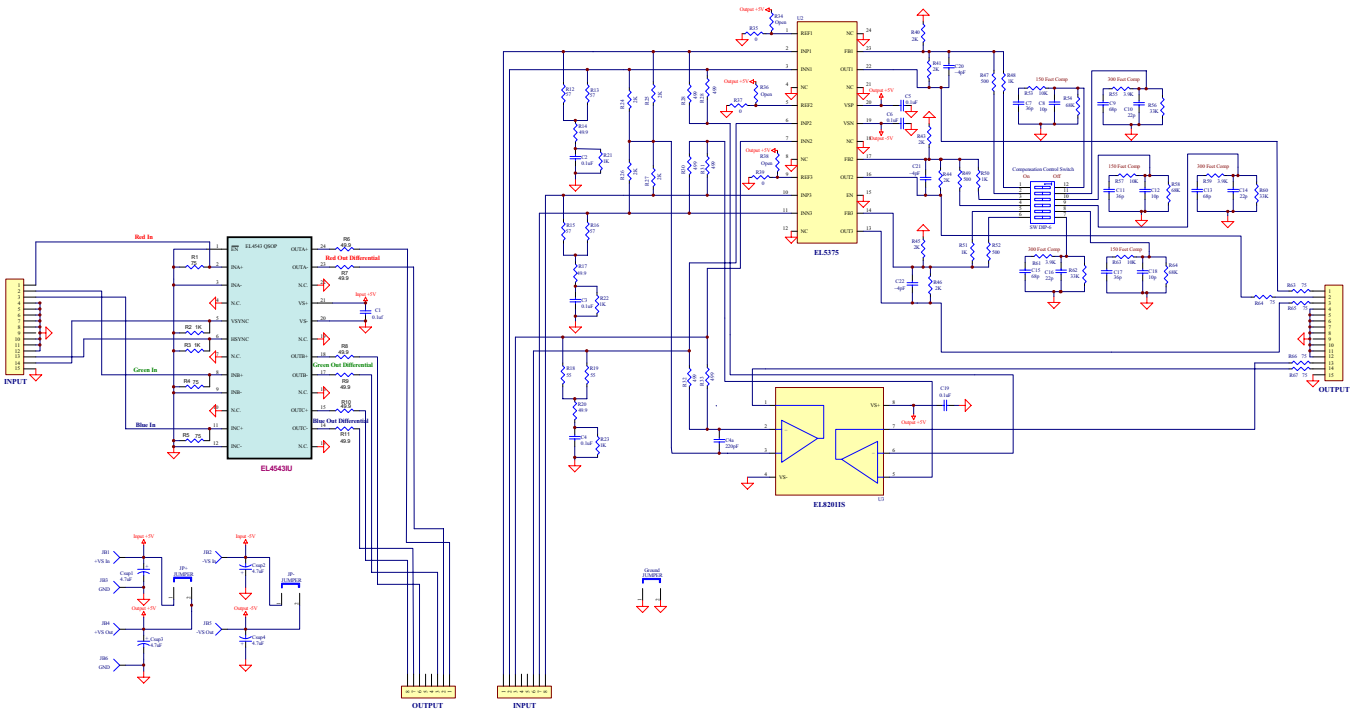
EL4543/EL5375/EL8201 CAT-5 RGB + Sync Video Transmission System

Introducing a low cost turn-key system for transmitting component video over short to moderate CAT-5 cable lengths (1 to 500 feet) with selectable cable loss and skew compensation. Using only 3 of the 4 pairs in standard CAT-5 the 4th pair is available for audio, function control or data transmission; an additional benefit.

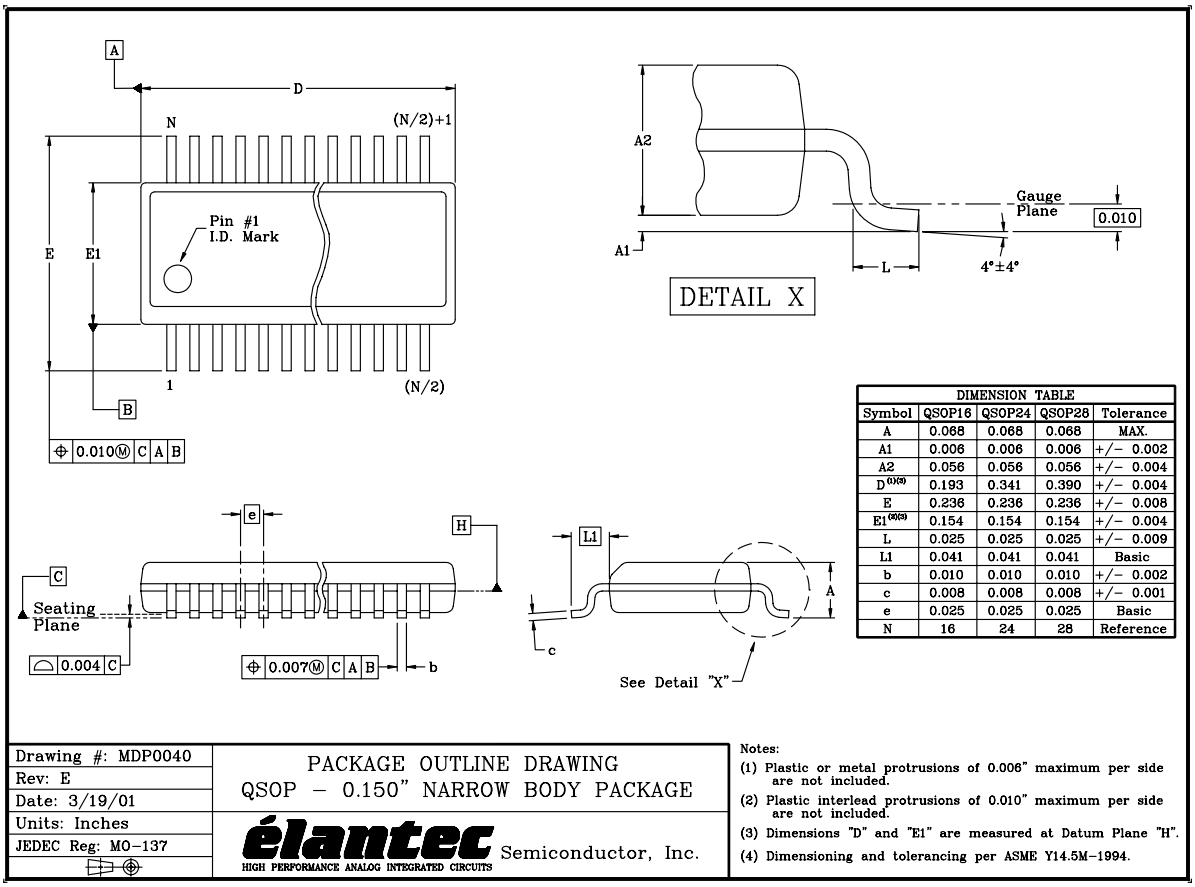
RGB video plus sync (5 channels) is received at the VGA terminal and presented single ended to the EL4543. The EL4543 converts single ended RGB into fully differential signals on three twisted pairs. Sync is encoded on the three RGB differential signals as differential common mode and then drives the differential signals with encoded sync through CAT-5 cable. The common mode of the signals is extracted from the differential signals with a passive network of resistors and passed to the EL8201 for sync decoding. The differential signal is passed directly to the EL5375 where it is amplified, converted back into single ended format. Signal attenuation occurs in all transmission lines as a function of increasing cable length; this application system utilizes individual channel 2-pole compensation for cable lengths of 150, 300 and 500 feet. Additionally, the compensation network can be manipulated to provide some measure of cable prop delay skew compensation for slight differences in cable lengths between CAT-5 pairs. Cable skew can best be done around the 300 ft range by under compensating the shortest color pair (color on the left side of a vertical line) and over compensate the longest color pair (color on the right side of a vertical line). Around 450 ft only the shortest color pair can be under compensated.

The board for the driver and receiver should use strip lines or strip line waveguides for the inputs and outputs of the drivers and receivers. The 75Ω input and output strip lines waveguide on 0.06 inch epoxy board with ground back plain should be 0.016 inch wide with 0.01 inch space to ground area around them. The diff pair strip line waveguides should be two 0.045 inch 50Ω lines spaced 0.01 inch apart and spaced 0.01 inch to ground area around them. This is a general guide and size values may very for many reasons.

The receiver feedback and gain resistor network which goes directly to the minus input should be connected very close with minimal trace length and minimal capacitance to ground. The ground plane on the backside of the board, in back of these resistors and the minus input pin should be removed as well.



QSOP Package Outline Drawing

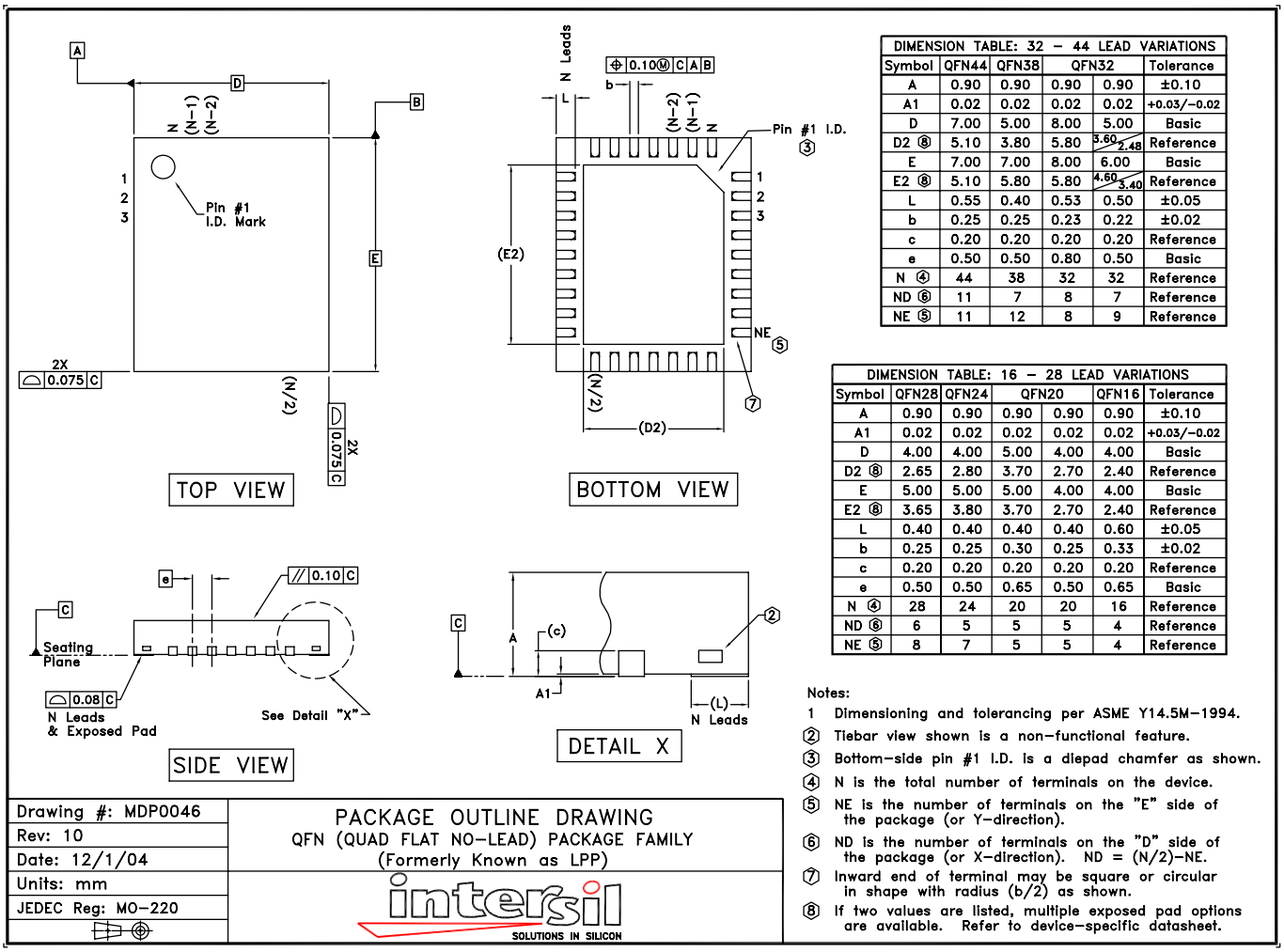


DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/− 0.002
A2	0.056	0.056	0.056	+/− 0.004
D(1)(3)	0.193	0.341	0.390	+/− 0.004
E	0.236	0.236	0.236	+/− 0.008
E1(2)(3)	0.154	0.154	0.154	+/− 0.004
L	0.025	0.025	0.025	+/− 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/− 0.002
c	0.008	0.008	0.008	+/− 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040	PACKAGE OUTLINE DRAWING QSOP – 0.150" NARROW BODY PACKAGE
Rev: E	
Date: 3/19/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO–137	

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M–1994.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/−0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/−0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑥	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING QFN (QUAD FLAT NO–LEAD) PACKAGE FAMILY (Formerly Known as LPP)
Rev: 10	
Date: 12/1/04	
Units: mm	
JEDEC Reg: MO–220	intersil SOLUTIONS IN SILICON

NOTE: The package drawings shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp

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