HM-65262/883

16K x 1 Asynchronous CMOS Static RAM

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Access Time . . . . . 70/85ns Max**
- **Low Standby Current. . . . . 50µA Max**
- **Low Operating Current . . . . . 50mA Max**
- **Data Retention at 2.0V. . . . . 20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout**
- **No Clocks or Strobes Required**
- **Temperature Range . . . . . +55°C to +125°C**
- **Gated Inputs-No Pull-Up or Pull-Down Resistors Required**
- **Equal Cycle and Access Time**
- **Single 5V Supply**

Description

The HM-65262/883 is a CMOS 16384 x 1-bit Static Random Access Memory manufactured using the Intersil Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262/883 is available in both JEDEC Standard 20 pin, 0.300 inch wide CERDIP and 20 pad CLCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

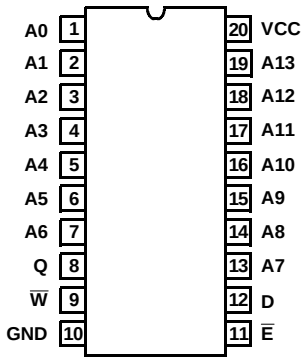
The HM-65262/883, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Ordering Information

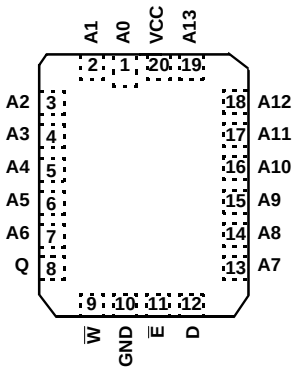
70ns/20µA	85ns/20µA	85ns/400µA	TEMP. RANGE	PACKAGE	PKG. NO.
-	HM1-65262/883	-	-55°C to +125°C	CERDIP	F20.3
HM4-65262B/883	HM4-65262/883	-	-55°C to +125°C	CLCC	J20.C

Pinouts

HM1-65262/883 (CERDIP)
TOP VIEW

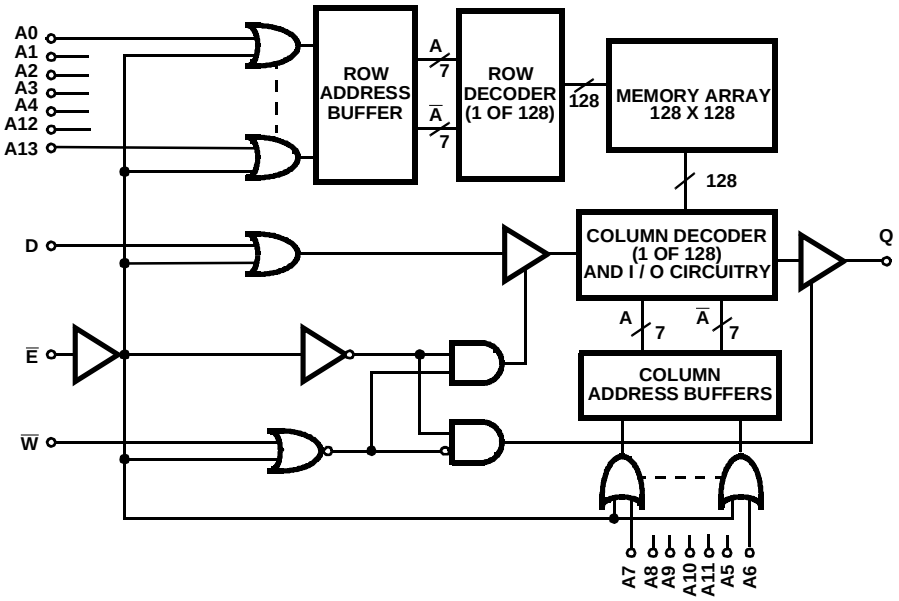


HM-65262 (CLCC)
TOP VIEW



A0 - A13	Address Input
$\overline{E}$	Chip Enable/Power Down
Q	Data Out
D	Data In
VSS/GND	Ground
VCC	Power (+5)
$\overline{W}$	Write Enable

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades . . . . . -0.3V to VCC +0.3V
Typical Derating Factor. . . . . .5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package.	$66^oC/W$	$13^oC/W$
CLCC Package	$75^oC/W$	$18^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range. . . . . -55^oC to $+125^oC$
Input Low Voltage. . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . . ±2.2V to VCC
Data Retention Supply Voltage . . . . . 2.0V to 4.5V
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. HM-65262/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	MIN	MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -4.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 8.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IOZ	VCC = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	50	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	20	µA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	50	mA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. HM-65262/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

AC PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	HM-65262B/883 LIMITS		HM-65262/883 LIMITS		UNITS
					MIN	MAX	MIN	MAX	
Read/Write/Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	85	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	85	ns

TABLE 2. HM-65262/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

AC PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	HM-65262B/883 LIMITS		HM-65262/883 LIMITS		UNITS
					MIN	MAX	MIN	MAX	
Chip Enable to End of Write	(3) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Chip Enable Access Time	(4) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	85	ns
Address Hold Time	(5) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Setup Time	(6) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Valid to End of Write	(7) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(9) TEHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Valid to End of Writes	(10) TAVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Write Enable Pulse Write	(11) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	45	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	35	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Enable Pulse Width	(14) TELEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Write to End of Write	(15) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	45	-	ns
Data Setup Time	(16) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	35	-	ns
Data Hold Time	(17) TEHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-65262/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 2	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 3	$T_A = +25^oC$	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 3	$T_A = +25^oC$	-	8	pF

TABLE 3. HM-65262/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Write Enable to Output in High Z	(18) TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	40	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	0	-	ns
Chip Enable to Output ON	(20) TELQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	40	ns
Chip Disable to Output Hold Time	(22) TE-HQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
High Level Output Voltage	(24) VOH2	VCC = 4.5V, IO = -100mA	1	$-55^oC \le T_A \le +125^oC$-	VCC -0.4V	-	V

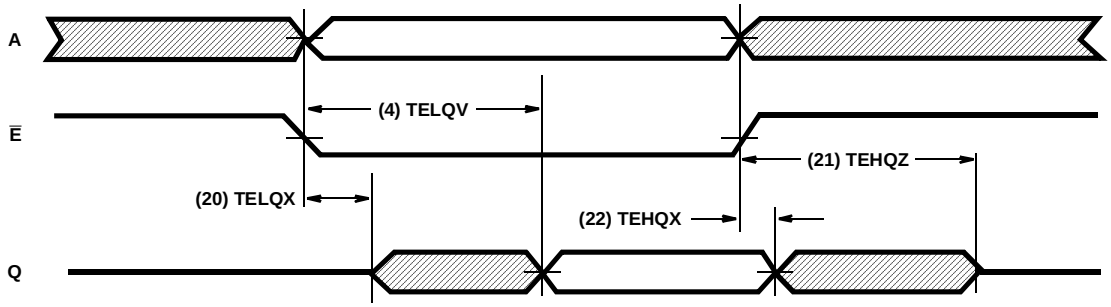
NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

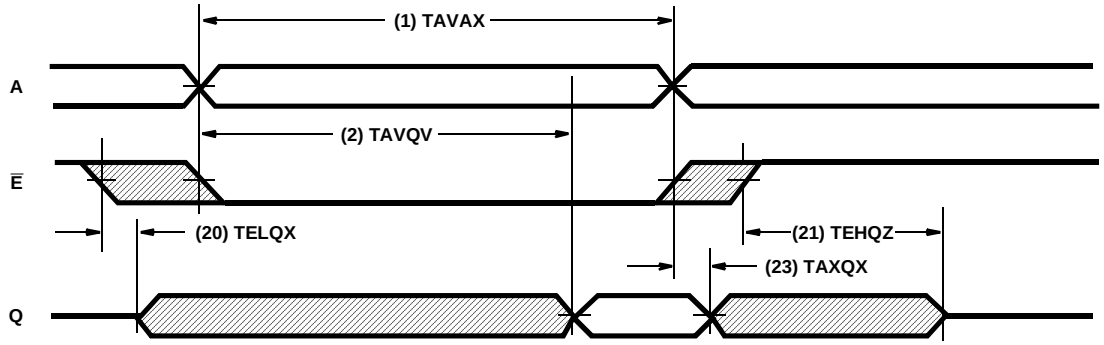
Timing Waveforms



NOTE:

1. $\overline{W}$ is high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

FIGURE 1. READ CYCLE 1: CONTROLLED BY $\overline{E}$

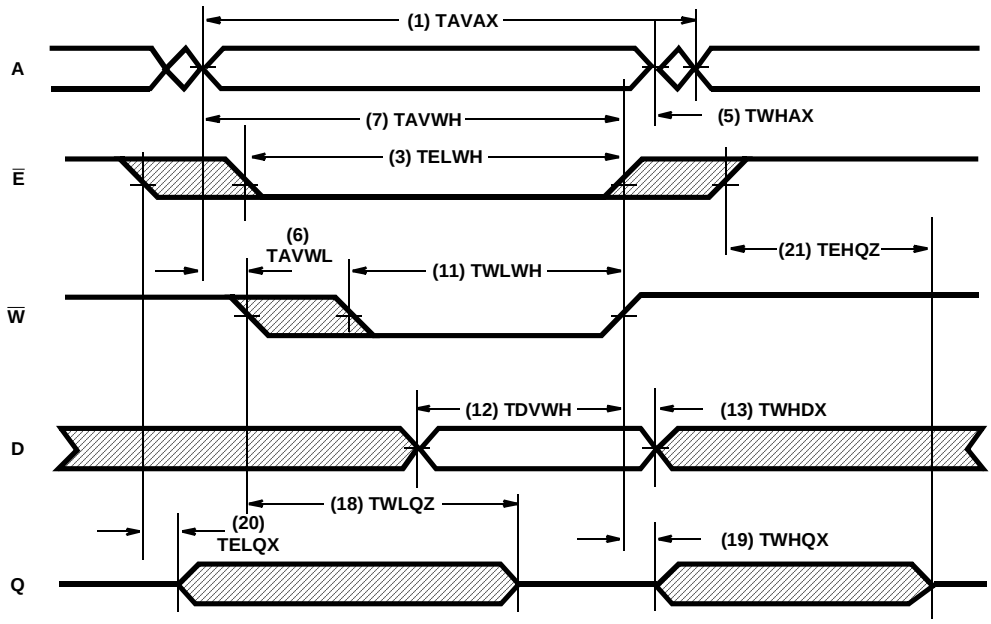


NOTE:

1. $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

FIGURE 2. READ CYCLE 2: CONTROLLED BY ADDRESS

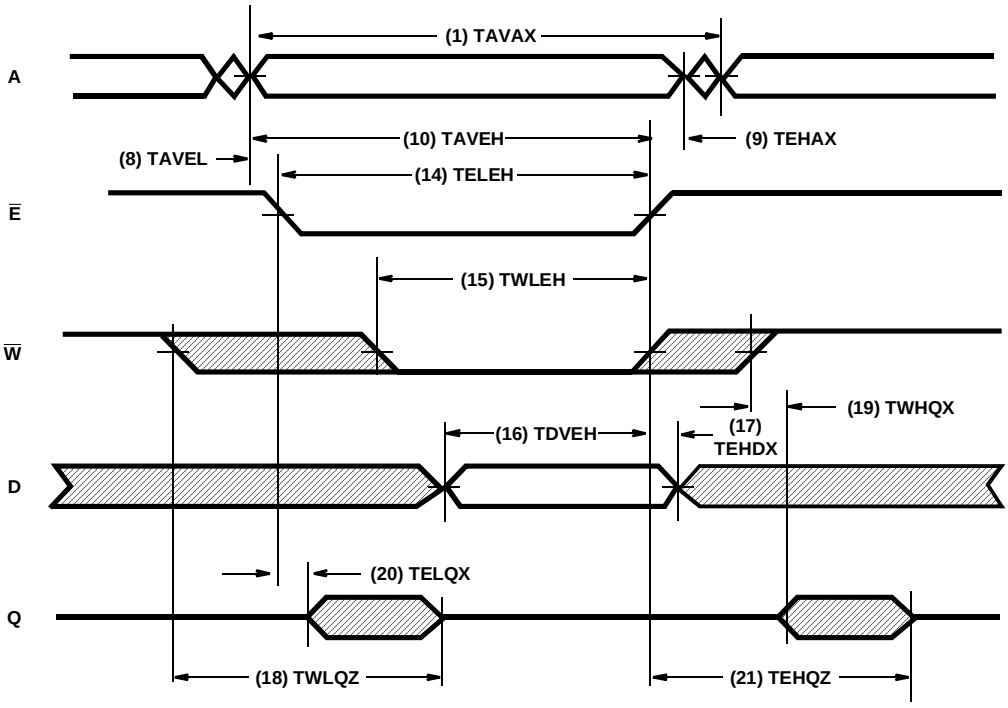
Timing Waveforms (Continued)



NOTE:

1. In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

FIGURE 3. WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE:

1. In this mode, $\overline{W}$ rises after $\overline{E}$. If W falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

FIGURE 4. WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)

Low Voltage Data Retention

Intersil CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation >55ns after VCC reaches the minimum operating voltage (4.5V).

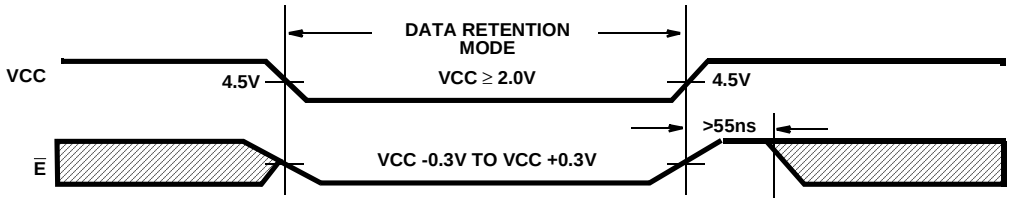
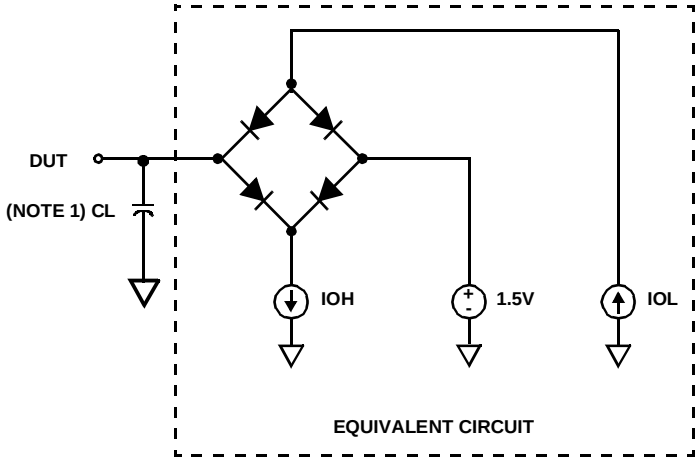


FIGURE 5. DATA RETENTION TIMING

Test Circuit

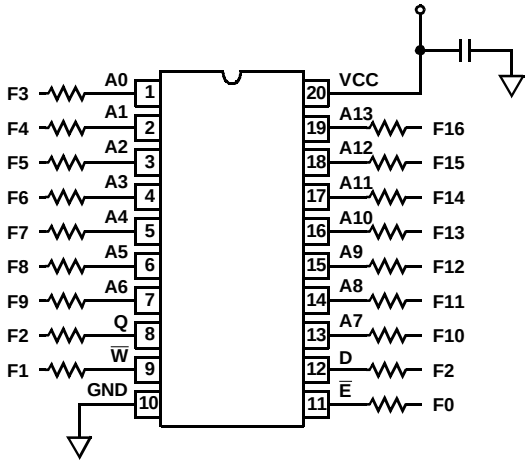


NOTE:

1. Test head capacitance includes stray and jig capacitance.

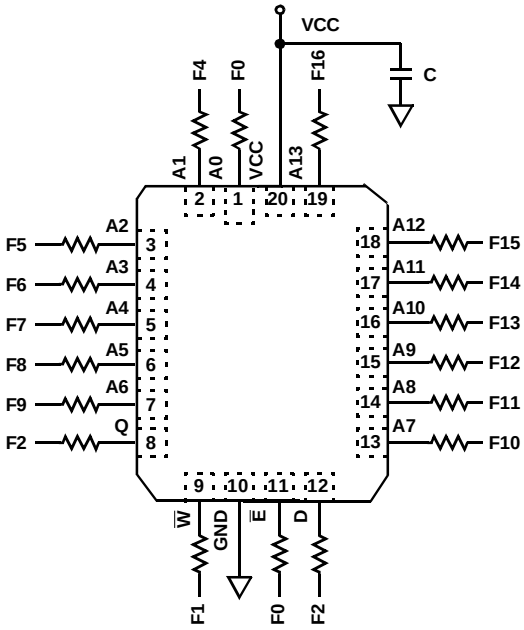
Burn-In Circuits

HM-65262/883
CERDIP
TOP VIEW



NOTES:
All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C = 0.01μF Min.

HM-65262/883
CLCC
TOP VIEW



NOTES:
All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C = 0.01μF Min.

Die Characteristics

DIE DIMENSIONS:
148 x 187 x 19 mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.2×10^5 A/cm^2

Metallization Mask Layout

HM-65262/883