Intel® PXA27x Processor Reference Platform

User's Guide

September 2004

Version 1.4

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Revision History

Date	Revision	Description
April 2004	001	Initial Version
May 2004	002	Updates for version 1.2
September 2004	003	Updates for version 1.4

Introduction and Startup 1

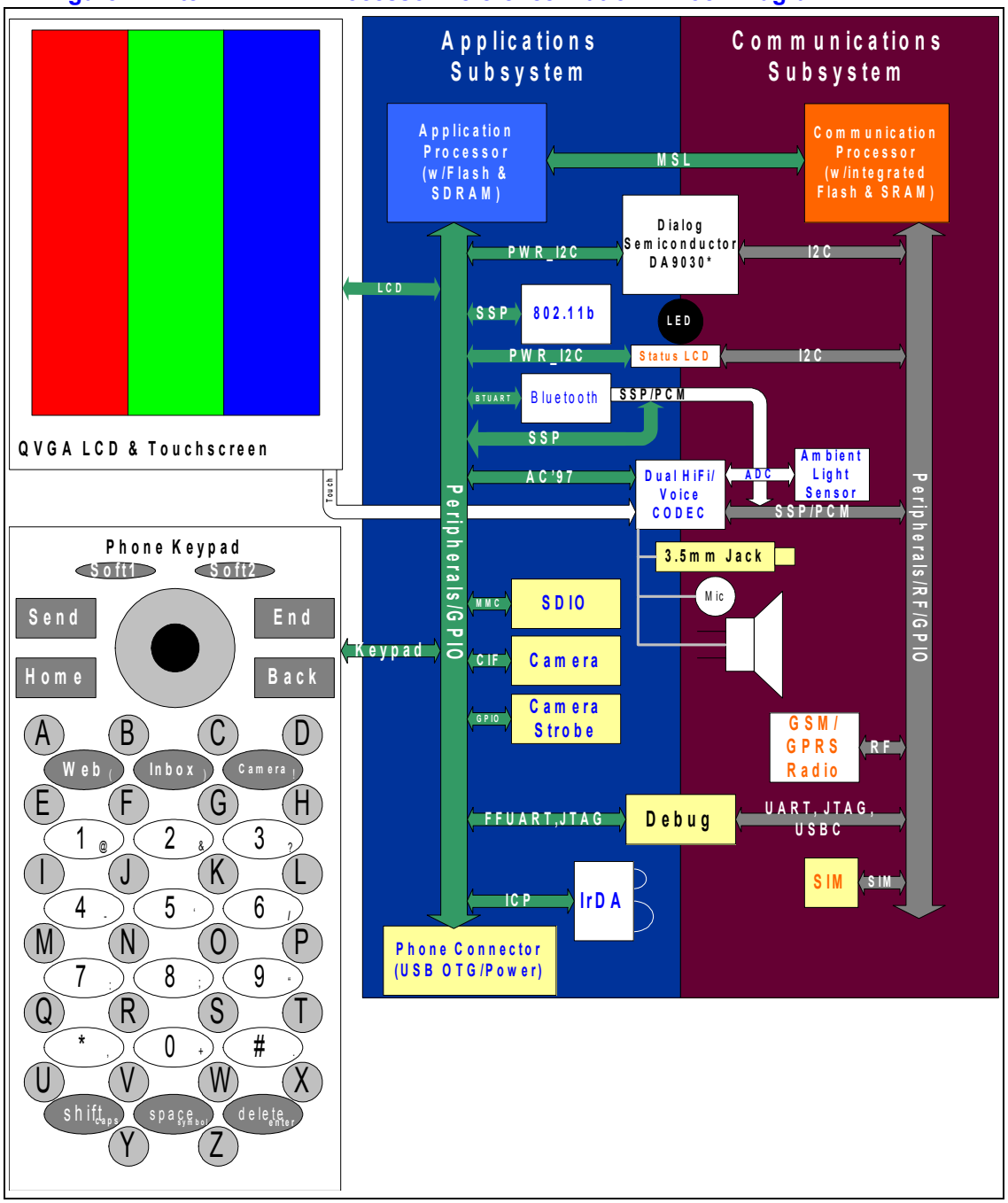
1.1 System Overview

The Intel® PXA27x Processor Reference Platform includes numerous peripherals that are available to the end user. The feature set consists of:

- High-performance processor, Intel® PXA27x Processor (PXA27x processor), which handles the running of a full-featured operating system (FFOS) and the man-machine interface peripherals (keyboards, LCD, etc.)
- High Performance communications processor, which handles the GSM/GPRS cellular protocol stack, the control for the GSM/GPRS radio, and the SIM interface
- Quad-band GSM cellular radio, supporting GPRS
- Bluetooth* radio, Bluetooth 1.1 compliant
- Wireless LAN 802.11b baseband and radio
- 240x320 pixel QVGA, 16 bit-per-pixel main LCD
- Five-line sub-LCD character display
- Alphanumeric keypad with dedicated alphabet keys, soft keys, and five-way directional pad
- High-fidelity stereo audio
- Notification LED
- Integrated 1.3 Megapixel CMOS camera and flash
- MMC/SDIO port
- USB client connector with On-The-Go (OTG) support
- IrDA infrared transceiver with CIR capability
- Housing which supports "Flip-n-Twist" operation for PDA-style or phone-style usage

Note: Changing firmware or software, adding or removing hardware may cause damage to the Intel® PXA27x Processor Reference Platform.

Figure 1. Intel® PXA27x Processor Reference Platform Block Diagram



1.1.1 User Interface

The user interface is comprised of a touch screen, keypad, and two LCDs that support data applications and cell-phone communications.

1.1.2 Intel® PXA27x Processor

Intel® PXA27x Processor (PXA27x processor) adds several new features that help enable wireless devices to capture high quality images, extend battery life, and deliver fast multimedia performance. It is the third implementation of the Intel XScale® microarchitecture family, featuring an improved LCD controller, expanded card interface, and more conservative power management features. It is also the first processor in the family to include a baseband interface, integrated SRAM, a camera capture interface, scalable core frequencies and voltages, USB On-The-Go (OTG), full SDIO support, and an Intel coprocessor. The coprocessor extends the Intel XScale® microarchitecture capabilities by adding Intel® Wireless MMX™ functionality and additional audio and video processing operations.

1.1.3 Communications Processor

The communications processor is the first Intel® Personal Internet Client Architecture (Intel® PCA) cellular processor to be fully integrated in a high-performance, power efficient Intel XScale® core for implementing wireless protocols with an Intel® Micro Signal Architecture (Intel® MSA) GSM/GPRS baseband processor. This provides wireless modem functionality along with on-die 0.13mm Flash memory and SRAM. The MSA core is a dual multiply and accumulate (MAC) digital signal processor running at 104 MHz. This design enables the development of powerful, cost-effective, advanced third-generation wireless devices capable of running rich data applications.

The PXA27x processor and the communications processor communicate with each other through the Intel® Mobile Scalable Link (Intel® MSL), a high performance baseband interface providing throughput up to 192 Mbps.

1.1.4 Mobile Scalable Link (MSL)

The communications processor has an RF connection to the cellular system and is connected to the PXA27x processor using a standard link called the MSL. The MSL hardware is capable of running up to 52 MHz or has a data throughput of 192 Mbps, and it is used mainly for exchanging data packets between subsystems.

1.1.5 Dialog Semiconductor DA9030*

The Intel® PXA27x Processor Reference Platform receives its power primarily from the Dialog Semiconductor DA9030*. The DA9030* controls battery charging and manages power supplies.

1.1.6 Wireless Subsystems

The wireless subsystem supports headset, hands-free, personal area network, dial-up network, and object push profiles using Bluetooth* technology.

The Bluetooth* baseband+radio chip is connected using a Universal Asynchronous Receiver Transmitter (UART) connection; it also has serial Pulse Coded Modulation (PCM) interfaces to both the PXA27x processor and the communications processor. The PCM connection to the PXA27x processor is used during audio scenarios handled by the PXA27x processor, such as voice memo pad (VMP), voice recognition (VR), calendar/incoming e-mail alerts, and so on. The direct connection to the communications processor is used during cellular voice calls.

The wireless LAN (WLAN) allows mobile users to connect to a LAN through a wireless radio connection. WLAN enables higher productivity, functionality, and convenience by untethering the user from any single wired port and allowing the user to access his databases and services remotely.

1.2 Document Organization

This user's guide contains the following chapters:

Chapter 1, "Introduction and Startup" provides an introduction of the Intel® PXA27x Processor Reference Platform.

Chapter 2, "User Interface" describes the system overview and user interfaces.

Chapter 3, "Intel® PXA27x Processor" describes the PXA27x processor and provides instructions for its use.

Chapter 4, "Communications Processor and Audio Concept" describes the communications processor and provides instructions for its use.

Chapter 5, "Intel® PXA27x Processor Reference Platform System Power Management" describes the Intel® PXA27x Processor Reference Platform power management design and Intel® Mobile Scalable Link (MSL).

Chapter 6, "Intel® PXA27x Processor Reference Platform Wireless Subsystems" describes the wireless subsystem components.

1.3 Getting Started

The Intel® PXA27x Processor Reference Platform *Quick Start Guide*, packed with the Intel® PXA27x Processor Reference Platform, contains a current packing list and instructions for setting up and starting the system. The Quick Start Guide also contains updates that became available after the publication of this document.

1.4 Related Documents

Table 1. Related Documents

Item	Number
Intel® PXA27x Processor Reference Platform Schematics	278877
Intel® PXA27x Processor Reference Platform Parts List	278879
Intel® PXA27x Processor Reference Platform Quick Start Guide	278982
Diagnostics for the Intel® PXA27x Processor Reference Platform User's Guide	278983
Intel® PXA27x Processor Family Developer's Manual	280000

User Interface 2

This chapter describes the Intel® PXA27x Processor Reference Platform hardware.

- Section - 2.1 User Interface
- Section - 2.2 Power Input and Voltage Regulation

2.1 User Interface

Figure 2. Intel® PXA27x Processor Reference Platform Form Factor Overview

2.1.1 Liquid Crystal Displays (LCD)

The Intel® PXA27x Processor Reference Platform includes a primary and secondary (status) LCD.

2.1.1.1 Primary LCD

The primary LCD is capable of 16-bit color depth, 240x320 pixel resolution, and a native portrait orientation. Since the Intel® PXA27x Processor Reference Platform is ‘flip’ style, the primary LCD is not required to be ‘always-on’.

2.1.1.2 Secondary (Status) LCD

The secondary (status) LCD displays the phone and call status information. It is operational when the phone is ‘closed-flip’ and powered down when the phone is ‘open-flip’.

2.1.2 User Notifications

2.1.2.1 Light Emitting Diode (LED)

The design includes an LED for visual user notifications. The control of the blink rate and duty cycles of this LED is handled autonomously by the LED modulator controller within the Dialog Semiconductor DA9030*.

2.1.2.2 Silent/Audible Notifications

For silent and audible user notifications, the design utilizes a multi-function speaker.

2.1.2.2.1 Silent Alert* Motor Control

A test point provides for controlling an external Silent Alert* vibrator motor.

2.1.3 Touchscreen

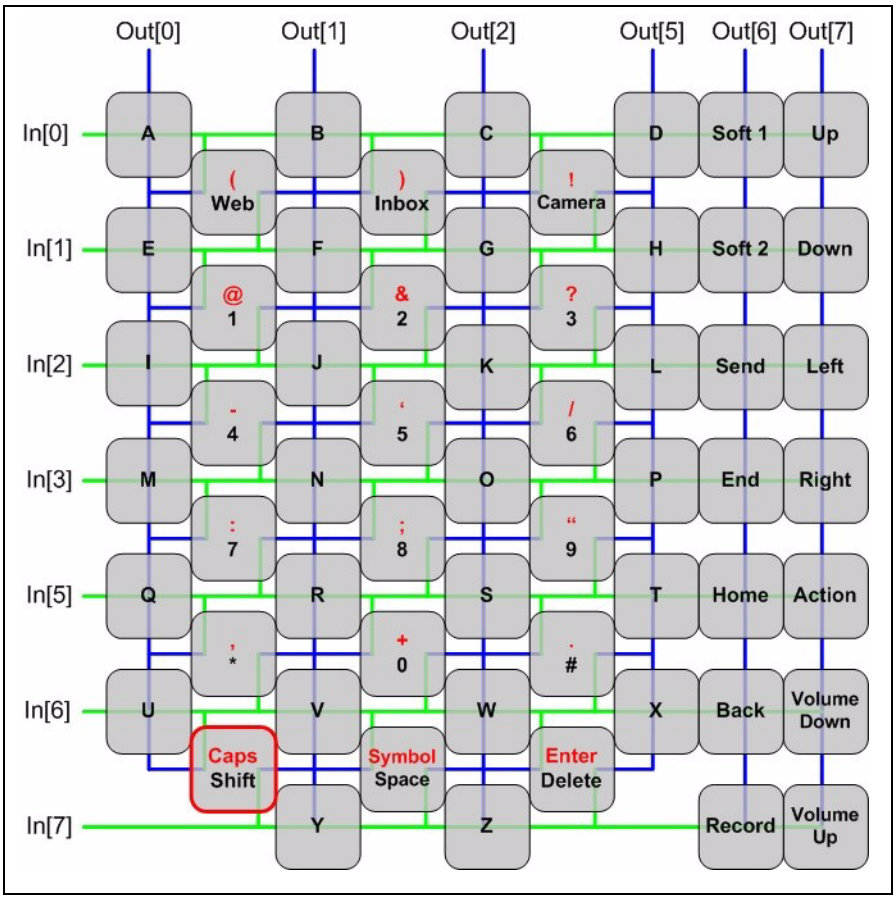
The touchscreen is mounted on the primary LCD. For operating systems that do not support a touch screen, the touch screen digitizer can be disabled or ignored.

2.1.4 Keypad

The keypad supports numeric entry capabilities, dedicated alphabet text entry capabilities, and navigation features.

Figure 3 shows the keypad logic.

Figure 3. Intel® PXA27x Processor Reference Platform Design Keypad Logic



Note: The keys in [] relate to the PXA27x processor GPIO keypad matrix.

Table 2. Intel® PXA27x Processor Reference Platform Keypad Logic

	Out0	Out1	Out2	Out5	Out6	Out7
In0	A	B	C	D	soft1	up
In1	E	F	G	H	soft2	down
In2	I	J	K	L	send	left
In3	M	N	O	P	end	right
In5	Q	R	S	T	home	action
In6	U	V	W	X	back	vol down
In7		Y	Z		record	vol up

	Out0&Out1	Out1&Out2	Out2&Out5
In0&In1	Web	Inbox	Camera
In1&In2	1	2	3
In2&In3	4	5	6
In3&In5	7	8	9
In5&In6	*	0	#
In6&In7	shift	space	delete

Shifted	Out0&Out1	Out1&Out2	Out2&Out5
In0&In1	(	)	!
In1&In2	@	&	?
In2&In3	-	'	/
In3&In5	:	;	"
In5&In6	,	+	.
In6&In7	caps	symbol	enter

2.1.5 Camera

The camera utilizes a 1.3 megapixel resolution CMOS imager that connects to the PXA27x processor's camera interface (for pixel data transfer) and I^2C interface (for command and control). It includes an integrated dual-mode, camera strobe/flash which contains a dimmer always-on mode for video capture and a flashlight capability and a brighter strobe mode for still picture capture capability. The camera can be used for both video conferencing and 'point-n-shoot' operation.

2.1.6 USB

The applications subsystem supports the USB OTG controller and the onboard transceivers in the PXA27x processor. It connects to other devices via an on-board mini type AB USB connector. A supply on the DA9030* generates the USB_VBUS supply.

2.1.7 Infrared

An IrDA transceiver is capable of supporting both serial infrared (SIR) and consumer infrared (CIR) operations.

2.1.8 Secure Digital

One on-board, full size secure digital socket supports a four-bit data bus width and SDIO operation.

2.1.9 Radio/Wireless

A quad band GSM/GPRS radio is supported for wireless communication.

2.1.10 Bluetooth*

The applications subsystem supports an onboard Bluetooth* baseband and RF module that comply with the Bluetooth 1.1 standard. The physical interfacing includes a PXA27x processor UART for control/data and a PCM link for Voice.

2.1.11 Wireless LAN (802.11b)

The applications subsystem supports an onboard 802.11b baseband and RF module. The physical interfacing utilizes a PXA27x processor SPI port for control and data.

2.2 Power Input and Voltage Regulation

The system derives its power from a single-cell lithium ion battery pack which mates with connector J5. The battery voltage is regulated down into the various power domains for the board by the DA9030*. Switch SW4 asserts the DA9030* ONKEY* signal, powering up the board and generating an interrupt from the DA9030* to the PXA27x processor. A DA9030* watchdog timer

is also started at this point. Software running on the PXA27x processor must disable this watchdog within eight seconds through a register write to the DA9030*. If eight seconds pass before this is done, the DA9030* will shut down.

Intel® PXA27x Processor 3

This chapter includes the following sections:

3.1 Hardware Description

Intel® PXA27x Processor (PXA27x processor) includes the following features.

3.1.1 Flash Memory and Boot ROM

The Intel® PXA271 Processor (PXA271 processor) contains 32 MBytes of Intel StrataFlash® memory and 32 MBytes of Low Power SDRAM.

The Intel® PXA27x Processor Reference Platform platform utilizes the PXA271 processor which uses chip select nCS[0], and boots from internal flash memory.

For more information on programming flash memory, see the JFlash release notes or the Intel® XDB JTAG Debugger release notes.

Additionally, the PXA271 processor has internal SDRAM, typically internally connected to chip select nSDCS[0].

3.1.2 Universal Serial Bus On-The-Go

The PXA27x processor contains a USB device controller that complies with the USBC 1.1 specification. It can also be used to produce A- and B-device, On-The-Go operations as specified in the On-The-Go supplement to the USB specification.

3.1.3 IrDA Infrared Transceiver

The main board contains a dual-mode Agilent IrDA transceiver capable of slow infrared (SIR) and consumer infrared (CIR) protocols. For more information about the transceiver's operation, refer to the Agilent HSDL-3002 data sheet.

The IrDA transceiver uses the PXA27x processor Infrared Communication Port.

3.1.4 Audio Codecs

A dual codec Wolfson WM9713 is included on the Intel® PXA27x Processor Reference Platform to produces HiFi audio over the AC'97 interface and a voice band codec over PCM.

3.1.5 Touch-Screen Controllers

The touchscreen controller is built into the Wolfson WM9713. This is a four wire touch panel controller supporting position measurements.

Keypad

The panel-mounted Fastap* keypad uses the PXA27x processor Keypad Interface, mapped as follows:

- The 55-button, 6x7 matrix keypad maps to the PXA27x processor matrix keypad signals MKIN<7:0> and MKOUT<7:0>.

3.1.6 MultiMediaCard* / Secure Digital* Card

The PXA27x processor contains a MultiMediaCard* (MMC), Secure Digital* (SD) card, and Secure Digital I/O controller. The main board socket supports both types of cards.

3.1.7 SIM Connector

The Subscriber Identity Module interface is a primary device and communications interface for a GSM mobile handset. The SIM interface also supports communication with SmartCards*, which are used in many applications including e-commerce. For the SIM Connector module, both 3.0 V and 1.8 V SIM cards are compatible.

3.1.8 Camera

The camera capture interface acquires data and control signals from the CMOS sensor. An Omnivision OV9640*, revision 3, 1.3 Mpixel camera module is standard.

3.1.9 Bluetooth* UART / Radio

A Philips BGB201 is connected to the PXA27x processor Bluetooth* UART.

3.1.10 Baseband

The baseband runs at 1.2 volts nominally and interfaces with the Intel® MSL module in the PXA27x processor.

3.2 Programming Guide

- Section 3.2.1 — Memory Map and Chip Selects
- Section 3.2.2 — Memory-Control Registers
- Section 3.2.3 — LCD-Control Registers
- Section 3.2.5 — Programming Application Flash Memory
- Section 3.2.6 — Flash Memory

3.2.1 Memory Map and Chip Selects

Table 3 describes the physical addresses and active-low chip selects for the PXA27x processor. For a complete listing of the PXA27x processor memory map, refer to the Memory Controller chapter in the *Intel® PXA27x Processor Family Developer's Manual*.

Table 3. Physical Addresses and Chip Selects (Sheet 1 of 2)

Function	Chip Select	Size	Base Address	Ending Address
Boot ROM flash memory	nCS0	32 Mbytes	0x0000_0000	0x03FF_FFFF
reserved	nCS1	64 Mbytes	0x0400_0000	0x07FF_FFFF
reserved	nCS2	6 Mbytes	0x0800_0000	0x0BFF_FFFF
reserved	nCS3	64 Mbytes	0x0C00_0000	0x0FFF_FFFF
Ethernet controller (Non-form factor Intel® PXA27x Processor Reference Platform only)	nCS4	64 Mbytes	0x1000_0000	0x13FF_FFFF
reserved	nCS5	64 Mbytes	0x1400_0000	0x17FF_FFFF
reserved	—	64 Mbytes	0x1800_0000	0x1BFF_FFFF
reserved	—	64 Mbytes	0x1C00_0000	0x1FFF_FFFF
reserved	—	256 Mbytes	0x2000_0000	0x2FFF_FFFF
reserved	—	256 Mbytes	0x3000_0000	0x3FFF_FFFF
Peripherals memory-mapped registers	—	64 Mbytes	0x4000_0000	0x43FF_FFFF
LCD memory-mapped registers	—	64 Mbytes	0x4400_0000	0x47FF_FFFF
Memory Control memory-mapped registers	—	64 Mbytes	0x4800_0000	0x4BFF_FFFF
USB host	—	64 Mbytes	0x4C00_0000	0x4FFF_FFFF
reserved	—	64 Mbytes	0x5000_0000	0x53FF_FFFF
reserved	—	64 Mbytes	0x5400_0000	0x57FF_FFFF
Internal memory control	—	64 Mbytes	0x5800_0000	0x5BFF_FFFF

Table 3. Physical Addresses and Chip Selects (Sheet 2 of 2)

Function	Chip Select	Size	Base Address	Ending Address
Internal memory storage	—	256 K	0x5C00_0000	0x5FFF_FFFF
reserved	—	256 Mbytes	0x6000_0000	0x6FFF_FFFF
reserved	—	256 Mbytes	0x7000_0000	0x7FFF_FFFF
reserved	—	256 Mbytes	0x8000_0000	0x8FFF_FFFF
reserved	—	256 Mbytes	0x9000_0000	0x9FFF_FFFF
SDRAM	nSDCS0	32 Mbytes	0xA000_0000	0xA3FF_FFFF
reserved	nSDCS1	64 Mbytes	0xA400_0000	0xA7FF_FFFF
reserved	nSDCS2	64 Mbytes	0xA800_0000	0xABFF_FFFF
reserved	nSDCS3	64 Mbytes	0xAC00_0000	0xAFFF_FFFF
reserved	—	256 Mbytes	0xB000_0000	0xBFFF_FFFF
reserved	—	256 Mbytes	0xC000_0000	0xCFFF_FFFF
reserved	—	256 Mbytes	0xD000_0000	0xDFFF_FFFF
reserved	—	256 Mbytes	0xE000_0000	0xEFFF_FFFF
reserved	—	256 Mbytes	0xF000_0000	0xFFFF_FFFF

3.2.2 Memory-Control Registers

The following subsections provide the recommended settings for the memory-control registers. These settings are required for proper operation of the PXA27x processor in a stand-alone application *or* in combination with the main board. The following registers must be configured:

- Section 3.2.2.1 — SDRAM Configuration Register (MDCNFG)
- Section 3.2.2.2 — SDRAM Mode Register Set Configuration Register (MDMRS)
- Section 3.2.2.3 — SLP SDRAM Mode Register Set Configuration Register (MDMRSLP)
- Section 3.2.2.4 — SDRAM Memory Device Refresh Register (MDREFR)
- Section 3.2.2.5 — Static Memory Control Register 0 (MSC0)
- Section 3.2.2.6 — Static Memory Control Register 1 (MSC1)
- Section 3.2.2.7 — Static Memory Control Register 2 (MSC2)
- Section 3.2.2.8 — Expansion Memory Configuration Register (MECR)
- Section 3.2.2.9 — Synchronous Static Memory Configuration Register (SXCNFG)
- Section 3.2.2.10 — Expansion Memory Timing Configuration Registers: MCMEM0, MCMEM1, MCATT0, MCATT1, MCIO0, MCIO1

The recommended settings for the memory-control registers presume the following:

- Memory-controller clock frequency (CLK_MEM) = 91 MHz, based upon the value of L in the PXA27x processor Core Clock Configuration Register. See the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*.

- 32 MB of SDRAM installed, mapped as 1 device, 13 row-address bits, 9 column-address bits, and 16 data bits. Extended Mode Register in the SDRAMs set as follows:
  - All SDRAM banks are maintained in self-refresh (all PASR bits clear).
  - Temperature-compensated refresh (TCR) is set for 45° C.

  To set these SDRAM characteristics for each device, refer to the following information sources:

  — **SDRAM device registers:** PXA271 processor with 32 MBytes of SDRAM.

  — **Accessing the SDRAM registers:** PXA27x processor Special Low-Power SDRAM Mode Register Set Configuration register (see the Memory Controller chapter in the *Intel® PXA27x Processor Family Developer's Manual*)

It may be necessary to adjust the recommended settings, depending on the following:

- Desired clock sources — for example, core PLL instead of internal or external processor oscillator. See the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*.
- Run- and turbo-mode frequencies (MEM_CLK depends on the core run-mode frequency in the PXA27x processor Core Clock Configuration Register. See the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*.)
- Use of fast-bus mode (see the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*)
- Expansion-card presence and memory-bus configuration (PXA27x processor Static Memory Control Register 2 — see the Memory Controller chapter in the *Intel® PXA27x Processor Family Developer's Manual*.)
- Use of SDRAM extended low-power modes — refer to the following information sources:

  — **SDRAM device registers:** Refer to the *Intel® PXA27x Processor Family Developer's Manual*.

  — **Accessing the SDRAM registers:** PXA27x processor Special Low-Power SDRAM Mode Register Set Configuration register (see the Memory Controller chapter in the *Intel® PXA27x Processor Family Developer's Manual*).

3.2.2.1 SDRAM Configuration Register (MDCNFG)

MDCNFG Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000			X	X	X	XX		X	XX		XX		X	XX		001			0	1	0	11		1	10†		01		1	01†	

† See "SDRAM Initialization", Memory Controller chapter, *Intel® PXA27x Processor Family Developer's Manual*

3.2.2.2 SDRAM Mode Register Set Configuration Register (MDMRS)

MDMRS Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Stand-alone Intel® PXA27x Processor *and* Intel® PXA27x Processor with Intel® PXA27x Processor Reference Platform main board																															
0	XXXX XXXX								011			0	010			0	0000 0000†								011			0	010		

† Burst reads, burst writes

3.2.2.3 SLP SDRAM Mode Register Set Configuration Register (MDMRSLP)

MDMRSLP Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	XXX XXXX XXXX XXXX															1	100 0000 0000 1000†														

† 45° C TCR, all banks PASR

3.2.2.4 SDRAM Memory Device Refresh Register (MDREFR)

When configuring this register, follow the procedure recommended in the *Intel® PXA27x Processor Family Developer's Manual* for initializing SDRAM.

MDREFR Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10	1[1]	0	0	0	0	0	0	0	0	0	1[2]	0	0	1[3]	1	1	0[4]	1	0	0000 0001 1110[5]											

NOTES:
1. SDCLK[0] = MEMCLK / 4
2. Auto Power-Down (APD) enabled for all except synchronous flash-memory devices.
   For more information on the APD function, see the MDREFR register description in the Memory Controller chapter of the *Intel® PXA27x Processor Family Developer's Manual*.
3. SDCLK[1] = 45.5 MHz
4. Overridden by MDREFR[29]
5. One refresh every 7.62 µs. This value may change, depending on the presence of an expansion board with SDRAM mapped to any of nSDCS<3:1>.

3.2.2.5 Static Memory Control Register 0 (MSC0)

Note: The flash-memory bank might not operate reliably at MEM_CLK = 130 MHz if all timing parameters are near worst-case conditions (long propagation delays). The first-access delay (t_{ELQV} in the 3-volt *Intel StrataFlash® Memory Data Sheet* for J3-family devices) is 150 ns. However, the maximum first-access delay allowed by the processor (MSC0[RDF0/1]) with MEM_CLK = 130 MHz (period = 7.69ns) is 192.3 ns. Thus, it might be necessary to select a run-mode frequency that produces a MEM_CLK frequency of 91 MHz or lower under normal operating conditions.

The table below shows how to program both nCS0 (synchronous flash memory on the PXA27x processor) and nCS1 (asynchronous flash memory on the main board) for asynchronous read accesses. The setting for nCS0 is optimized for CLK_MEM = 91 MHz.

Upon reset or power-up, the MEM_CLK frequency defaults to 91 MHz.

MSC0 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	XXX			XXXX				XXXX				X	XXX			0	111			1111				1111				1	010		

3.2.2.6 Static Memory Control Register 1 (MSC1)

The timing values shown in the following table are for the SRAM.

MSC1 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Stand-alone Intel® PXA27x Processor *and* Intel® PXA27x Processor with Intel® PXA27x Processor Reference Platform main board																															
0	000				0000				0000			0	000			1	010			0110				1001				0	001		

3.2.2.7 Static Memory Control Register 2 (MSC2)

MSC2 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Processor card with Intel® PXA27x Processor main board																															
X	XXX				XXXX				XXXX			X	XXX			0	011			1000				1000				0	100		

3.2.2.8 Expansion Memory Configuration Register (MECR)

MECR Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0X0																														X	1

3.2.2.9 Synchronous Static Memory Configuration Register (SXCNFG)

Before setting up SXCNFG, configure the PXA27x processor flash-memory devices for synchronous operation. To do this, refer to the *Intel® Synchronous StrataFlash® Memory Data Sheet* for the L18-family devices. In the Flash Configuration register for each device, set the first-access latency count (CR[13:11]) to 0b011.

SXCNFG Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	00		000 0000							001			00		0	1	00		000 0000										00	

3.2.2.10 Expansion Memory Timing Configuration Registers

The following table shows the settings for all six of these configuration registers.

Note: The values in the following table presumes a 250-ns card cycle time.

MCMEM0, MCMEM1, MCATT0, MCATT1, MCIO0, and MCIO1 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0000 0000												00 0111						00		0 0111					001 0001						

3.2.3 LCD-Control Registers

The following subsections provide the recommended settings for the PXA27x processor LCD-control registers. These settings are required for proper operation with the Sharp LS022Q8DD06, CG Silicon LCD Module (320x240).

The following registers must be configured:

- Section 3.2.3.1 — LCD Controller Control Register 0 (LCCR0)
- Section 3.2.3.2 — LCD Controller Control Register 1 (LCCR1)
- Section 3.2.3.3 — LCD Controller Control Register 2 (LCCR2)
- Section 3.2.3.4 — LCD Controller Control Register 3 (LCCR3)
- Section 3.2.3.5 — LCD Controller Control Register 4 (LCCR4)
- Section 3.2.3.6 — LCD Controller Control Register 5 (LCCR5)

The recommended settings for the LCD-control registers presume the following:

- Core is clocked off of the core PLL, with a core run-mode frequency of 130 MHz (L=10 in the Core Clock Configuration Register)
- The LCD-controller frequency is 65 MHz (see the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*)

It may be necessary to adjust the recommended settings, depending on the following:

- Custom clock configurations:
  - Clock sources
  - Run- and turbo-mode frequencies
  - Use of fast-bus mode

  For clock-configuration information, see the Clocks and Power Manager chapter in the *Intel® PXA27x Processor Family Developer's Manual*.
- Presence of an alternate LCD

3.2.3.1 LCD Controller Control Register 0 (LCCR0)

LCCR0 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 000							1	1	0	1	1	0000 0000								1	0	0	0	1	1	1	1	1	0	0	1

3.2.3.2 LCD Controller Control Register 1 (LCCR1)

LCCR1 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0111								0000 0000								0000 01						00 1110 1111									

3.2.3.3 LCD Controller Control Register 2 (LCCR2)

LCCR2 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000 0000								0000 0010								0000 10						01 0011 1111									

3.2.3.4 LCD Controller Control Register 3 (LCCR3)

LCCR3 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00		0	0	0	100			0	1	1	1	XXXX				0000 0000								0000 1000							

3.2.3.5 LCD Controller Control Register 4 (LCCR4)

LCCR4 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Toshiba LTM04C380K VGA																															
0x0															XX	0x0							XXX			XXX			XXX		
Toshiba LTM035A776C QVGA																															
0x0															XX	0x0							XXX			XXX			XXX		

3.2.3.6 LCD Controller Control Register 5 (LCCR5)

LCCR5 Recommended Settings:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Toshiba LTM04C380K VGA																															
00	X	X	X	X	X	X	00	X	X	X	X	X	X	00	X	X	X	X	X	X	00	X	X	X	X	X	X				
Toshiba LTM035A776C QVGA																															
00	X	X	X	X	X	X	00	X	X	X	X	X	X	00	X	X	X	X	X	X	00	X	X	X	X	X	X				

3.2.4 Intel® PXA27x Processor Pin Usage

Table 4. Intel® PXA27x Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

GPIO_Pin	Pin_Name	Direction	Description
0	GPIO[0]	I	nPMIC_INT; DA9030* interrupt
1	GPIO[1]	I	AC'97 Interrupt
2	SYS_EN	O	SYS_EN; System enable
3	PWR_SCL	O	PWR_SCL; Power I^2C clock
4	PWR_SDA	I/O	PWR_SDA; Power I^2C data
5	PWR_CAP[0]	-	PWR_CAP[0]; Sleep/deep-sleep regulator capacitor
6	PWR_CAP[1]	-	PWR_CAP[1]; Sleep/deep-sleep regulator capacitor
7	PWR_CAP[2]	-	PWR_CAP[2]; Sleep/deep-sleep regulator capacitor
8	PWR_CAP[3]	-	PWR_CAP[3]; Sleep/deep-sleep regulator capacitor
9	CLK_POUT	I	CLK_PIO; Processor clock
10	CLK_TOUT	O	CLK_TOUT; 32 kHz clock
11	EXT_SYNC[0]	I	802.11b interrupt
12	EXT_SYNC[1]	I	CIF_DD[7]; Camera data
13	CLK_EXT	I	KP_MKIN[7]; Keypad matrix in 7
14	L_VSYNC	I	SDIO Card Detect
15	nCS[1]	I	Hall Flip Sensor Closed
16	PWM_OUT[0]	O	LED Camera Strobe
17	PWM_OUT[1]	I	CIF_DD[6]; camera interface
18	RDY	I	RDY; Ready
19	L_CS	I/O	SSPSCLK2; Audio PCM Clock
20	nSDCS[2]	I	Hall Flip Sensor Flipped
21	nSDCS[3]	I	Ethernet Interrupt
22	SSPEXTCLK2	O	KP_MKOUT[7]; keypad output
23	SSPSCLK	O	CIF_MCLK; Camera master clock
24	SSPSFRM	I	CIF_FV; Camera frame sync
25	SSPTXD	I	CIF_LV; Camera line sync
26	SSPRXD	I	CIF_PCLK; Camera pixel clock
27	SSPEXTCLK	I	CIF_DD[0]; Camera data
28	BITCLK	I	AC97_BITCLK; AC97 bit clock
29	SDATA_IN	I	AC97_SDATA_IN_0; AC97 data in
30	SDATA_OUT	O	AC97_SDATA_OUT; AC97 data out

Table 4. Intel® PXA27x Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

GPIO_Pin	Pin_Name	Direction	Description
31	SYNC	O	AC97_SYNC; AC97 synch
32	MMCLK	O	MMCLK; MMC clock
33	nCS[5]	I/O	General Purpose Switch or LED
34	FFRXD	I	FFRXD; FFUART receive
35	FFCTS	I/O	SSPSFRM3; WLAN slave select
36	SSPSCLK2	O	USB_P2_4; USB OTG
37	SSPSFRM2	O	USB_P2_8; USB OTG
38	SSPTXD2	O	SSPTXD3; WLAN transmit
39	FFTXD	O	FFTXD; FFUART transmit
40	SSPRXD2	O	SSPSCLK3; WLAN clock
41	FFRTS	I	USB_P2_7; USB OTG
42	BTRXD	I	BTRXD; Bluetooth* receive
43	BTTXD	O	BTTXD; Bluetooth* transmit
44	BTCTS	I	BTCTS; Bluetooth* clear to send
45	BTRTS	O	BTRTS; Bluetooth* request to send
46	ICP_RXD	I	ICP_RXD; Infrared receive
47	ICP_TXD	O	ICP_TXD; Infrared transmit
48	BB_OB_DAT[1]	O	BB_OB_DAT[1]; MSL outbound data 1
49	nPWE	O	nPWE [Ethernet]; Ethernet/ PCMCIA work enabled
50	BB_OB_DAT[2]	O	BB_OB_DAT[2]; MSL outbound
51	BB_OB_DAT[3]	O	BB_OB_DAT[3]; MSL outbound
52	BB_OB_CLK	O	BB_OB_CLK; MSL clock
53	BB_OB_STB	O	BB_OB_STB; MSL strobe
54	BB_OB_WAIT	I	BB_OB_WAIT; MSL wait
55	BB_IB_DAT[1]	I	BB_IB_DAT[1]; MSL inbound data
56	BB_IB_DAT[2]	I	BB_IB_DAT[2]; MSL inbound data
57	BB_IB_DAT[3]	I	BB_IB_DAT[3]; MSL inbound data
58	L_DD[0]	O	L_DD[0]; LCD data
59	L_DD[1]	O	L_DD[1]; LCD data
60	L_DD[2]	O	L_DD[2]; LCD data
61	L_DD[3]	O	L_DD[3]; LCD data
62	L_DD[4]	O	L_DD[4]; LCD data
63	L_DD[5]	O	L_DD[5]; LCD data

Table 4. Intel® PXA27x Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

GPIO_Pin	Pin_Name	Direction	Description
64	L_DD[6]	O	L_DD[6]; LCD data
65	L_DD[7]	O	L_DD[7]; LCD data
66	L_DD[8]	O	L_DD[8]; LCD data
67	L_DD[9]	O	L_DD[9]; LCD data
68	L_DD[10]	O	L_DD[10]; LCD data
69	L_DD[11]	O	L_DD[11]; LCD data
70	L_DD[12]	O	L_DD[12]; LCD data
71	L_DD[13]	O	L_DD[13]; LCD data
72	L_DD[14]	O	L_DD[14]; LCD data
73	L_DD[15]	O	L_DD[15]; LCD data
74	L_FCLK	O	L_FCLK: LCD frame clock
75	L_LCLK	O	L_LCLK; LCD clock
76	L_PCLK	O	L_PCLK; LCD pixel clock
77	L_BIAS	O	LCDCS / L_BIAS; LCD chip select
78	nCS[2]	O	Strobe Intensity
79	nCS[3]	O	CIR On
80	nCS[4]	O	nCS[4] Ethernet; Ethernet chip select
81	BB_OB_DAT[0]	O	BB_OB_DAT[0]; MSL outbound data
82	BB_IB_DAT[0]	I	BB_IB_DAT[0]; MSL outbound data
83	BB_IB_CLK	I	BB_IB_CLK: MSL clock
84	BB_IB_STB	I	BB_IB_STB; MSL strobe
85	BB_IB_WAIT	O	BB_IB_WAIT; MSL wait
86	L_DD[16]	I/O	SSPRXD2; Audio PCM receive
87	L_DD[17]	I/O	SSPTXD2; Audio PCM transmit
88	USBHPWR[0]	I/O	SSPSFRM2; Audio PCM frame
89	USBHPEN[0]	I	SSPRXD3; WLAN receive
90	nURST	I	CIF_DD[4]; Camera data
91	UCLK	I	CIF_DD[5]; Camera data
92	MMDAT[0]	I/O	MMDAT[0]; MMC data
93	KP_DKIN[0]	I	KP_DKIN[0]; Keypad direct IN
94	KP_DKIN[1]	I	KP_DKIN[1]; Keypad direct IN
95	KP_DKIN[2]	I	KP_MKIN[6]; Keypad direct IN
96	KP_DKIN[3]	O	KP_MKOUT[6]; Keypad direct OUT
97	KP_DKIN[4]	I	KP_MKIN[3]; Keypad direct IN

Table 4. Intel® PXA27x Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

GPIO_Pin	Pin_Name	Direction	Description
98	KP_DKIN[5]	O	AC97_SYSCLK; AC97 system clock
99	KP_DKIN[6]	I	KP_MKIN[5]; Keypad matrix IN
100	KP_MKIN[0]	I	KP_MKIN[0]; Keypad matrix IN
101	KP_MKIN[1]	I	KP_MKIN[1]; Keypad matrix IN
102	KP_MKIN[2]	I	KP_MKIN[2]; Keypad matrix IN
103	KP_MKOUT[0]	O	KP_MKOUT[0]; Keypad matrix OUT
104	KP_MKOUT[1]	O	KP_MKOUT[1]; Keypad matrix OUT
105	KP_MKOUT[2]	O	KP_MKOUT[2]; Keypad matrix OUT
106	KP_MKOUT[3]	I	CIF_DD[9]; Camera data
107	KP_MKOUT[4]	I	CIF_DD[8]; Camera data
108	KP_MKOUT[5]	O	KP_MKOUT[5]; Keypad matrix OUT
109	MMDAT[1]	I/O	MMDAT[1]; MMC data
110	MMDAT[2]	I/O	MMDAT[2]; MMC data
111	MMDAT[3]	I/O	MMDAT[3]; MMC data
112	MMCMD	O	MMCMD; MMC command
113	AC97_RESET_n	O	AC97_RESET_n; AC97 reset
114	UVS0	I	CIF_DD[1]; Camera data
115	nUVS1	I	CIF_DD[3]; Camera data
116	nUVS2	I	CIF_DD[2]; Camera data
117	SCL	I	SDIO WP; SDIO write packet
118	SDA	O	Keypad EL Driver
119	USBHPWR[1]	O	IRDA Shutdown
120	USBHPEN[1]	O	Camera Shutdown

3.2.5 Programming Application Flash Memory

This section provides instructions for programming the flash memory in the PXA27x processor.

Programming these devices takes place via the PXA27x processor JTAG interface, using the Intel® JTAG Cable programming kit and a host computer with Windows* 98, Windows* NT, Windows* 2000, or Windows* XP installed as the operating system.

3.2.5.1 Preparing the Hardware

The Intel® JTAG Cable programming kit hardware consists of two cables and an interface module. To install the Intel® JTAG Cable programmer and prepare the Intel® PXA27x Processor Reference Platform for programming, follow these steps:

1. Turn off the Intel® PXA27x Processor Reference Platform power.
2. Plug in the Intel® PXA27x Processor Reference Platform Debug Board.
3. Attach the 25-pin parallel-port cable between the host computer's parallel port and the matching connector on the Intel® JTAG Cable interface device.
4. Attach the 20-pin ribbon cable between the matching connector on the interface card and the JTAG connector (J2) on the Intel® PXA27x Processor Reference Platform Debug Board.

Note: The Intel® JTAG Cable interface device draws a few milliamps of 3.3-volt power from the Intel® PXA27x Processor Reference Platform on pin 1 of the Intel® JTAG Cable connector.

3.2.5.2 Preparing the Host Computer

The flash-memory programming software, JFlashMM, requires that a parallel port device driver be installed on the host computer when using Windows* 98,Windows* NT, Windows* 2000, or Windows* XP. To configure the host with this device driver, follow these steps:

1. Configure the parallel port for ECP mode.
2. Install the JFlashMM software by following the instructions in the JFlashMM release notes.

3.2.6 Flash Memory

To start the flash-memory programmer, follow these steps:

1. Remove power from the platform.
2. Connect a Intel® PXA27x Processor Reference Platform Debug Board to the system by inserting it fully into the SD socket.
3. Apply power to the system and turn on the system.
4. Follow the instruction in JFlash release notes to install JFlashMM.
5. Apply power to the PXA27x processor.
6. On the host computer, execute the file `jflashmm.exe`.

After programming is complete, return the PXA27x processor to normal operation by turning off PXA27x processor power.

Communications Processor and Audio Concept 4

This chapter includes the following sections:

4.1 Communications Processor

4.1.1 Communications Processor Frequency Settings

4.1.1.1 Communications Processor PMU Clock Settings

- Main PLL - 104 MHz
- USB PLL - not used
- Intel Xscale® - 104 MHz
- MSA - 104 MHz
- PX bus - 104 MHz
- APB clock - 26 MHz
- MEMC - not used (no external memory)

4.1.2 Communications Processor Pin Usage

The following table describes the communications processor pin usage for the Intel® PXA27x Processor Reference Platform.

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
GPIO2	DSSP3_FRM	PCM Frame Sync
GPIO32	DSSP3_CLK	PCM CLK
GPIO5	SLEEP	Communications Processor Sleep Indication

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
GPIO6	N/A	N/A
GPIO7	N/A	N/A
GPIO4	N/A	N/A
GPIO43	N/A	N/A
GPIO44	DSSP3_RX	RCM RXD
GPIO8	N/A	N/A
GPIO9	DSSP3_TX	PCM TXD
USB_P	USB_P	Communications Processor USB Client
USB_N	USB_N	Communications Processor USB Client
GPIO45	N/A	N/A
GPIO46	N/A	N/A
GPIO47	N/A	N/A
TCO14	TCO14	RF Control Signal
TCO13	TCO13	RF Control Signal
TCO12	TCO12	RF Control Signal
TCO11	TCO11	RF Control Signal
ABBCLK	ABBCLK	Common DSSP Clock
ABBCLK_EN	ABBCLK_EN	Common DSSP Clock enable
DSSP3_FRM	N/A	N/A
DSSP3_RX	N/A	N/A
DSSP3_TX	N/A	N/A
DSSP4_RX	DSSP4_RX	RF synthesizers control SSP
DSSP4_FRM	DSSP4_FRM	RF synthesizers control SSP
DSSP4_TX	DSSP4_TX	RF synthesizers control SSP
ABB_RESET_N	N/A	N/A
DSSP2_FRM	DSSP2_FRM	RF Data In SSP
DSSP2_RX	DSSP2_RX	RF Data In SSP
DSSP1_FRM	DSSP1_FRM	RF Data Out SSP
DSSP1_TX	DSSP1_TX	RF Data Out SSP
DSSP5_CLK	DSSP5_CLK	N/A
DSSP5_FRM	DSSP5_FRM	N/A
DSSP5_TX_RX	DSSP5_TX_RX	N/A
VCXO_ON	VCXO_ON	DA9030* LDO 14 Enable
GPIO20	TCO10	DA9030* TXON input
GPIO19	TCO9	RF Control Signal - N/A

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
GPIO18	TCO8	RF Control Signal - N/A
GPIO17	TCO7	RF Control Signal - N/A
GPIO16	TCO6	RF Control Signal - N/A
GPIO15	TCO5	RF Control Signal - N/A
GPIO14	TCO4	RF Control Signal - N/A
GPIO13	TCO3	RF Control Signal - N/A
GPIO12	TCO2	RF Control Signal - N/A
GPIO11	TCO1	RF Control Signal - N/A
GPIO10	TCO0	RF Control Signal - N/A
VCXO	VCXO_IN	Main 13M IN
SIM_RST_N	SIM_RST_N	SIM Card reset
SIM_DIO	SIM_DIO	SIM Card data
SIM_CLK	SIM_CLK	SIM Card clock
PMIC_INTR_N	PMIC_INTR_N	DA9030* interrupt input
CP_TCLK	CP_TCLK	Main JTAG
CP_TDI	CP_TDI	Main JTAG
CP_TMS	CP_TMS	Main JTAG
CP_TRST_N	CP_TRST_N	Main JTAG
CP_TDO	CP_TDO	Main JTAG
GPIO34	N/A	N/A
GPIO35	N/A	N/A
GPIO38	N/A	N/A
EXT_ADDR1	N/A	N/A
GPIO24	N/A	N/A
EXT_OE_N	N/A	N/A
EXT_DATA0	N/A	N/A
EXT_DATA8	N/A	N/A
EXT_DATA1	N/A	N/A
EXT_DATA9	N/A	N/A
EXT_DATA2	N/A	N/A
EXT_DATA10	N/A	N/A
EXT_DATA3	N/A	N/A
EXT_DATA11	N/A	N/A
EXT_DATA4	N/A	N/A
EXT_DATA12	N/A	N/A
EXT_DATA5	N/A	N/A

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
EXT_DATA13	N/A	N/A
EXT_DATA6	N/A	N/A
EXT_DATA14	N/A	N/A
EXT_DATA7	N/A	N/A
EXT_DATA15	N/A	N/A
EXT_ADDR17	N/A	N/A
GPIO37	N/A	N/A
GPIO28	MSL_OB_DAT2	MSL Data out 1
GPIO31	N/A	N/A
GPIO36	N/A	N/A
GPIO63	N/A	N/A
GPIO1	N/A	N/A
ALARM	ALARM	DA9030* wake up
RESET_IN_N	RESET_IN_N	Communications Processor Main Reset
OSC_32KHZ_OUT	OSC_32KHZ_OUT	32K crystal
OSC_32KHZ_IN	OSC_32KHZ_IN	32K crystal
KPD_R7	BOOT_SEL	Internal/External Boot select
GPIO62	N/A	N/A
GPIO3	N/A	N/A
EXT_NPWE	N/A	N/A
I2C_SCL	I2C_SDL	I^2C Clock
I2C_SDA	I2C_SDA	I^2C Data
KPD_R0	MSL_IB_STB	MSL Strobe In
KPD_R1	MSL_RESET_N	Communications Processor Secondary Reset
EXT_RDY	N/A	N/A
EXT_ADDR20	N/A	N/A
EXT_ADDR21	N/A	N/A
GPIO25	N/A	N/A
EXT_CS0_N	N/A	N/A
GPIO23	N/A	N/A
GPIO60	N/A	N/A
KPD_R2	MSL_IB_DAT0	MSL Data In 0
KPD_R3	MSL_CLK_REQ	13M clock request
KPD_R4	MSL_OB_DAT0	MSL Data out 0
KPD_R5	MSL_OB_STB	MSL Strobe Out

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
GPIO30	MSL_OB_DAT3	MSL Data out 3
EXT_SDCLK0	N/A	N/A
KPD_C0	MSL_IB_DAT2	MSL Data In 2
KPD_C1	MSL_OB_DAT1	MSL Data Out 1
KPD_C2	MSL_IB_DAT1	MSL Data In 1
KPD_C3	MSL_OB_CLK	MSL Clock Out
KPD_C4	MSL_IB_CLK	MSL Clock In
KPD_C5	MSL_13MCLK_OUT	13M out for PXA27x Processor
GPIO29	MSL_IB_DAT3	MSL Data In 3
GPIO21	N/A	N/A
GPIO22	N/A	N/A
GPIO50	MSL_IB_WAIT	MSL Wait In
GPIO51	MSL_OB_WAIT	MSL Wait Out
GPIO39	N/A	N/A
GPIO40	N/A	N/A
GPIO41	N/A	N/A
GPIO42	N/A	N/A
GPIO52	HSL_DATA0	HSL (DSP logger) port
GPIO53	HSL_DATA1	Communications Processor UART_DTR
GPIO55	HSL_DATA2	Communications Processor IRQ from PXA27x Processor
GPIO27	HSL_DATA3	PXA27x processor IRQ from Communications Processor
GPIO56	HSL_DATA4	Communications Processor UART_CTS
GPIO57	HSL_CLK	Communications Processor UART_RTS
GPIO54	UART1_RX	AT Command Port
GPIO33	UART1_TX	AT Command Port
GPIO26	MUX_CLK0	32K out for PXA27x Processor
MN_CLK_OUT0	MN_CLK_OUT0	M/N clock (2.048M)
EXT_ADDR16	N/A	N/A
EXT_ADDR15	N/A	N/A
EXT_ADDR14	N/A	N/A
EXT_ADDR13	N/A	N/A
EXT_ADDR12	N/A	N/A
EXT_ADDR11	N/A	N/A

Table 5. Communications Processor Pin Usage for the Intel® PXA27x Processor Reference Platform

Pin Name	Intel® PXA27x Processor Reference Platform Usage	Description
EXT_ADDR10	N/A	N/A
EXT_ADDR9	N/A	N/A
EXT_WE_N	N/A	N/A
EXT_DQM1	N/A	N/A
EXT_DQM0	N/A	N/A
EXT_ADDR19	N/A	N/A
EXT_ADDR18	N/A	N/A
EXT_ADDR8	N/A	N/A
EXT_ADDR7	N/A	N/A
EXT_ADDR6	N/A	N/A
EXT_ADDR5	N/A	N/A
EXT_ADDR4	N/A	N/A
EXT_ADDR3	N/A	N/A
EXT_ADDR2	N/A	N/A

4.2 Intel® PXA27x Processor Reference Platform GSM Radio

The GSM radio portion of the Intel® PXA27x Processor Reference Platform is based on the RFMD chipset named POLARIS II. It supports GSM, GPRS, and forms the foundation for EGPRS operations, as well.

The radio is operated in GSM850, GSM900, DCS (1800), and PCS (1900) bands. It includes all of the circuitry from antenna to baseband.

The receiver uses Zero-IF (ZIF) direct conversion (DCR) architecture, in which the received signal is converted directly to baseband, eliminating the need for IF SAW filters. The transmitter implements a direct digital modulation technique that eliminates the need for a separate modulator or translation loop.

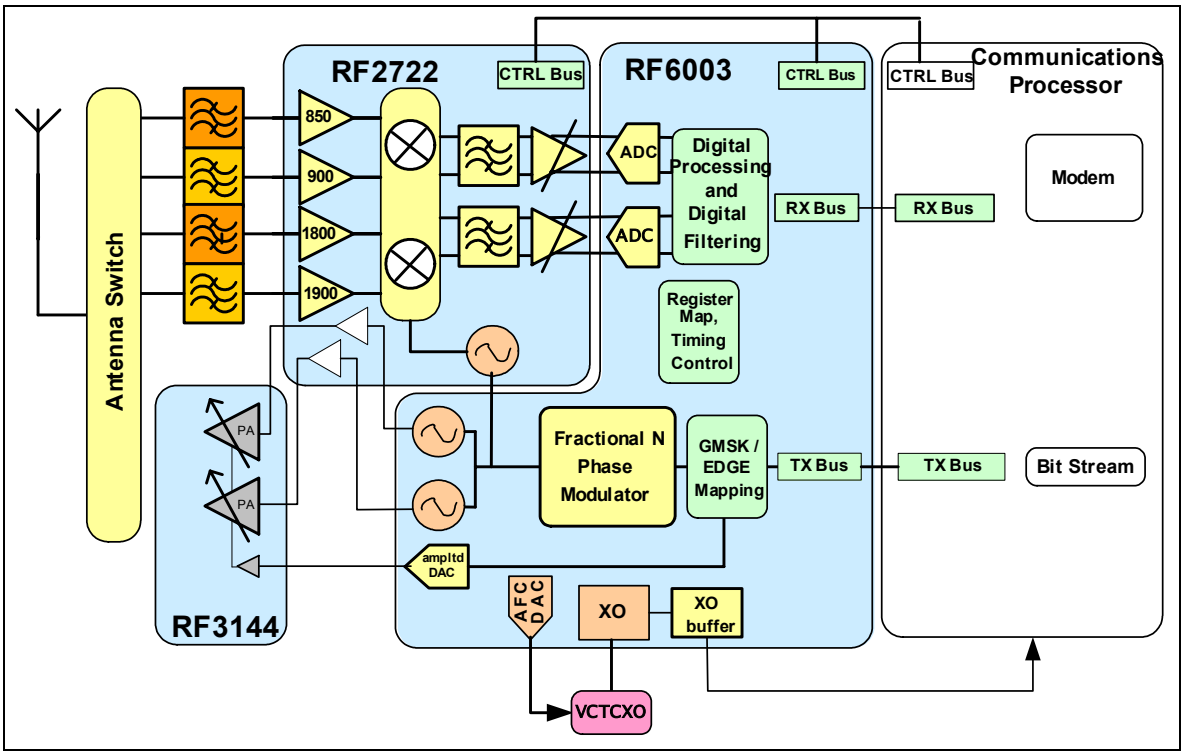
Adapting a radio solution, which is based on POLARIS II chipset, has the advantage of allowing easy transition to EGPRS operation.

The Intel® PXA27x Processor Reference Platform radio design allows use of the POLARIS solution. The POLARIS solution supports GSM, and GPRS standards.

4.2.1 Radio Description

The RF portion block diagram is described in Figure 4.

Figure 4. RF Block Diagram



There are two main subsystems - the POLARIS chipset and the RF front end.

The POLARIS II chipset consists of an RF2722 receiver, an RF6003 digital filter which includes an RX digital filer, a TX modulator, and a synthesizer; and an RF3144 power amplifier. The VCOs are integrated into the chipset.

The POLARIS II chipset has the capability to use either a TCXO or a crystal resonator for its reference oscillator.

The RF front end is currently based on EPCOS components. It consists of an antenna switch and four separated RX SAW filters (one for each band). The antenna switch includes band-select switch and TX harmonic reject filters.

The POLARIS II solution consists of the following main elements:

Table 6. Polaris II Main Components

Function	Part Number	Vendor
Receiver	RF2722	RFMD
Synt, modulator, digital BB filters.	RF6003	RFMD
Power Amplifier	RF3144	RFMD
TCXO / XTAL	END3562A	NDK
RF switch	A010	EPCOS
GSM850 Rx SAW filter	B9001	EPCOS

Table 6. Polaris II Main Components

GSM900 Rx SAW filter	B7820	EPCOS
DCS Rx SAW filter	B7821	EPCOS
PCS Rx SAW filter	B7825	EPCOS

The POLARIS solution can be implemented in place of the POLARIS II (using the same printed circuit board), by replacing RF6001 with RF6003 and replacing RF3140 with RF3144.

4.2.1.1 Receive Path

The receiver (RF2722) incorporates four LNAs to allow quad-band operation capability.

The received signal is applied to the appropriate LNA through the correct RX SAW filter according to the desired band. The LNAs share a common mixer.

The received signal is converted directly to baseband signal, at zero IF, and then amplified and filtered. The outcome is provided through the I and Q differential outputs for further processing.

The signals are sampled and digitally filtered in the RF6003 IC. The filtered samples are then provided to the baseband portion.

4.2.1.2 Transmit Path

The transmit data bits are provided through the transmit serial bus to RF6003 IC. The RF6003 IC contains transmit VCOs for low and high bands. The modulated signal is buffered to the RF3144 power amplifier, where it is amplified and then applied to the antenna.

4.2.2 Antenna

The quad-band antenna is part of the radio portion.

4.2.3 Radio Interface Requirements

The POLARIS II interface requirements are defined in the *Physical Layer Interface for RF Module Based on POLARIS II* document.

The following information is included:

- Power requirements
- Frequency plan
- Operational modes description
- Radio control instructions (register mapping, sequences, and timing)

4.3 Communications Processor Boot Loader Application

The Boot Loader application enables the downloading of software and data to the internal, external, or MSA flash memory of the communications processor on the Intel® PXA27x Processor Reference Platform board.

The Boot Loader application is activated via the ICAT application. For additional information on the ICAT application, refer to *Diagnostics for the* Intel® PXA27x Processor Reference Platform *User's Guide*.

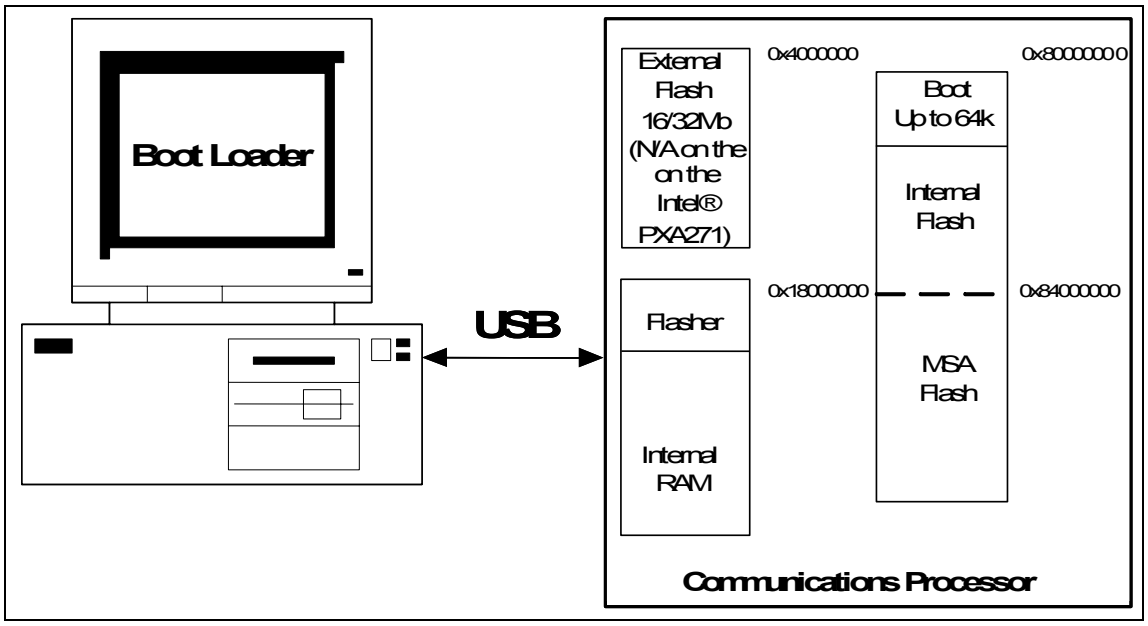
The Boot Loader connects with the communications processor board via a USB communication connection on the Intel® PXA27x Processor Reference Platform Debug Board. For additional information on the Intel® PXA27x Processor Reference Platform Debug Board, refer to *Diagnostics for the* Intel® PXA27x Processor Reference Platform *User's Guide*.

The USB connection requires the following drivers:

- Intel Boot Loader Device Driver
- Intel Flasher Device Driver

Figure 5 provides a system overview of the Boot Loader application.

Figure 5. Boot Loader System Overview



4.3.1 Activating the Boot Loader

To activate the ICAT Boot Loader for the first time, perform the following steps:

1. Choose "Select Modules" from the Workspace menu on the top menu bar and click the "Select Module" command. The Select Module dialog box is displayed.

2. Select the Boot Loader module and click “Add” to confirm the selection.
3. Click “OK” to activate the Boot Loader module. The Boot Loader menu is displayed on the top menu bar.

Once the boot loader module is activated (ICAT default state), just select Utilities>Boot Loader>Run Boot Loader to display the Boot Loader main window.

4.3.2 Connecting the Boot Loader

To connect the communications processor to the ICAT Boot Loader, perform the following steps:

1. Activate the ICAT Boot Loader, as described in Section 4.3.1.
2. Install the Boot program by burning "bootloader.bin" file to Address 0x0 of the communications processor using the Intel® XDB JTAG debuggers.
3. Connect the USB cable between the ICAT workstation and the communications processor (USB connector on the Intel® PXA27x Processor Reference Platform Debug Board).
4. Put the communications processor in boot loader mode (boot pin = "HIGH", 1.8V).
5. Power up the Intel® PXA27x Processor Reference Platform board; a communication "handshake" is performed automatically and the following message is displayed in the status bar at the bottom of the BootLoader menu: "Boot process version X . X is running on the Target".

4.3.3 Transfer Files into the Communications Processor

4.3.3.1 Download the Flasher Application

To transfer the Flasher application from the ICAT workstation to the communications processor board, perform the following steps:

1. Activate the ICAT Boot Loader, as described in Section 4.3.1.
2. Connect the communications processor as described in Section 4.3.2.
3. Select “Set Path” from the Flasher drop down menu on the Boot Loader menu bar. The Boot Properties dialog box is displayed.
4. Enter a valid path name in the field labeled “Flasher Path” and click “OK” to confirm the selection; the path name should specify the location of the "Flasher.elf" file.
5. Select “Burn” from the Flasher drop down menu to activate the Flasher application and transfer files to the target board.

4.3.3.1.1 Security Mode

If the Boot Loader is running in security mode, the Password Authentication dialog box is displayed before downloading starts. In this case, the user needs to set the path of the authentication file, including an authentication number provided by the supplier (plain text and encrypted text).

1. Enter the path of the authentication number file and click “OK” to continue. If the authentication file or number is incorrect, an error message is displayed and the download process terminates.

2. Click “OK” when the Process Complete message box is displayed. A communication restart operation is performed. This operation terminates the Boot USB driver and activates the Flasher USB driver. If automatic mode is enabled, then the Process Complete message box is not displayed.
3. The Flasher driver is recognized by the PC workstation and the following message is displayed: "Flasher process is running on the Target". When this message is displayed, the user can download the embedded application to the target.

4.3.3.2 Download and Run Application Files

To transfer embedded application files from the ICAT workstation to the communications processor, perform the following steps:

1. Select “Add” from the Edit drop down menu to display the Add File dialog box.
2. Select the location of the XScale bin file to burn in the field labelled Filename.
3. Set the start address for the XScale "*.bin" file to 0x80010000 in the field labelled "Start Address".
4. Select the location of the DSP bin file to burn in the field labelled “Filename”.
5. Set the start address for the DSP "*.bin" file to 0x84000000 in the field labeled "Start Address".
6. Verify that the Xscale file is the first one in the list menu, use the Up/Down buttons on the menu to change the file order.
7. Select “Burn” from the Flasher menu to begin the file transfer process.
8. Once the download process is complete, “Passed” is displayed in the Status column of the BootLoader menu and the Flasher process status dialog box indicates “Process complete!”.

Note: The ICAT Boot Loader performs an automatic verification test for each file. To perform a manual verification test, highlight the appropriate file(s) and select “Verify” or “Verify All” from the Flasher menu.

To run the application on the target board, perform the following steps:

1. Close the Boot Loader application from the ICAT workstation.
2. Set the communications processor boot mode to "normal" (boot pin = "LOW").
3. Cycle the power to run the communications processor code you just burned.

4.3.4 Load\Save File List

To save an existing file list, perform the following steps:

1. Activate the ICAT Boot Loader, as described in Section 4.3.1.
2. Create a file list to download, as described in Steps 1 through 6 in Section 4.3.3.2.
3. Select File>Save File List As and enter a filename in the field labeled Filename. Click “OK” to verify the save operation.

Note: Boot Loader file lists are automatically designated with a .blf file extension.

To load an existing file list, perform the following steps:

1. Activate the ICAT Boot Loader, as described in Section 4.3.1.
2. Select File>Open File and enter a filename in the field labeled Filename. Click “OK” to confirm load operation. The selected file list is displayed in the Boot Loader application window.

4.4 Audio Concept

The purpose of this section is:

- To define the Intel® PXA27x Processor Reference Platform audio concept from a system perspective and describe the connectivity between the different audio elements (processors, codec, Bluetooth*, Accessories, etc.).
- To describe the audio flow for a major set of audio scenarios

The Intel® PXA27x Processor Reference Platform, as a two-chip configuration system, inherits the communications processor audio concept.

The communications processor audio concept utilizes a dual codec architecture. This concept is based on one single shared codec resource that is connected to both the PXA27x processor and the communications processor.

The WM9713 codec, which is a single-chip AC97+PCM codec, was specified together with Wolfson for use in the Intel® PXA27x Processor Reference Platform configuration.

The PCM side of that codec is connected to a:

- Communication processor - for normal voice call purposes
- Bluetooth* PCM I/F - for voice applications using Bluetooth* (VMP, answering machine, etc.)

The hardware switching between those connections is done by means of muting and/or tri-stating the relevant ports while enabling the desired ports. The switching is executed by the audio management software layer. This multiple connectivity architecture enables the use of all voice applications required by the applications side without the need to wake up the communications side at all. Both required MSL throughput and the system power consumption are reduced.

The AC97 port of the 9713 codec is connected only to the application side for the purpose of MP3 playback, user notifications, MMI tones play, Touch screen data, etc.

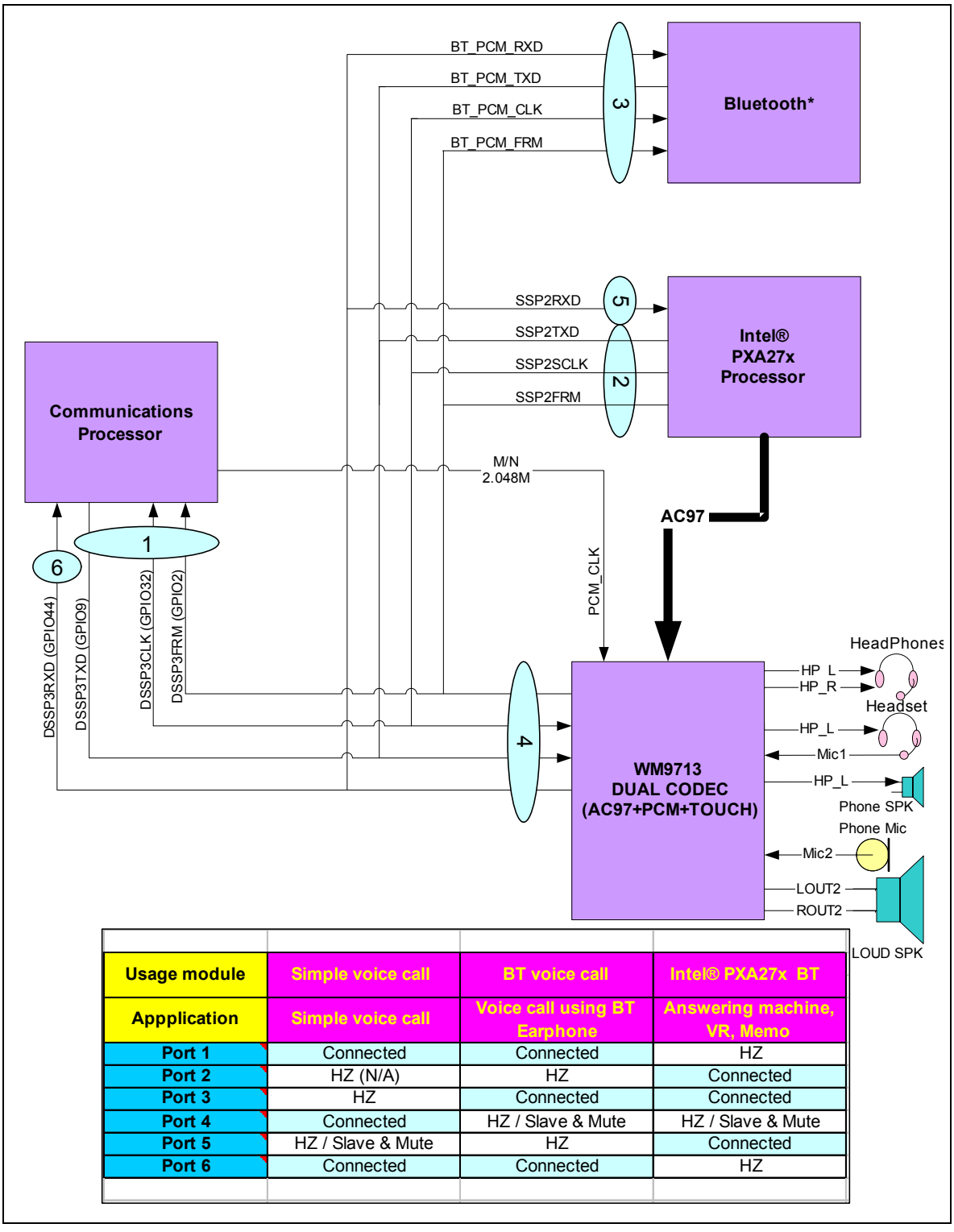
This codec also has some internal mixing capabilities that will enable the support for all required operating system features, such as MP3 as a background to voice call, MP3 play to far end, etc.

The control over that codec is done from the applications side only via AC97.

The figure below shows a basic block diagram of the audio concept using a dual codec (PCM+AC97).

The table attached to it describes the modes of each port in the main audio usage models.

Figure 6. Dual Codec Audio Concept and Hardware Connectivity



Usage module	Simple voice call	BT voice call	Intel® PXA27x BT
Appplication	Simple voice call	Voice call using BT Earphone	Answering machine, VR, Memo
Port 1	Connected	Connected	HZ
Port 2	HZ (N/A)	HZ	Connected
Port 3	HZ	Connected	Connected
Port 4	Connected	HZ / Slave & Mute	HZ / Slave & Mute
Port 5	HZ / Slave & Mute	HZ	Connected
Port 6	Connected	Connected	HZ

4.5 Audio Scenarios

This section describes the audio flow across the Intel® PXA27x Processor Reference Platform system (shown above).

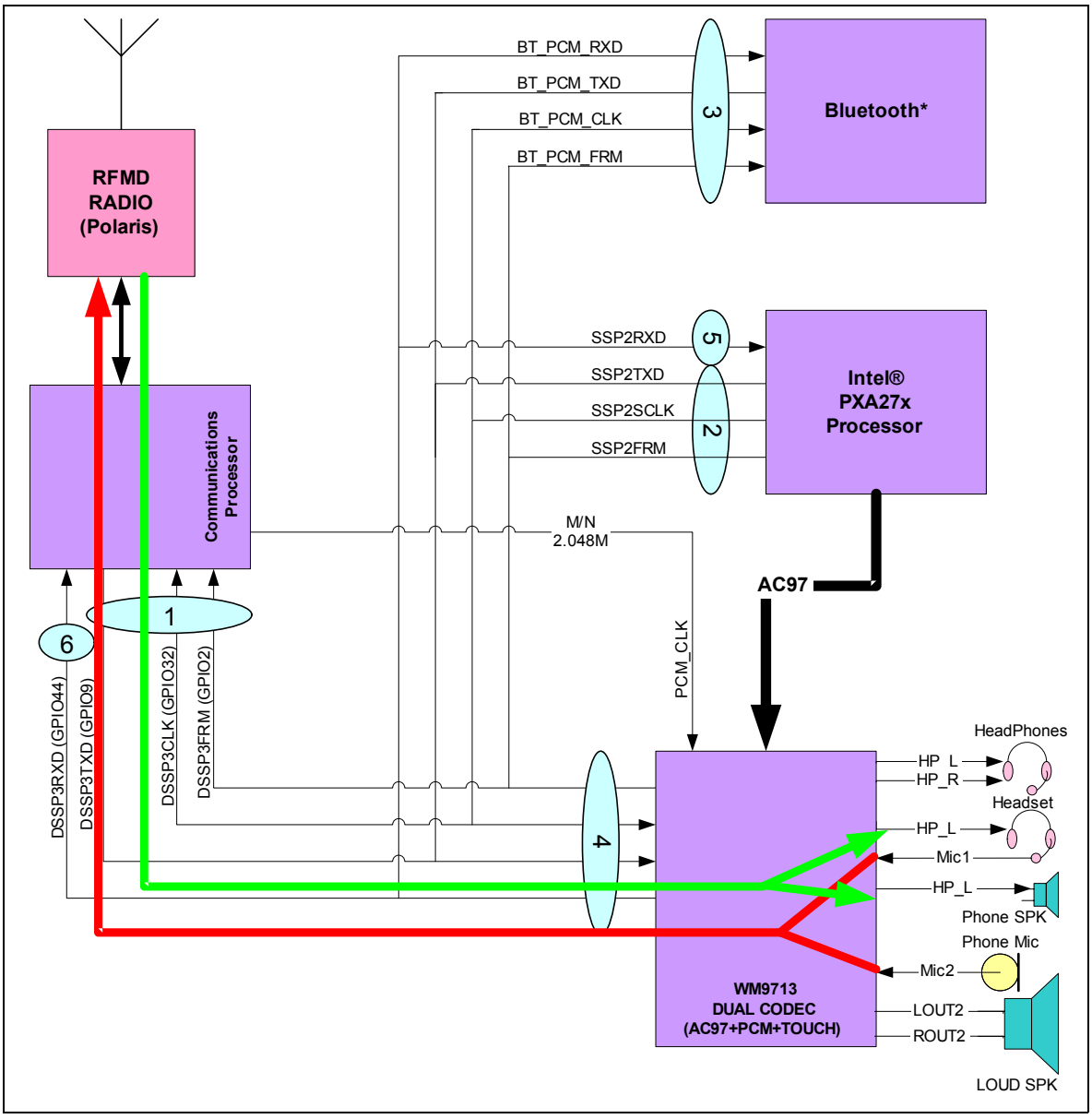
The following audio scenarios are described in this section:

- Normal voice call
- Voice call with Bluetooth* earphone
- Endless recording from microphone (to application file system)
- Normal voice call + MP3 play to near end
- Normal voice call + MP3 play to both near end and far end
- Recording of voice call.

Note: All audio scenarios listed below are controlled by the PXA27x Processor via the AC97 link.

4.5.1 Basic Voice Call

Figure 7. Basic Voice Call



4.5.1.1 Description

Audio RX path description (Green):

BS => RF => Communications Processor DSSP3 => Codec PCM I/F => Codec Speaker or headset.

Audio TX path description (Red):

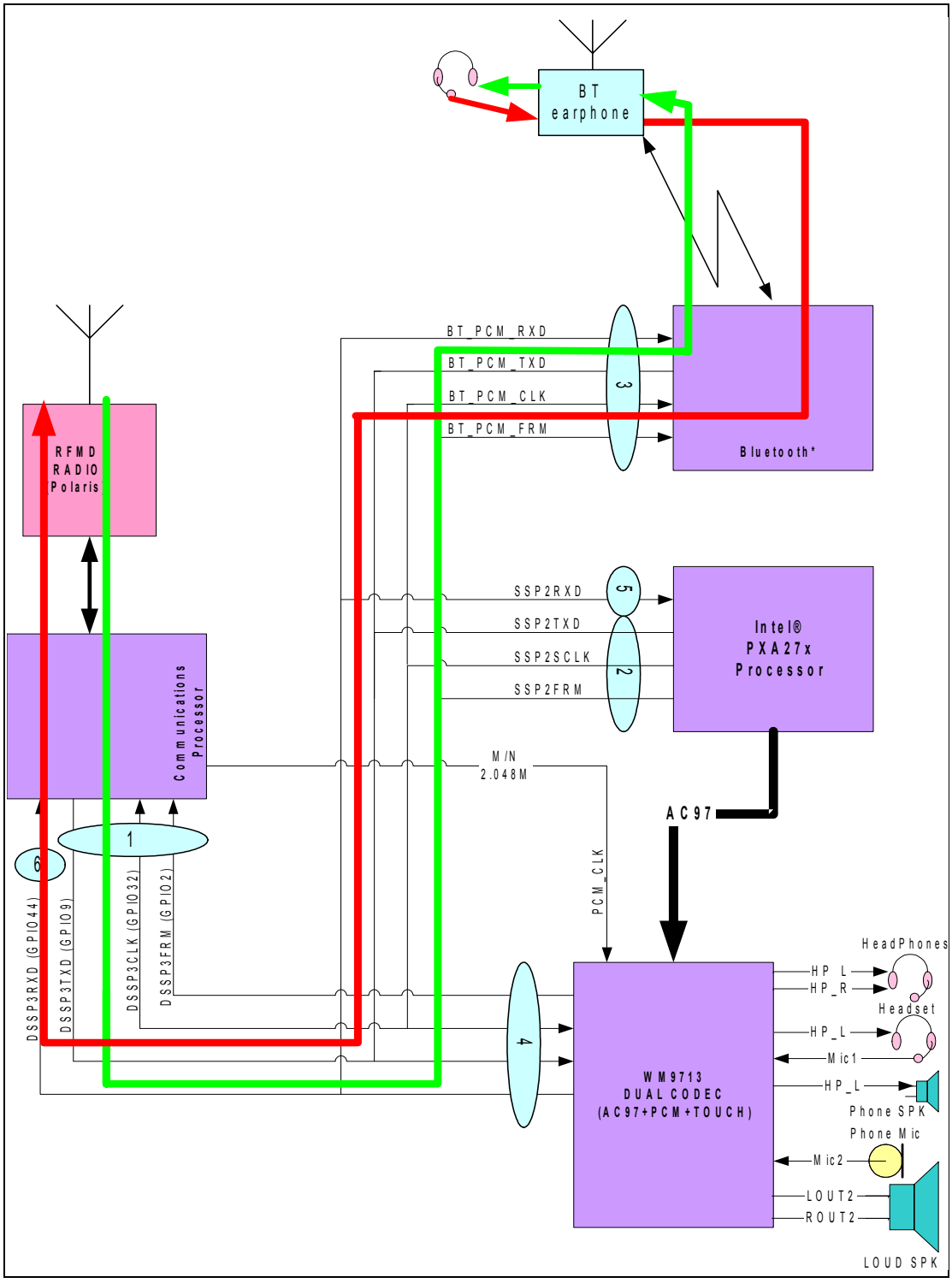
Phone internal/external Mic => Codec PCM I/F => Communications Processor DSSP3 => RF => BS.

4.5.1.2 Ports State

- Ports enabled - 1, 4, and 6.
- Ports High Z - 2, 3, and 5.

4.5.2 Voice Call with Bluetooth* Earphone

Figure 8. Voice Call with Bluetooth*



4.5.2.1 Description

Audio RX path description (Green):

BS => RF => Communications Processor DSSP3 => Bluetooth* PCM I/F => Bluetooth* Air link => Bluetooth* earphone.

Audio TX path description (Red):

Bluetooth* Microphone => Bluetooth* Air link => Bluetooth* PCM I/F => Communications Processor DSSP3 => RF => BS.

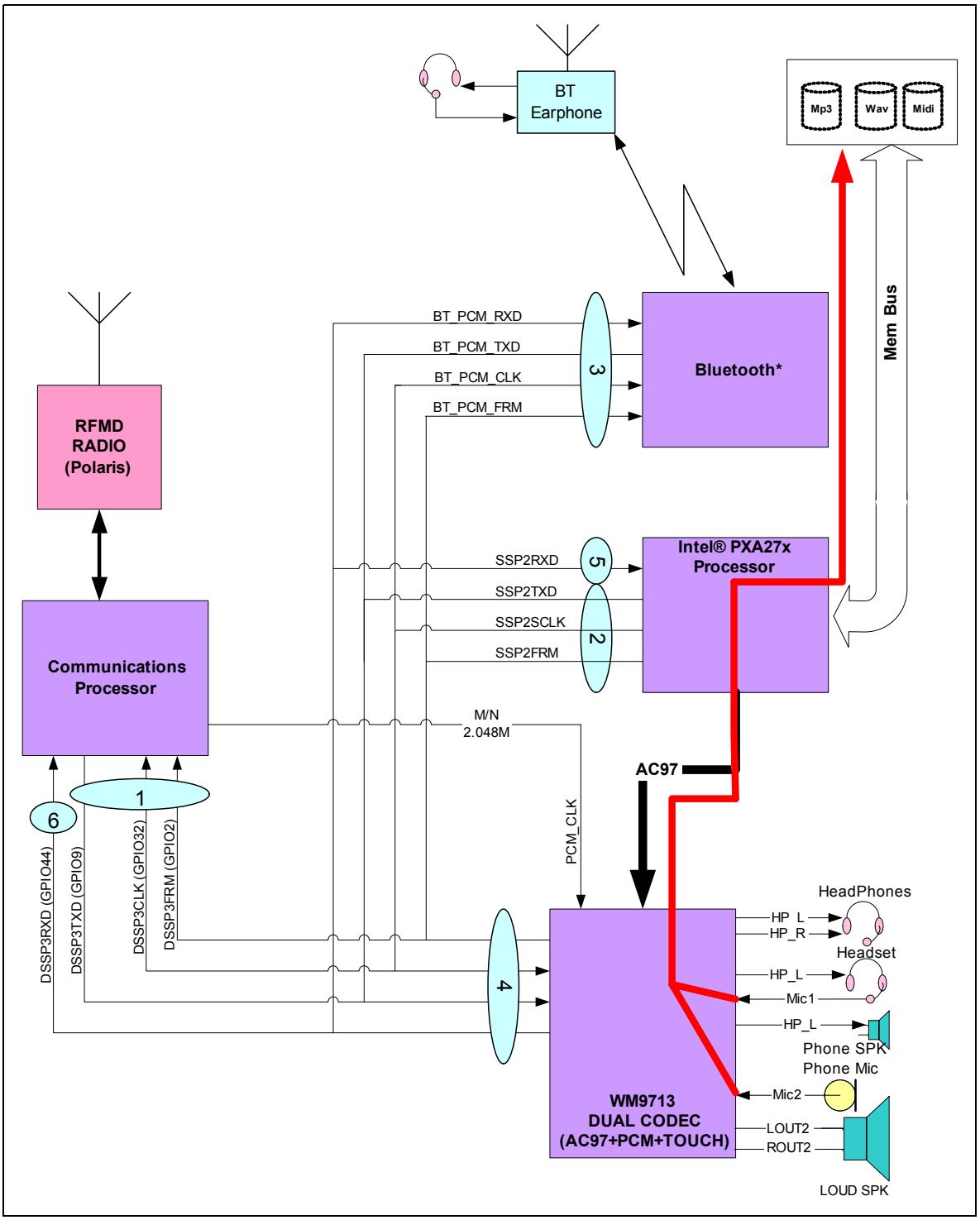
4.5.2.2 Ports State

Ports enabled - 1, 3, and 6.

- Ports High Z - 2, 4, and 5.

4.5.3 Endless Recording

Figure 9. Endless Recording



4.5.3.1 Description

This scenario is valid also for SIVR mode.

Audio RX path description (Green): N/A

Audio TX path description (Red):

Phone internal/external Mic => Codec PCM I/F => PXA27x Processor AC97 => PXA27x Processor file system.

Note the following:

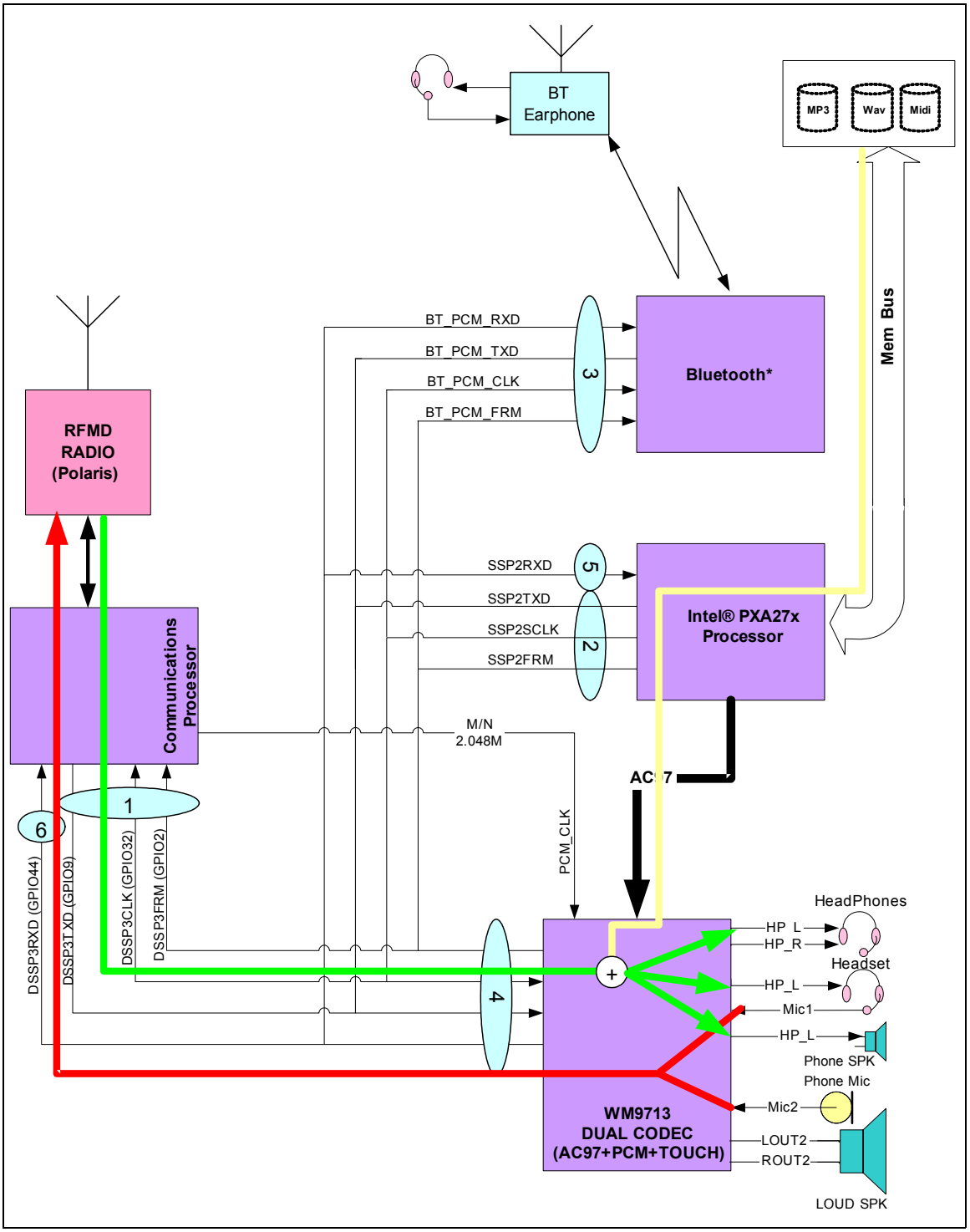
1. The communication side can be totally in sleep at this time.
2. The codec supports the redirection of the microphone to AC97 so the Codec PCM I/F shouldn't be used and can be powered down at this scenario.

4.5.3.2 Ports State

N/A

4.5.4 Voice Call with MP3 Play to Near End

Figure 10. MP3 Playback to Near End During a Call



4.5.4.1 Description

This scenario is also for rendering MMI tones to user near end during a call.

Audio RX path description (Green): See Section 4.5.1.1.

Audio TX path description (Red): See Section 4.5.1.1.

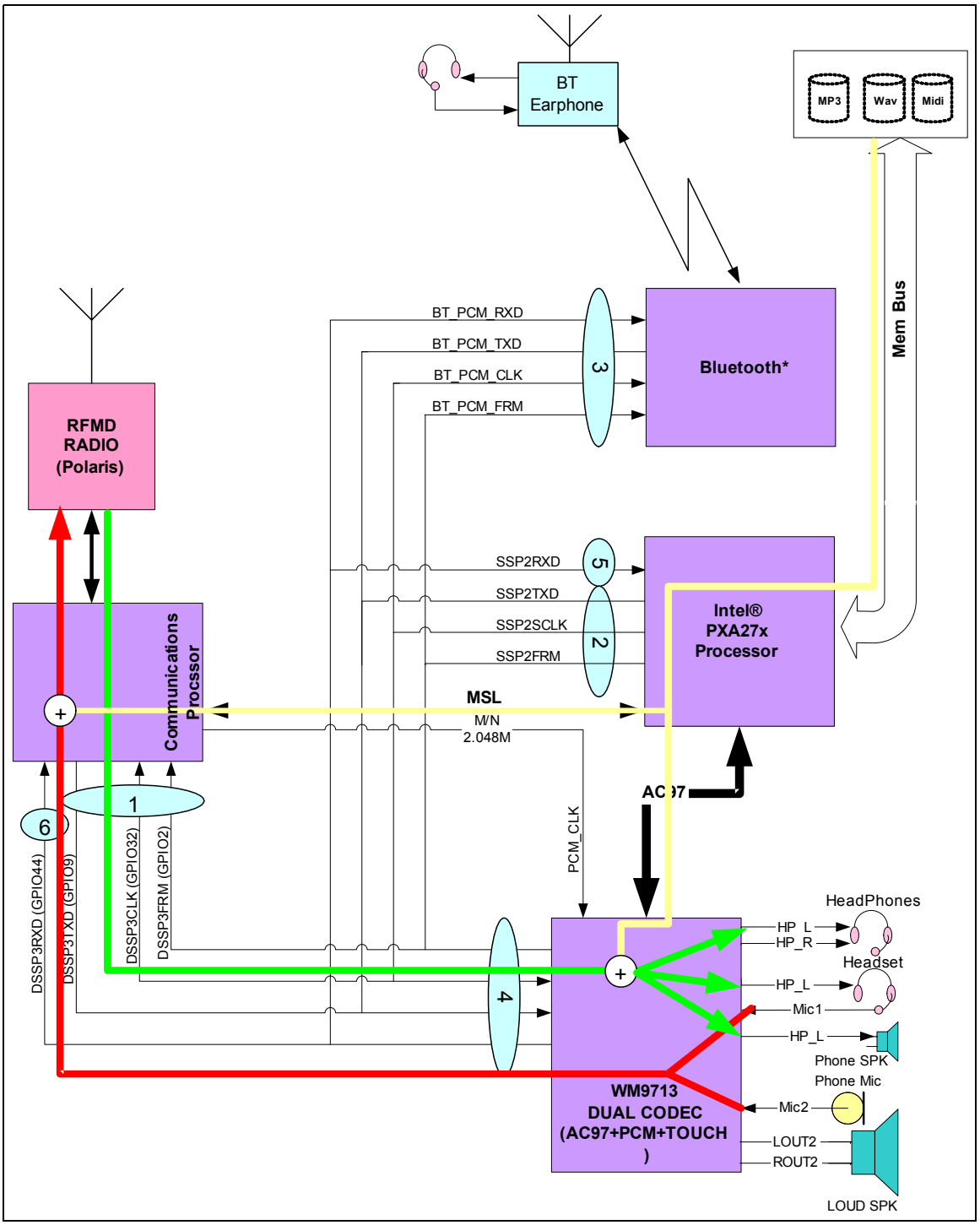
The MP3 analogically mixed with the voice (coming from the communications processor) inside the codec.

4.5.4.2 Ports State

See Section 4.5.1.1.

4.5.5 Voice Call with MP3 Play to Near and Far End

Figure 11. Voice Call with MP3 Play to Near and Far Ends



4.5.5.1 Description

This scenario is also for rendering MMI tones to user near end and far end during a call.

Audio RX path description (Green): See Section 4.5.1.1.

Audio TX path description (Red): See Section 4.5.1.1.

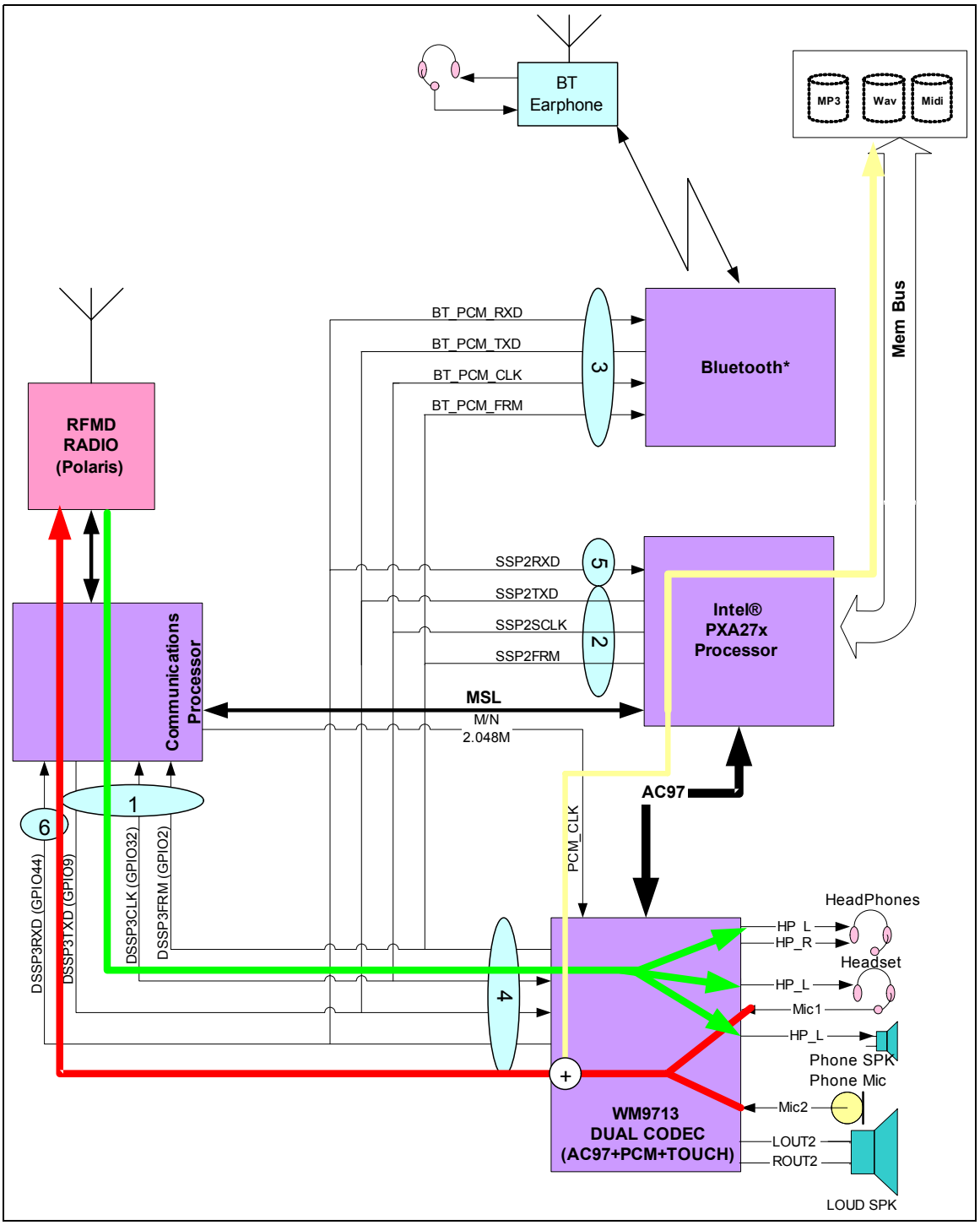
The MP3/wave to near end is analogically mixed with the voice (coming from the communications processor) inside the codec. The MP3/wave to far end is streamed over the MSL and mixed digitally before transmitted via RF I/F.

4.5.5.2 Ports State

See Section 4.5.1.1.

4.5.6 Recording Near End Notes During Voice Call

Figure 12. Recording Near End Notes During Voice Call



4.5.6.1 Description

Audio RX path description (Green): See Section 4.5.1.1.

Audio TX path description (Red): See Section 4.5.1.1.

The user notes are streamed inside the codec to the AC97/I2S I/F and saved into the PXA27x Processor file system.

4.5.6.2 Ports State

See Section 4.5.1.1 (same as voice call).

Intel® PXA27x Processor Reference Platform System Power Management 5

This chapter defines the power management for the Intel® PXA27x Processor Reference Platform:

- DA9030* Definition
- Clock Tree
- System Reset
- Two-Chip System Power Management using MSL
- Power Consumption Approximations

5.1 DA9030* Definition

The Intel® PXA27x Processor Reference Platform is powered mainly from the Dialog Semiconductor DA9030* with the following features.

- Integrated, single-chip solution for battery charge control and power supply management
- Twenty-one programmable low-dropout linear voltage regulators with over 65-dB power supply rejection ratio (PSRR) from 10 Hz to 10 kHz
- High efficiency DC-to-DC converter (Buck), with programmable output voltage
- High efficiency DC-to-DC converter (Buck), with programmable output voltage and DVC
- One step up low current charge pump DC-to-DC converter with external capacitors
- System over-voltage and under-voltage shutdown
- Power on/off and reset control logic
- Five individually selectable LED drivers with PWM control
- Boost converter for two parallel strings of up to four white LEDs each
- Vibrator driver with Pulse Width Modulation (PWM) control
- Internal 8-bit analog-to-digital converter with auxiliary inputs. An automatic mode of operation allows monitoring of charger operation.
- Eight Ohm 500 mW speaker driver with volume control
- Linear- or pulse-mode charger for single-cell Li-Ion or Li-Polymer packs
- Integrated control over pre-charge, constant-current, and constant-voltage charging phases. Pulse-mode charging with programmable on/off time.
- Programmable charging current and voltage
- Programmable charge termination by time
- Battery temperature sensing
- Battery pack wake-up

- Serial 400 KHz I^2C compatible interface to transfer the control data between the DA9030* and the host controller (with 2 I^2C addresses)
- Internal current controlled oscillator (hereafter CCO) generates the internal high clock frequency
- Interrupt signal (hereafter IRQ) that generates the interrupt request for the host controller
- Super capacitor back-up charger
- Enhanced Electrostatic Discharge (ESD) protection on all pins that connect to the main battery pack
- USB On-The-Go (OTG) charge pump with session detection
- USB detection via EXTON pin enables automatic start-up including linear charging at 100 mA

5.1.1 DA9030* Connectivity to the Intel® PXA27x Processor Reference Platform

5.1.1.1 Domains Allocation

The following table shows the allocation of the DA9030* power domains across the Intel® PXA27x Processor Reference Platform.

Table 7. Intel® PXA27x Processor Reference Platform <=> DA9030* Domains Allocation

Section	Domains	Voltage	Min	Max	DA9030* Domain	Capacity	Default
Communications Processor	VCC_CORE	1.2V	1.08	1.32	DC/DC1	600mA	1.2V
Intel® PXA27x Processor	VCC_CORE	1.3V	0.765	1.43	DC/DC2	600mA	1.3V
Communications Processor	VCC_PLL	1.2V	1.08	1.5	LDO1	50mA	1.2V
Communications Processor	VCCP_18V 1&2	1.8V	1.62	1.92	LDO2	100mA	1.8V
Communications Processor	VCCH	1.8V	1.7	1.9	LDO2	100mA	1.8V
Communications Processor	VPP	1.8V	0.9	1.9	LDO2	100mA	1.8V
Communications Processor	VCC_ABB	2.8V	1.53	3.3	LDO3	150mA	2.8V
Communications Processor	VCCP_RF	2.8V	1.53	3.3	LDO3	150mA	2.8V
Communications Processor	VCCP3V	2.8V			LDO3	150mA	2.8V

Table 7. Intel® PXA27x Processor Reference Platform <=> DA9030* Domains Allocation

Section	Domains	Voltage	Min	Max	DA9030* Domain	Capacity	Default
Polaris	Digital	2.8V			LDO3	150mA	2.8V
Intel® PXA27x Processor	VCC_MEM	2.5V/1.8V	1.71	3.63	LDO4	100mA	1.8V
Intel® PXA27x Processor	VCC_SDRAM	2.5V/1.8V	1.6	2.7	LDO4	100mA	2.8V
HiFi Codec	ADD	2.6V	1.8	3.6	LDO5	100mA	2.5V
PCM Codec	ADD	2.6V	1.8	3.6	LDO5	100mA	2.5V
Camera	AVDD	2.6V	2.4	2.6	LDO5	100mA	2.5V
Communications Processor	VCCP_SIM	1.8V/3.0V	1.8	3	LDO6	30mA	1.8V
SIM	VCC	1.8V/3.0V	1.8	3	LDO6	30mA	1.8V
Polaris	RX/TX	2.8V			LDO7	80mA	2.8V
Polaris	VCO	2.8V			LDO8	80mA	2.8V
Bluetooth*	VCCRF	2.9V	2.65	3.4	LDO9	100mA	2.8V
Bluetooth*	VDDIOV	2.9V	1.65	3.4	LDO9	100mA	2.8V
802.11 BB	VDDD	1.8V	1.75	1.85	LDO10	200mA	2.8V
802.11 BB	VDDA3	1.8V	1.65	1.95	LDO10	200mA	2.8V
802.11 BB	VDD33	2.9V	2.7	3.6	LDO11	200mA	2.8V
802.11 BB	VDD33_RF	2.9V	2.7	3.6	LDO11	200mA	2.8V
802.11 BB	DCDC_VDD33	2.9V	2.7	3.6	LDO11	200mA	2.8V
802.11 BB	VDDA1/2	2.9V	2.7	3.6	LDO11	200mA	2.8V
Intel® PXA27x Processor	VCC_IO	2.9V	2.7	3.63	LDO12	200mA	2.8V
Intel® PXA27x Processor	VCC_USIM	2.9V	1.8	3	LDO12	200mA	2.8V
Intel® PXA27x Processor	VCC_USB	2.9V	2.7	3.63	LDO12	200mA	2.8V
Intel® PXA27x Processor	VCC_LCD	2.9V	1.71	3.63	LDO12	200mA	2.8V
HiFi Codec	DBVDD	2.9V	1.42	3.6	LDO12	200mA	2.8V
HiFi Codec	TPVDD	2.9V	1.8	3.6	LDO12	200mA	2.8V
PCM Codec	DBVDD	2.9V	1.42	3.6	LDO12	200mA	2.8V
Camera	DOVDD	2.9V	2.5	3.1	LDO12	200mA	2.8V
IrDA	VCC	2.9V	2.7	3.6	LDO12	200mA	2.8V

Table 7. Intel® PXA27x Processor Reference Platform <=> DA9030* Domains Allocation

Section	Domains	Voltage	Min	Max	DA9030* Domain	Capacity	Default
LCD	VDD	2.9V	2.9	3.1	LDO12	200mA	2.8V
Headset Mic (not used)					LDO13	2mA	2.1V
Polaris	VCTCXO	2.8V			LDO14	15mA	2.75V
Intel® PXA27x Processor	VCC_PLL	1.3V	1.17	1.43	LDO15	25mA	1.3V
Intel® PXA27x Processor	VCC_SRAM	1.1V	0.99	1.21	LDO16	40mA	1.1V
802.11 RF	DVDD	2.9V	2.85	3.6	LDO17	30mA	1.8V
802.11 RF	VCCPA	2.9V	2.85	3.6	LDO17	30mA	1.8V
SDIO	VDD	3.1V	3.1	3.5	LDO18	100mA	2.8V
Intel® PXA27x Processor	F_VCC	1.8V	1.7	2	LDO19	100mA	1.8V
Intel® PXA27x Processor	VCC_BB	1.8V	1.71	3.63	LDO19	100mA	1.8V
Camera	DVDD	1.8V	1.62	1.98	LDO19	100mA	1.8V
HiFi Codec	DCVDD	1.8V	1.42	3.6	LDO19	100mA	1.8V
PCM Codec	DCVDD	1.8V	1.42	3.6	LDO19	100mA	1.8V
Intel® PXA27x Processor	VCC_BATT	2.9V	2.25	3.75	RTC		2.65V
Communications Processor	VCC_RTC	2.9V	2	3.6	RTC		2.65V
USB Battery Charger					USB Battery charger		
DA9030*					Battery		
IrDA TX LED					Battery		
LCD Backlight					Battery		
Keypad Backlight					Battery		
Silent Alert Motor					Battery		
Polaris PA					Battery		
802.11 RF	AVDD	2.9V	2.85	3.6	External LDO	300mA	2.8V

5.1.1.2 USB OTG Connectivity

The DA9030* drives the following USB OTG signals.

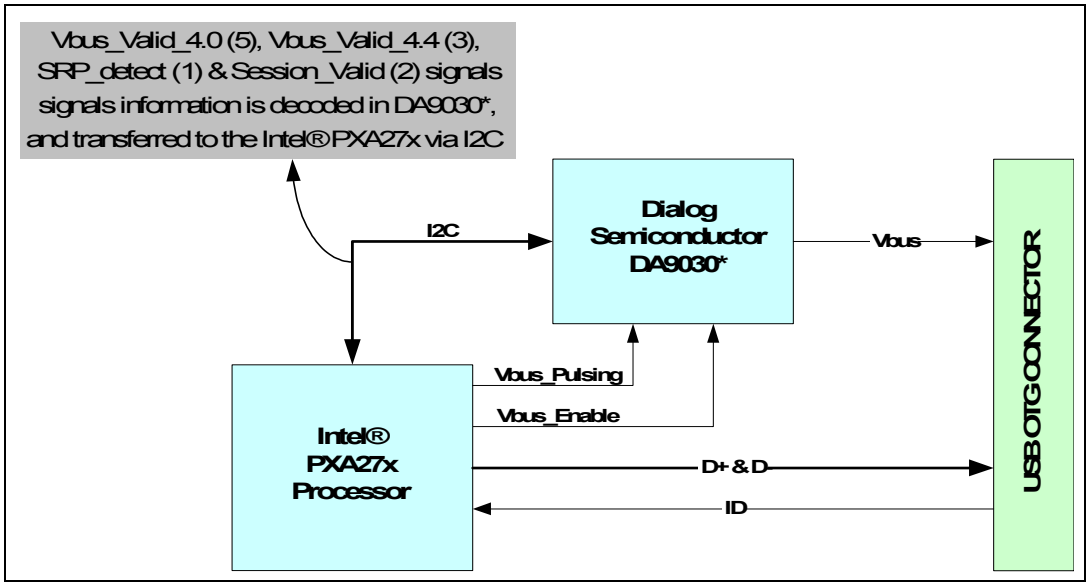
- Charge pump for driving the USB OTG Vbus
- Four detectors for monitoring:
  - VBUS_valid_4_4
  - VBUS_valid_4_0
  - SRP_detect
  - Session_valid
- Vbus controls:
  - Vbus pulsing
  - Vbus enable

The DA9030* USB OTG capability reduces the number of PXA27x processor GPIO pins that need to be used for monitoring. Only three pins are used, instead of seven pins. The four monitor signals are decoded in the DA9030* and delivered to the PXA27x processor via the PWR I^2C bus.

The figure below shows the USB OTG connectivity while using this configuration.

Note: The DA9030* also supports the use of four detectors by real hardware signals.

Figure 13. DA9030* <=> Intel® PXA27x Processor USB OTG Configuration



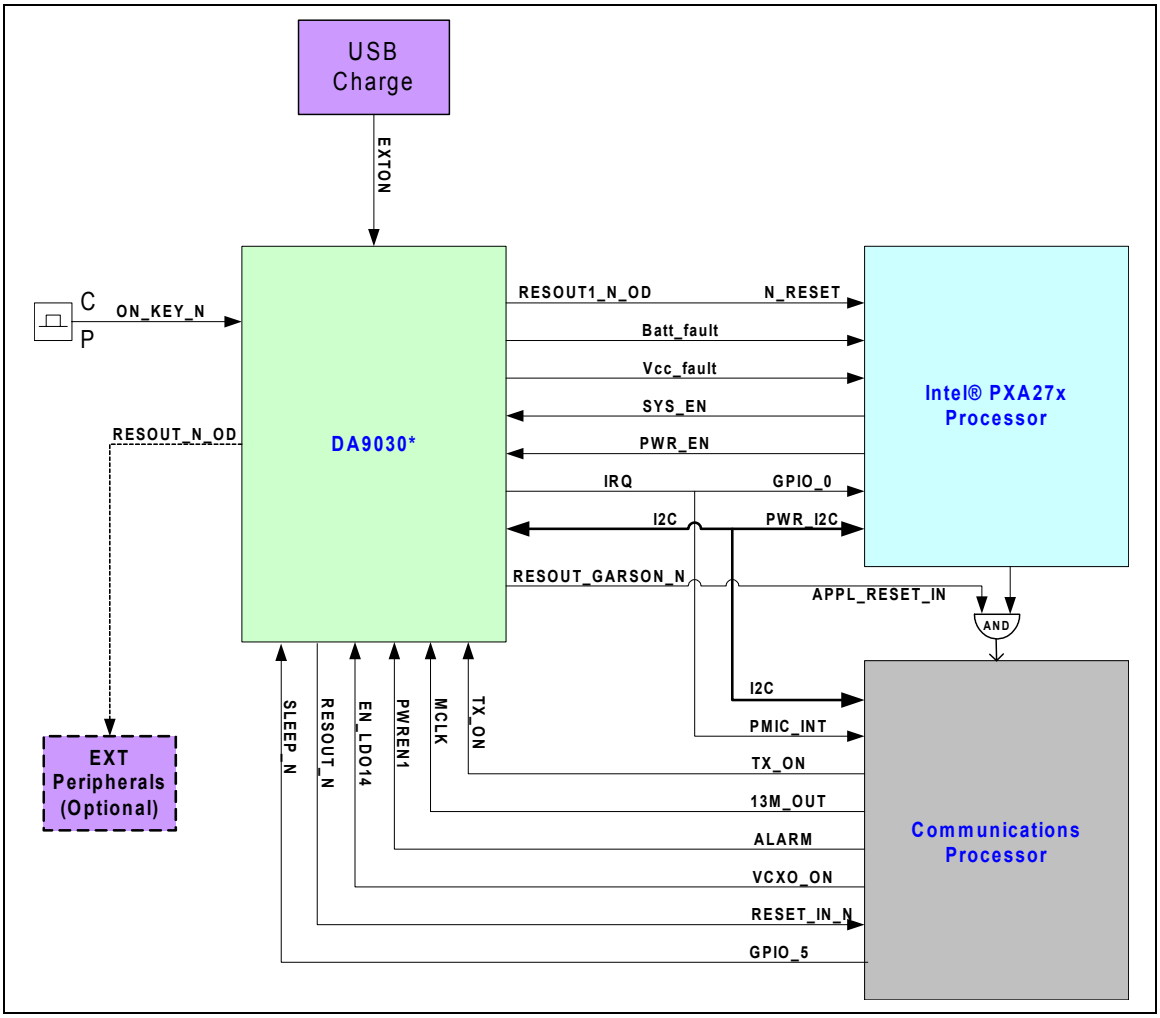
5.1.1.3 Logical Connections

The logical connection between the DA9030* and the rest of the Intel® PXA27x Processor Reference Platform consists of the following signals.

- On_Key_N - Input to the DA9030* from the Intel® PXA27x Processor Reference Platform main power switch button. This will start the DA9030* power-on reset sequence.
- EXT_ON - Alternate ON_KEY input to DA9030* indicates USB insertion for "USB charge" feature, etc.
- I^2C bus - Connects to the PXA27x processor PWR_I^2C and to the communications processor I^2C buses. The DA9030* has two I^2C slave addresses to support access from both processors.
- RESOUT1_N_OD - Open drain reset output; connects to the PXA27x processor nRESET.
- RESOUT_N - Reset-out to communications processor baseband processor; connects to RESET_IN_N of the communications processor.
- RESOUT_GARSON_N - Alternate reset to communications processor baseband processor; allows resetting the communications processor via I^2C command from PXA27x processor side (connects in parallel to PXA27x processor reset-out into communications processor MSL_Reset_In).
- RESOUT_N_OD - DA9030* reset-out for external peripherals (Flash, SDRAM, etc.).
- IRQ - Interrupt request from the DA9030* to both processors indicating power events such as charger inserted or ON_KEY was pressed, etc.
- VCC_FAULT and BATT_FAULT - Indicates power failure in the PXA27x processor LDOs
- SYS_EN and PWR_EN - Input from PXA27x processor to control desired LDOs
- MCLK - DA9030* main clock, coming from communications processor 13M clock-out (MSL_CLK_OUT)
- EN_LDO_14 - communications processor output that controls RF VCTCXO LDO
- SLEEP_N - Active low input to DA9030* from communications processor baseband: indicates that communications processor allows the communications side of the DA9030* to enter sleep mode. Connects to communications processor GPIO5 (valid only for communications processor A4 stepping).
- TX_ON - Timing control from communications processor; indicates transmit burst of the RF. Used for synchronization purposes to battery measurements.
- PWREN1 - Active high input to DA9030* from the communications processor: indicates that the communications processor wants to wakeup from sleep. Connects to the communications processor ALARM output signal.

The following figure shows the logical connections.

Figure 14. DA9030* <=> Intel® PXA27x Processor Reference Platform Logical Connectivity



5.2 Clock Tree

This section describes the Clock flow of the Intel® PXA27x Processor Reference Platform.

Table 8. Intel® PXA27x Processor Reference Platform Clock Allocation

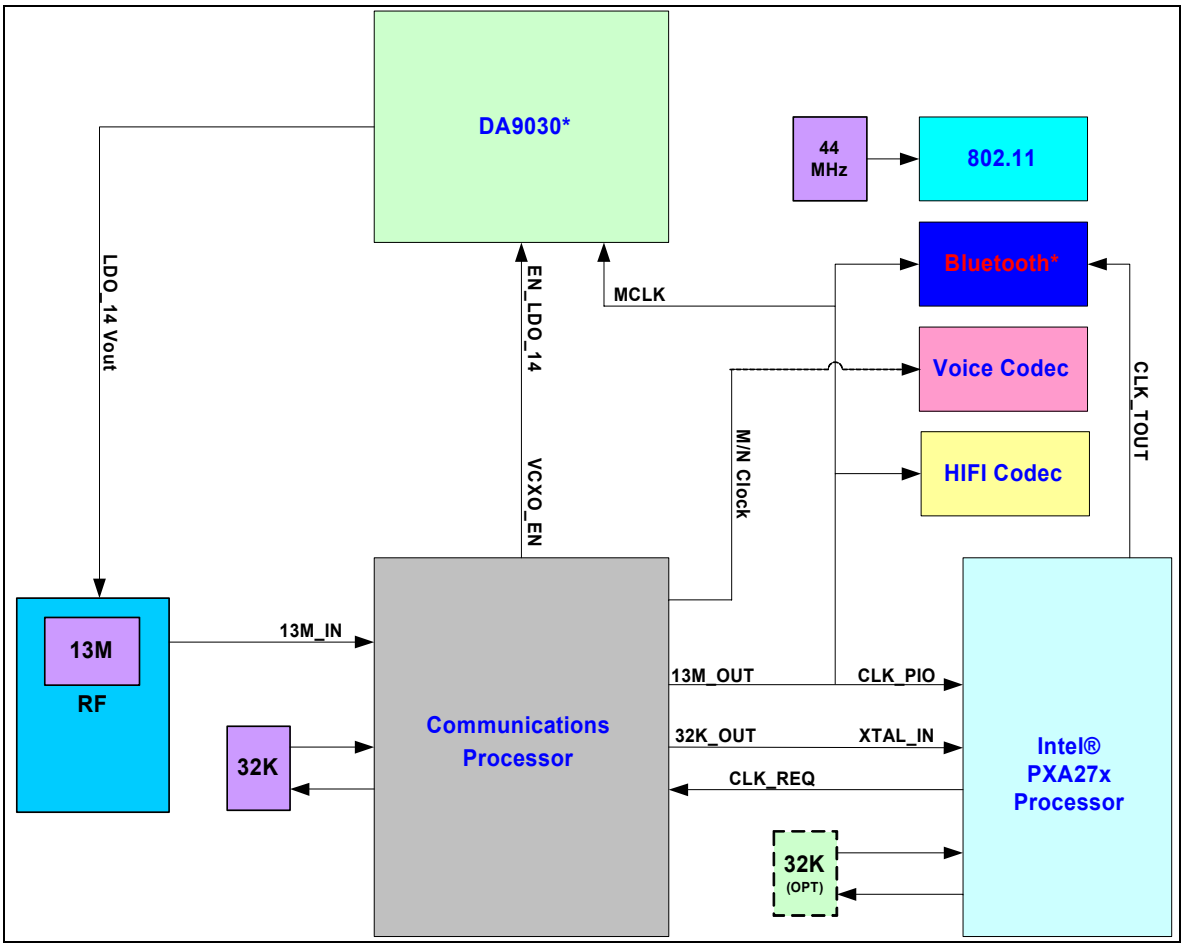
		Intel® PXA27x Processor Reference Platform Clock Sources						
		32K Crystal	RF 13M VCTCXO	44MHz OSO	Intel® PXA27x Processor 32K Out	Communications Processor 32K Out	Communications Processor 13M Out	Communications Processor M/N CLK
Intel® PXA27x Processor Reference Platform Reset Consumers	Intel® PXA27x Processor 32K IN					X		
	Intel® PXA27x Processor 13M IN						X	
	Communications Processor 32K	X						
	Communications Processor 13M IN		X					
	DA9030* MCLK						X	
	Bluetooth* 13M						X	
	Bluetooth* 32K				X			
	Codec Main CLK						X[a]	
	PCM Codec CLK							X[b]
	802.11 RF			X				

a. Can also be driven by AC97_SYSCLK.
b. Set to 2.048 MHz to drive the WM8753 PCM clock.

The figure below shows the clock flow distribution across the Intel® PXA27x Processor Reference Platform.

Dotted lines represent optional connections.

Figure 15. Intel® PXA27x Processor Reference Platform Clock Flow



5.2.1 Clock Tree Functional Description

1. The 13M Main clock originates from the RF VCTCXO and connects to the communications processor 13M_Clock_IN. This clock will shut down only if **ALL** of the following conditions exist ("AND" condition).

- The communications processor is in drowsy state with VCTCXO_OFF
- The PXA27x processor is not requesting the clock (CLK_REQ signal is low)

When all of the conditions are true, the communications processor PMU pulls the VCXO_EN pin down, thus shutting down the VCTCXO LDO (LDO 14) in the DA9030*.

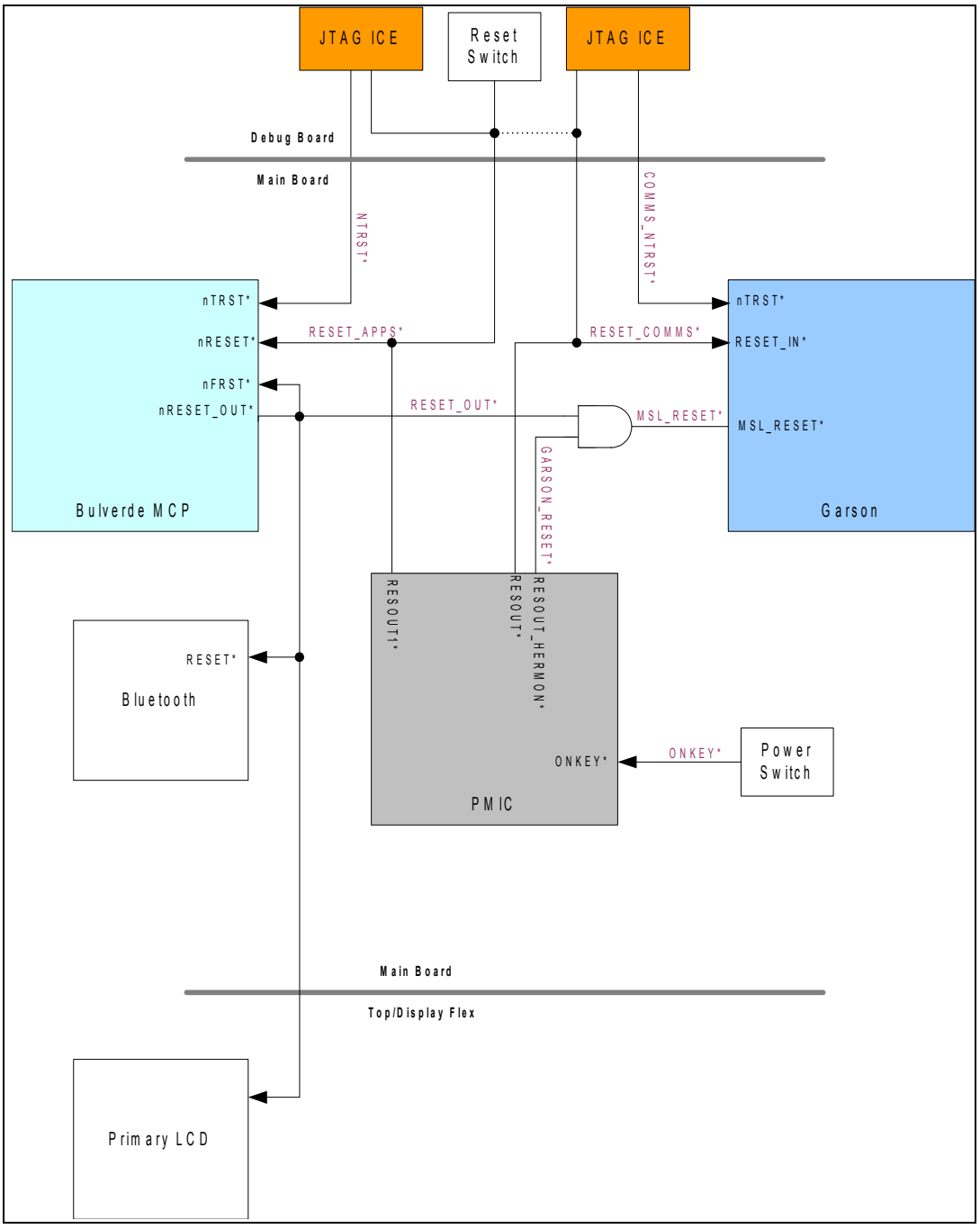
2. The 32K crystal only connects to the communications processor and is driven to the PXA27x processor via GPIO26 (MUX_CLK_0)
3. Bluetooth* 13M is driven from the communications processor 13M out
4. Bluetooth* 32K is driven from the PXA27x processor 32K out
5. 802.11b clock is driven from a dedicated 44MHz oscillator

6. DA9030* MCLK is driven from the communications processor 13M out
7. Voice-band codec PCMCLK/MCLK is driven from the communications processor 13M out

5.3 System Reset

This section describes the reset structure and provides instructions for user-initiated reset.

Figure 16. Reset Logic and Structure



5.3.1 System Power Up and Reset Sequence

For this discussion, Figure 16 depicts the reset logic and structure. The following sequence occurs, after power is applied to the system or after a user-initiated reset.

1. A battery is connected to the system. The DA9030* supplies the VRTC domain, which in turn provides power to the communications processor's VCC_RTC domain and to the PXA27x processor's VCC_BATT domain. The VRTC domain is always powered up when a battery is present in the system. The DA9030* also asserts The BATT_FAULT and VCC_FAULT signals to the PXA27x processor to prevent it from initiating its power-up sequence.

Warning: The Intel® PXA27x Processor Reference Platform should only be powered by the battery or a bench supply connected to the Intel® PXA27x Processor Reference Platform Debug Board. If the Intel® PXA27x Processor Reference Platform is powered by both, the battery could be subjected to higher than allowed currents and fail.

2. Any of the following events occur:
   a. The power switch is pressed
   b. An external charger is connected
   c. The phone is connected to a powered USB Host device

At this point, two independent series of events occur in the DA9030* to power up the PXA27x processor supplies and the communications processor supplies. The two series of events are described below.

PXA27x processor supply power up sequence:

- The DA9030* deasserts (High) the BATT_FAULT signal to the PXA27x processor (indicating that VBAT is ok).
- The DA9030* waits for the PXA27x processor to assert (High) SYS_EN and powers up the domains associated with this signal.
- The DA9030* waits for the PXA27x processor to assert PWR_EN (min. 125ms after asserting SYS_EN) and powers up the sources associated with this signal.

After all sources are stable for the PXA27x processor, the DA9030* will de-assert (High) VCC_FAULT (so the PXA27x processor can continue with its power up sequence).

Communications processor supply power up sequence:

- The DA9030* powers up the several communications processor IO and peripheral domains.
- After a delay of 200 us, the DA9030* powers up the communications processor core and PLL domains.
- After delay of 10 ms, the DA9030* powers up the communications processor's internal Flash domain.

After delay of 64 ms, the DA9030* will dessert RESET_COMMS*.

At this point the necessary power domains are powered on the board and the reset sequence continues:

3. The PXA27x processor asserts RESET_OUT* which places the following devices in reset:

a. The communications processor is placed in MSL Reset, a period during which the communications processor is reset, but it continues to provide the 13MHz clock to the PXA27x processor

b. The Internal Flash device(s) in the PXA271 processor.

c. The Bluetooth* module

d. RESET_APPS* becomes deserted.

4. The PXA27x processor completes its hardware reset procedure and desserts RESET_OUT*. The following actions then occur:

a. The communications processor begins to execute code from its boot memory

b. The Internal Flash device(s) are released from reset and the PXA27x processor fetches its first instruction from address 0x0 on chip select nCS[0]

c. The Bluetooth* module is released from reset.

Table 9. Intel® PXA27x Processor Reference Platform Reset Allocation

		Intel® PXA27x Processor Reference Platform Reset Sources					
		DA9030* APPs Reset (M9)	DA9030* Main Comms Reset (N9)	DA9030* Alt Comms Reset (C11)	DA9030* GP Ext Reset (N11)	Intel® PXA27x Processor Reset_Out (B19)	Intel® PXA27x Processor AC97_Reset (K4)
Intel® PXA27x Processor Reference Platform Reset Consumers	Intel® PXA27x Processor Reset (A16)	X					
	Communications Processor Main Reset (U15)		X				
	Communications Processor Alt Reset (MSL_RESET -N13)[a]			X		X	
	Bluetooth* Reset (G5)					X	
	Camera Reset					X	
	Codec Reset (11)						X
	LCD Reset (J8-2)					X	

a. Note that MSL_RESET is the logical “AND” of DA9030* COMMS_RESET and PXA27x Processor RESET_OUT.

Note: The numbers in brackets indicate the pin numbers of the associated device.

5.3.2 Initiating Reset

To initiate a hardware reset, press and release switch SW1 on an attached Intel® PXA27x Processor Reference Platform Debug Board.

5.4 Two-Chip System Power Management using MSL

5.4.1 General

The main premise behind the power management scheme in the two-chip configuration is that the power management of each subsystem is completely independent.

Each subsystem has an independent sleep schedule that is based on the sleep requirements of the subsystem. The only coordination that will be required between the two systems will be at the MSL Bus Device Driver (BDD) layer. The MSL Bus Device Driver layer eliminates the need to send an "MSL wake signal" for every data packet sent.

In both the communications processor and PXA27x processor subsystems, the MSL bus clock stops one or two clock cycles after the link becomes idle. Each subsystem includes a software mechanism that can detect if there are no tasks executing in the system. The system is allowed to go to sleep when no tasks are executing.

On the communications processor subsystem, the “go to sleep” condition is performed in the Lowest Priority Task. Software entities also have the ability to veto a go to sleep condition. On the communications processor subsystem, this is done by using the functionality of the PMU software driver.

On the PXA27x processor subsystem, this is done using functionality of the Wireless Intel SpeedStep® Power Manager driver.

5.4.2 MSL Power Management

The power management of each subsystem is managed independently and each subsystem has its own sleep schedule. The protocol stack, which must sleep and wake at a very fast rate, governs the communications processor subsystem sleep schedule.

The PXA27x processor subsystem sleep schedule is governed mostly by user input and also by the interactions with the protocol stack on the communications processor subsystem. The PXA27x processor subsystem sleep/wake schedule functions in seconds, whereas the communications processor subsystems schedule functions in milliseconds.

The MSL Data Link bridges the two independent subsystems.

On the communications processor subsystem, when data is sent over the MSL link, the BDD sends the data and 7then waits a configured settling period for more data. The default Data Link Settle period is 10 ms, because the Data Link must wait for at least 2 GSM frames that do not contain data before allowing the system to go to sleep. For packet data coming from the network, data is generally sent in intervals equal to the length of a frame. If one GSM data packet is too large to be transmitted in a single GSM frame, the remainder of the packet is put into the next frame. A window of time greater than two empty GSM frames is sufficient to trigger the MSL peripheral to enter sleep mode. This configured settle period has the potential to drastically change the sleep characteristics of the system. Careful consideration must be made when making changes to the configured settle period of the MSL Data Link.

Figure 17 below shows a general MSL sleep scenario using the settle period.

Figure 17. MSL Sleep Settle Period

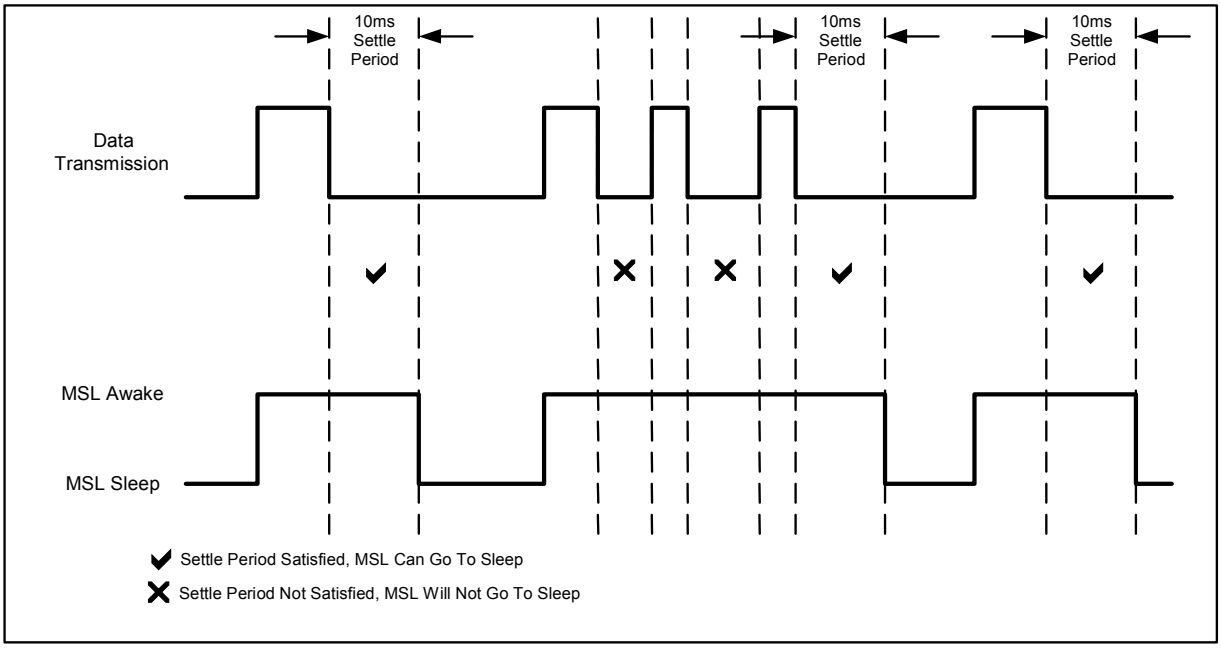
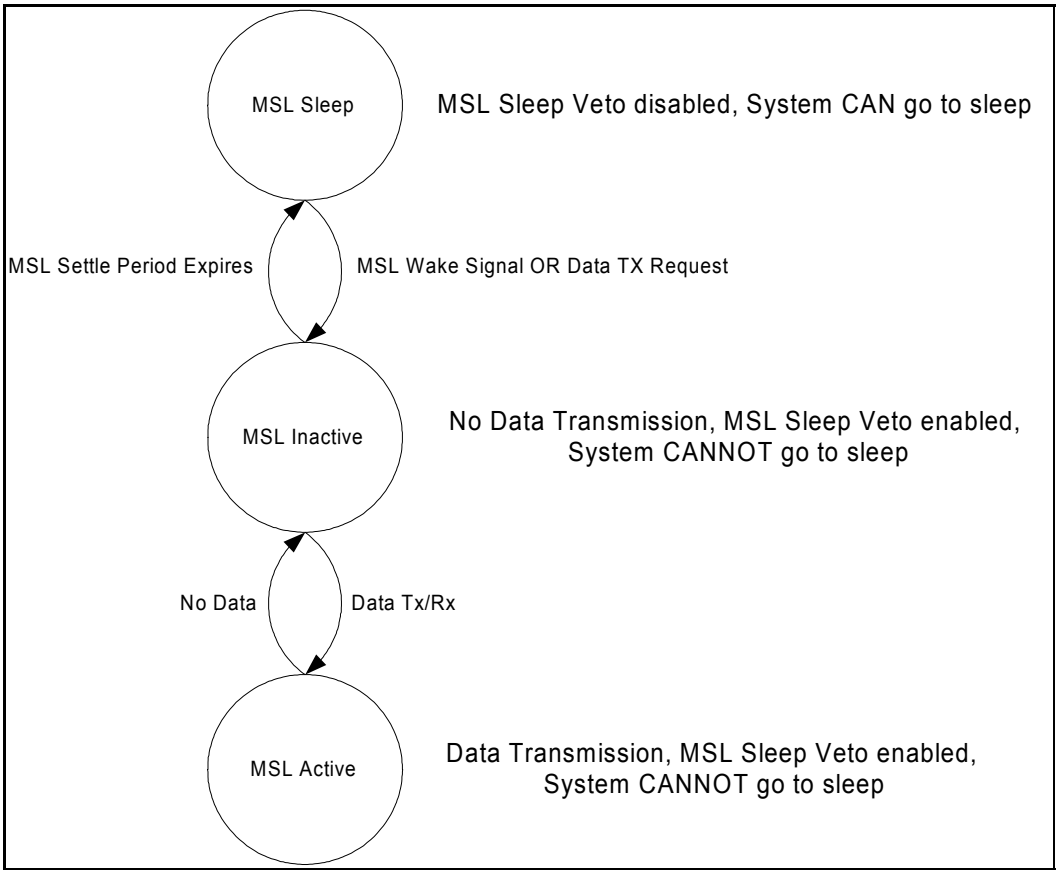


Figure 18. MSL DL Power Management States



Before the MSL BDD disables the MSL clock, a "sleep indication" is sent to the PXA27x processor MSL BDD that the communications processor MSL link is going to sleep. When the "sleep acknowledge" returns from the PXA27x processor MSL BDD, the communications processor MSL BDD disables both the MSL clock and the system sleep veto. The communications processor subsystem can now resume the normal sleep schedule.

The process is the same from the PXA27x processor subsystem to the communications processor.

When data arrives right after receiving the sleep indication, a sleep "cancel" or "NACK" is sent instead of the "sleep acknowledge".

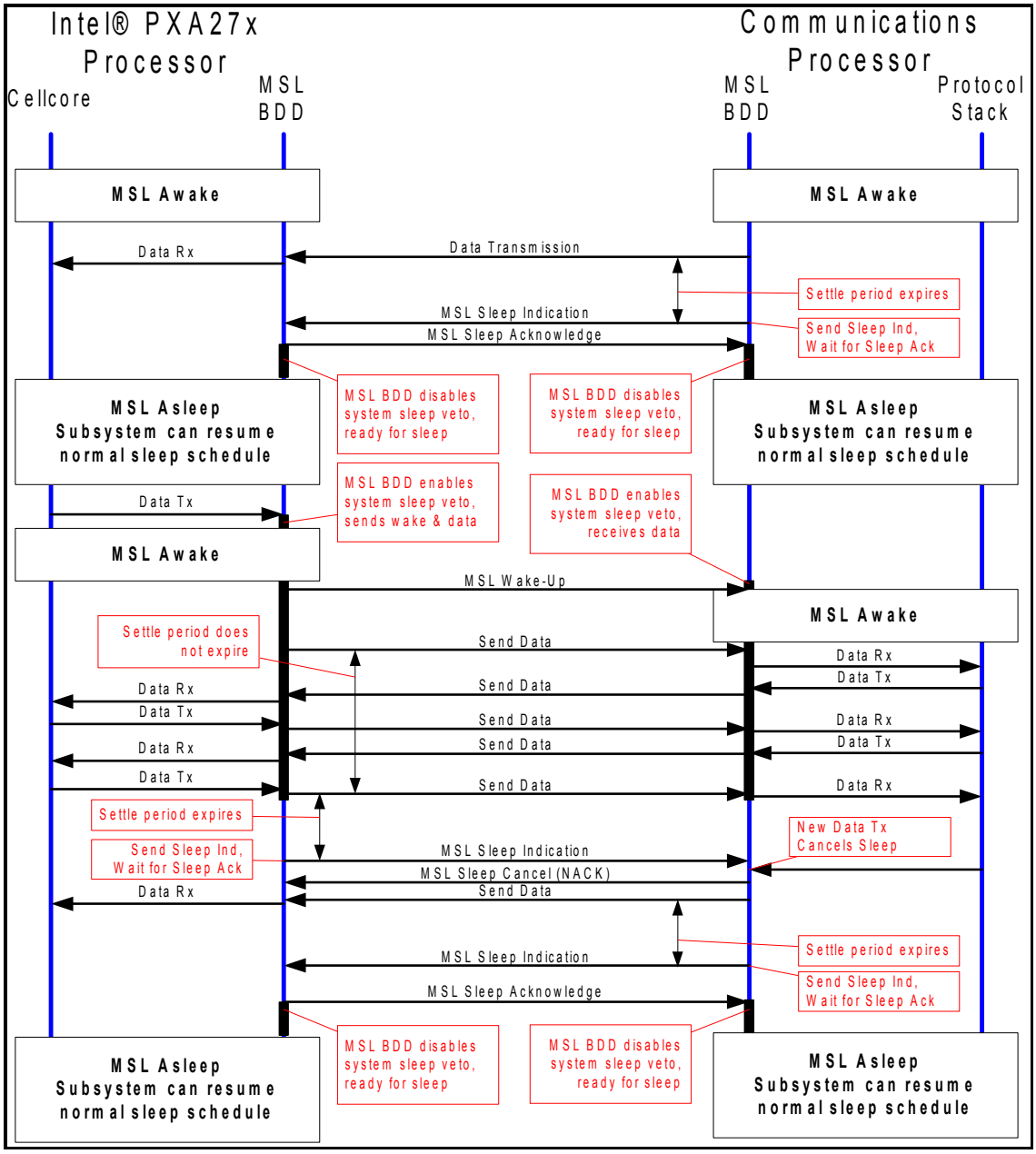
Upon wake-up, from a local initiated wake-up, data cannot be sent until a “wake request’ is received.

Therefore, the sleep/wake activity of the MSL Data Link, as well as the entire subsystem sleep, is governed by the activity on the MSL link.

- When there is activity on the MSL link, neither system can go to sleep.
- When there is no activity, each subsystem can resume the normal sleep schedule, independently.

Figure 19 below shows the power management sequences on the MSL link and the implication on the overall system sleep.

Figure 19. System Power Management Sequence



5.4.3 MSL Wake

When one of the subsystem's MSL links is asleep, a "wake signal" is required before sending data to it. Since the MSL link is configured with Dynamic Flow Control (DFC) enabled, by default, there is no need to wait after sending the "wake signal". Data can be sent immediately after sending the "wake signal" and the MSL BDD layer will only physically transmit the data after DFC is disabled.

5.4.4 Power Management During a Call (Voice and Data)

During the initiation of a voice call, either mobile terminated or mobile originated, both subsystems are awake.

After the call is connected, the communications processor subsystem is precluded from sleeping but the PXA27x processor subsystem can enter sleep mode.

The PXA27x processor subsystem will only wake up from user input or to process information coming from the communications processor subsystem such as Receive Signal Strength Indications.

During a data call, the PXA27x processor subsystem can sleep when no data is sent or received.

The communications processor subsystem is not able to sleep because it processes the active call.

5.5 Power Consumption Approximations

The purpose of this section is to show the theoretical power consumption expected from the full Intel® PXA27x Processor Reference Platform system. This section only presents the outcome of the analysis and the assumptions behind it.

This information is the result of a theoretical analysis done by Intel.

5.5.1 Assumptions and Modes Definitions

The following items are the key system assumptions taken in the calculations.

- Battery capacity is 700mAh (Intel® PXA27x Processor Reference Platform normal battery).
- RF TX power for Voice and data calculation is 29dBm (GSM testing typical number).
- Average battery voltage is 3.6 (Li-ion).
- DA9030* is used in the Intel® PXA27x Processor Reference Platform.

5.5.1.1 “Hard Stand-By" Mode Definition

Intel® PXA27x Processor Reference Platform "HARD-STBY" mode is defined as a mode where the Intel® PXA27x Processor Reference Platform is left untouched by the user; the communication subsystem is synchronized to a real network (but working with the 32K crystal).

The following list summarizes the mode conditions:

- Communications processor is in drowsy mode with 13M OFF (CLK_REQ is low).
- PXA27x processor is in sleep mode with all power domains, except VBAT and SDRAM core, OFF.
- PXA27x processor’s SDRAM is in self-refresh mode.
- Codec is OFF.
- Bluetooth* subsystem is OFF.
- 802.11 subsystem is OFF.

- All application peripherals, such as Camera, SDIO, main LCD and backlight, are OFF.
- Status LCD is ON (backlight is OFF).
- Keypad backlight is OFF.

5.5.1.2 Hard STBY Mode Results

Results	Value	Units
Battery Capacity	700	mA-Hr
STBY mode Current	3.49	mA
STBY Time	200.72	Hours
	8.36	Days

5.5.1.2.1 Detailed Results

The following table shows the power consumed by each Intel® PXA27x Processor Reference Platform components during STBY mode.

Table 10. STBY Detailed Results

STBY Mode Currents by Components	Value	Units	%
Comm + RF	1.653	mA	47.4%
Intel® PXA27x Processor + Memories	0.450	mA	12.9%
Bluetooth*	0.100	mA	2.9%
LCD	0.000	mA	0.0%
Status LCD	0.110	mA	3.2%
Keypad EL	0.000	mA	0.0%
ON devices at all times	0.409	mA	11.7%
Codec (HiFi+Voice)	0.092	mA	2.6%
Camera	0.010	mA	0.3%
IrDA	0.000	mA	0.0%
DA9030*	0.364	mA	10.4%
Miscellaneous	0.300	mA	8.6%
Total	3.49	mA	100.0%
	12.55	mW	

5.5.1.3 “PDA" Mode Definition

Intel® PXA27x Processor Reference Platform "PDA" mode is defined as a mode where the communications processor subsystem is in STBY mode (i.e. synchronized to a real network), but the user is operating other applications on the PXA27x processor subsystem such as:

- MP3 playback
- Game play

- Video playback

This mode can be referred to also as PDA only mode (or "Flight" mode). The application side is active according to an average PDA usage model, while the communication side is in standby mode and supplying the application side main clock.

The following list summarizes the mode conditions:

- Communications processor is drowsy mode with 13M ON (CLK_REQ is high).
- PXA27x processor is:
  - 20% running at 104 MHz
  - 20% running at 208 MHz.
  - 10% running at 312 MHz.
  - 10% running at 416 MHz.
  - 15% in idle mode.
  - 15% in sleep mode.
  - 10% in deep sleep mode
- Codec is 20% ON (DAC only mode-MP3, game tones, movie sound track, etc.).
- Bluetooth* subsystem is 10% ON (for data application only).
- 802.11b subsystem is OFF.
- Camera is used for 10%.
- SDIO is used for 20% (storage usage).
- Main LCD is ON while the backlight is 30% ON.
- Status LCD is ON while the backlight is 30% ON
- Keypad backlight is 20% ON
- IrDA is used 4% the time.

5.5.1.4 PDA Mode Results

Table 11. PDA Results Summary

Results	Value	Units
Battery Capacity	700	mA-Hr
PDA+ mode Current	151.16	mA
PDA Time	4.63	Hours

5.5.1.4.1 Detailed Results

The following table shows the power consumed by each Intel® PXA27x Processor Reference Platform components during PDA mode.

Table 12. PDA Detailed Results

PDA Mode Currents by Components	Value	Units	%
Comm + RF	1.653	mA	1.1%
Intel® PXA27x Processor + Memories	98.770	mA	65.3%
Bluetooth*	7.518	mA	5.0%
LCD	13.733	mA	9.1%
Status LCD	6.110	mA	4.0%
Keypad EL	6.400	mA	4.2%
ON devices at all times	0.692	mA	0.5%
Codec (HiFi+Voice)	9.748	mA	6.4%
Camera + Strobe	3.059	mA	2.0%
IrDA	2.278	mA	1.5%
DA9030*	0.202	mA	0.1%
Miscellaneous	1.000	mA	0.7%
Total	151.16	mA	100.0%
	544.18	mW	

5.5.1.5 Voice-Only Mode Definition

Intel® PXA27x Processor Reference Platform "Voice only" mode is defined as a mode where the communications processor subsystem is in voice-mode (i.e. receiving & transmitting 1 TS of voice samples on a GSM network), while the PXA27x processor subsystem is in active mode with MMI functions only. The following list summarizes this mode conditions:

- Communications processor is in Voice mode with 13M ON (CLK_REQ is high).
- PXA27x processor is:
  - 10% Active mode running at 104 MHz
  - 30% in idle mode.
  - 60% in sleep mode.
- Codec is ON (PCM section only).
- Bluetooth* subsystem is in deep sleep.
- 802.11 subsystem is OFF.
- Camera is OFF.
- SDIO is OFF.
- Main LCD is ON while the backlight is 30% ON.
- Status LCD is ON while the backlight is 30% ON
- Keypad backlight is 5% ON.

5.5.1.6 Voice Mode Results

Table 13. Voice Mode Results Summary

Results	Value	Units
Battery Capacity	700	mA-Hr
Voice mode Current	268.19	mA
Voice Time	2.61	Hours

5.5.1.6.1 Detailed Results

The following table shows the power consumed by each Intel® PXA27x Processor Reference Platform components during Voice mode.

Table 14. Voice Mode Detailed Results

Voice Mode Currents by Components	Value	Units	%
Comm + RF	194.770	mA	72.6%
Intel® PXA27x Processor + Memories	35.576	mA	13.3%
Bluetooth*	0.000	mA	0.0%
LCD	13.733	mA	5.1%
Status LCD	6.110	mA	2.3%
IrDA	0.000	mA	0.0%
Camera + Strobe	0.010	mA	0.0%
Keypad EL	1.600	mA	0.6%
ON devices at all times	0.786	mA	0.3%
Codec (HiFi+Voice)	14.604	mA	5.4%
Miscellaneous	1.000	mA	0.4%
Total	268.19	mA	100.0%
	965.48	mW	

5.5.1.6.2 Bluetooth* Implication

When Bluetooth* is used for voice streaming using a Bluetooth* earphone instead of the Intel® PXA27x Processor Reference Platform integrated earphone, the power is slightly changed.

The following table summaries the result

Table 15. Voice Mode Results Using Bluetooth*

Results	Value	Units
Battery Capacity	700	mA-Hr
Voice mode Current	295.54	mA
Voice Time	2.37	Hours

5.5.1.7 Data Mode Definition - GPRS

Intel® PXA27x Processor Reference Platform "GPRS DATA" mode is defined as a mode where the communications processor subsystem is in "GPRS Class 12 DATA" mode (i.e. 4 TS of downlink data and 1 TS of uplink data on a GPRS network), while the PXA27x processor subsystem is active to support data applications such as:

- Web surfing
- Mail applications
- MSN messenger
- VOIP
- ECommerce
- OTA applications

The following list summarizes the mode conditions:

- Communications processor is in "GPRS-Data" mode with 13M ON (CLK_REQ is high).
- PXA27x processor is:
  - 60% Active running at 208 MHz
  - 30% in idle mode.
  - 10% in sleep mode.
- Codec is 50% ON (for MMS like applications, DAC only mode).
- Bluetooth* subsystem is in deep sleep
- 802.11 subsystem is OFF.
- Camera is OFF.
- SDIO is OFF.
- Main LCD is ON while the backlight is 30% ON.
- Status LCD is ON while the backlight is 30% ON
- Status LED (network indication is ON).
- Keypad backlight is 10% ON.

5.5.1.8 GPRS Data Mode Results

Table 16. GPRS Data Mode Results Summary

Results	Value	Units
Battery Capacity	700	mA-Hr
Data mode Current	370.21	mA
GPRS Data Time	1.89	Hours

5.5.1.8.1 Detailed Results

The following table shows the power consumed by each Intel® PXA27x Processor Reference Platform components during GPRS data mode.

Table 17. GPRS Data Mode Detailed Results

Data Mode Currents by Components	Value	Units	%
Comm + RF	225.650	mA	61.0%
Intel® PXA27x Processor + Memories	101.633	mA	27.5%
802.11	0.000	mA	0.0%
Bluetooth*	0.100	mA	0.0%
LCD	19.843	mA	5.4%
Status LCD	6.110	mA	1.7%
SD	0.000	mA	0.0%
Keypad EL	3.200	mA	0.9%
IrDA	0.000	mA	0.0%
Camera + Strobe	0.010	mA	0.0%
ON devices at all times	0.786	mA	0.2%
Codec (HiFi+Voice)	11.880	mA	3.2%
Miscellaneous	1.000	mA	0.3%
Total	370.21	mA	100.0%
	1332.76	mW	

5.5.1.9 Data Mode Definition - 802.11

Intel® PXA27x Processor Reference Platform "802.11 DATA" mode is defined as a mode where the communications processor subsystem is in STBY mode (i.e. synchronized to a real network), while the PXA27x processor subsystem is in active mode and running an 802.11 host protocol for applications such as:

- Web surfing
- Mail applications
- MSN messenger
- VOIP using Bluetooth*

- ECommerce
- OTA applications

The following list summarizes the mode conditions:

- Communications processor is in "STBY" mode with 13M ON (CLK_REQ is high).
- PXA27x processor is:
  - 80% Active running at 416 MHz
  - 15% in idle mode.
  - 5% in sleep mode.
- Codec is 50% ON (for MMS like applications, DAC only mode).
- Bluetooth* subsystem is 10% ON.
- 802.11 subsystem is 100% ON at the following usage model
  - 15% TX mode
  - 60% RX mode.
  - 5% wait mode
  - 20% idle mode.
- Camera is OFF.
- SDIO is OFF.
- Status LCD is ON while the backlight is 30% ON
- Status LED (network indication is ON).
- Keypad backlight is 10% ON.

5.5.1.10 802.11 Data mode Results

Table 18. 802.11 Data Mode Results Summary

Results	Value	Units
Battery Capacity	700	mA-Hr
Data mode Current	397.82	mA
802.11 Data Time	1.76	Hours

5.5.1.11 Detailed Results

The following table shows the power consumed by each Intel® PXA27x Processor Reference Platform components during 802.11 data mode.

Table 19. 802.11 Data Mode Detailed Results

Data Mode Currents by Components	Value	Units	%
Comm + RF	1.653	mA	0.4%
Intel® PXA27x Processor + Memories	155.626	mA	39.1%
802.11	197.610	mA	49.7%

Table 19. 802.11 Data Mode Detailed Results

Data Mode Currents by Components	Value	Units	%
Bluetooth*	0.100	mA	0.0%
LCD	19.843	mA	5.0%
Status LCD	6.110	mA	1.5%
SD	0.000	mA	0.0%
Keypad EL	3.200	mA	0.8%
IrDA	0.000	mA	0.0%
Camera + Strobe	0.010	mA	0.0%
ON devices at all times	0.786	mA	0.2%
Codec (HiFi+Voice)	11.880	mA	3.0%
Miscellaneous	1.000	mA	0.3%
Total	397.82	mA	100.0%
	1432.15	mW	

Intel® PXA27x Processor Reference Platform Wireless Subsystems 6

6.1 Bluetooth*

Bluetooth* is an industry specification that describes how mobile phones, computers, and PDAs can seamlessly interconnect with each other and with network access points and local services using a short-range wireless connection. Bluetooth* wireless technology revolutionizes the personal connectivity market by providing freedom from wired connections, enabling the formation of wireless personal area networks (WPAN).

6.1.1 Supported Profiles and Applications

The following profiles are supported:

- Headset
- Hands-Free
- Personal Area Network (PAN)
- Dial-Up Network (DUN)
- Object Push

6.1.1.1 Headset Profile (HSP)

The HSP enables use of wireless Bluetooth* headsets for voice calls. The headset device allows voice dialing using Voice Recognition, (if supported by the handset), call disconnection from the headset, and remote handset volume control.

6.1.1.2 Hands-Free Profile (HFP)

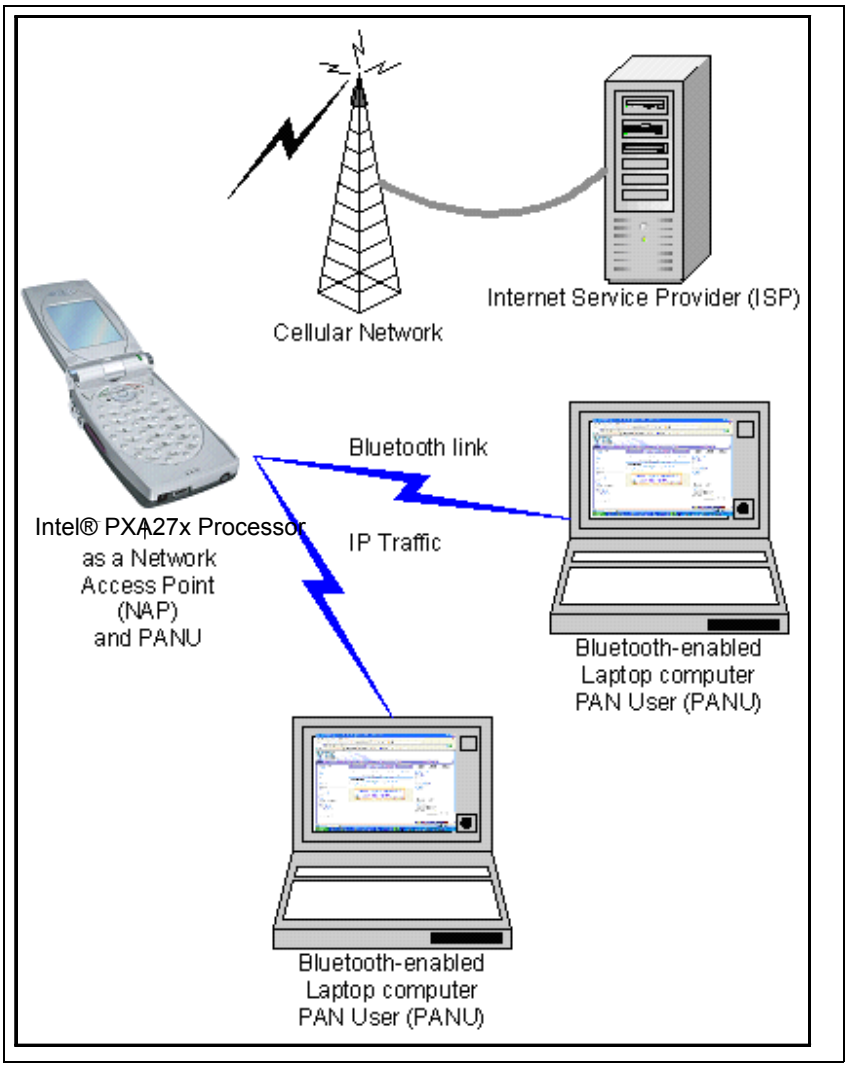
The hands-free profile (HFP) defines a functionality which allows a mobile phone to be used with a Hands-Free device. It differs from the headset profile (HSP) because it provides a means for remote control of the mobile and wireless voice connection.

The connection between the mobile phone and the HF unit is performed with Bluetooth* technology, based on serial cable emulation, using the RFCOMM protocol. For this purpose, the HFP relies directly on the procedures of the Serial Port Profile (SPP).

An implementation of the Hands-Free Profile typically enables a car's embedded Hands-Free unit ("Bluetooth* car-kit") to be wirelessly connected to a cellular phone for the purposes of acting as the cellular phone's audio input and output mechanism. This provides full duplex audio and functionality of mobile phone remote control, voice recognition, noise suppression, and acoustic echo cancellation.

6.1.2 Personal Area Networking (PAN)

Figure 20. PAN Usage Models



The PAN profile determines the rules for carrying IP traffic across Bluetooth* connections.

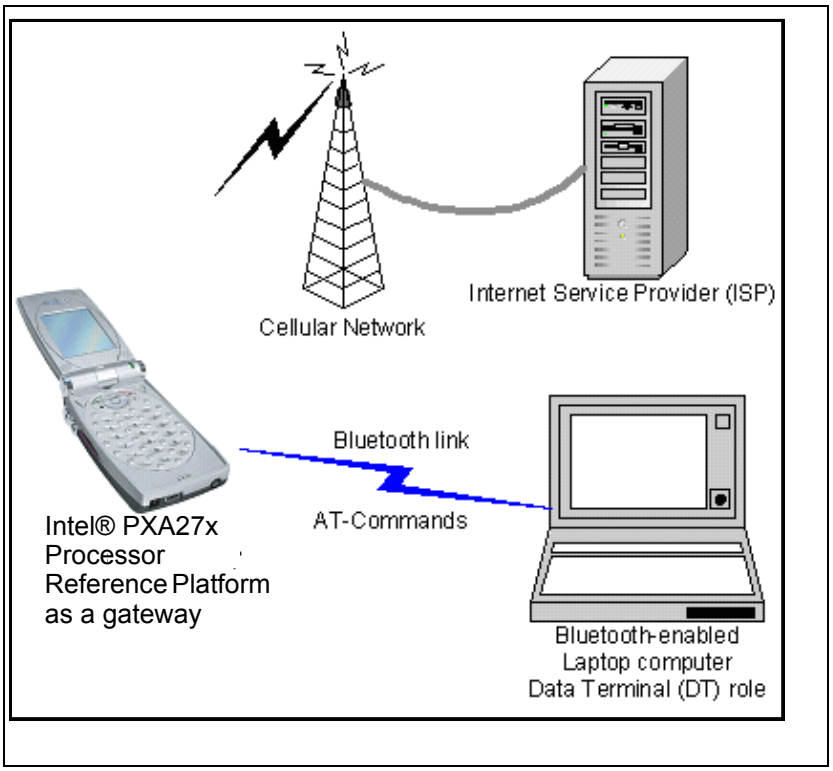
The IP traffic is sent in Ethernet packets that are encapsulated in L2CAP packets according to the Bluetooth* Network Encapsulation Protocol (BNEP).

A Bluetooth* technology enabled, mobile phone supported, PAN profile can serve as a network access point (NAP) for a PAN user (e.g., a Bluetooth* technology enabled laptop computer), for packet-switched, and web-surfing.

Alternatively, it can run as a PAN user in order to exchange data files in an IP-based manner with other PAN devices (a second Intel® PXA27x Processor Reference Platform-like phone).

6.1.3 Dial-Up Network (DUN)

Figure 21. DUN Usage Model



6.1.3.1 DUN Usage Profile

The DUN profile enables a Bluetooth*-enabled laptop (acting as a data-terminal) to use a Bluetooth*-enabled cellular mobile phone (acting as a gateway), as a wireless modem, to connect to an ISP (for web surfing, for example) using circuit switched data-call ("dial-up network") over a GSM network. The DUN profile makes use of standard AT-commands during the command mode in which the data call is being placed.

The Bluetooth* DUN application virtually emulates a serial cable replacement mechanism, so that the cellular application layer (AT-parser in this case) does not notice whether the laptop is connected to it using a physical RS-232 cable, or a virtual, Bluetooth* technology emulated, serial cable.

6.1.3.2 Generic Object Exchange (OBEX)

The Generic Object Exchange profile allows for OBEX object-exchange protocols to be used over Bluetooth* links. Other profiles, such the Synchronization profile, build upon this basis providing synchronization of contacts, calendars, e-mails, notes, and tasks. The Object Push and File Transfer Profile provide a standard by which data objects can be pushed to another device to provide for the exchange of business cards and meetings.

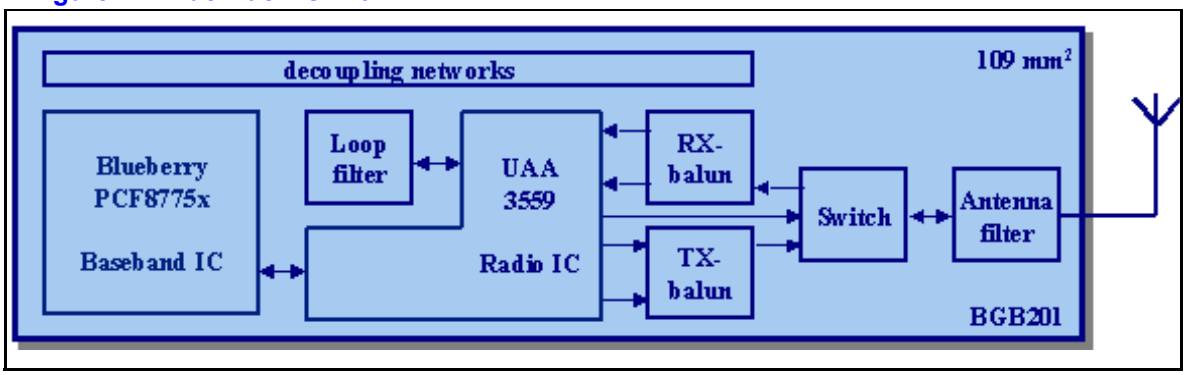
6.1.4 Intel® PXA27x Processor Reference Platform Bluetooth* Concept

Bluetooth* is integrated into the Intel® PXA27x Processor Reference Platform as an external single chip, combining the baseband and the RF. The Bluetooth* connects using a 4-line UART interface to the PXA27x processor, which hosts the external Bluetooth* host controller. In addition, the external Bluetooth* contains PCM audio interfaces connected to both the PXA27x processor and communications processor. The Bluetooth* host-stack and applications run on the PXA27x processor. The connectivity to the communications processor is only with PCM for voice call scenarios.

6.1.5 Philips TrueBlue* (BGB201)

The Intel® PXA27x Processor Reference Platform uses the Philips's TrueBlue Bluetooth* module. The TrueBlue BGB201 is a multi-chip module incorporating a baseband processor, embedded flash memory, near zero IF transceiver chip, and all the critical RF parts (such as baluns, TX/RX switch and a bandpass filter).

Figure 22. TrueBlue BGB201



6.1.6 BGB201 Hardware Interfaces with Intel® PXA27x Processor Reference Platform

6.1.6.1 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices. The UART acts as the HCI transport layer (H4). The interface consists of 4 lines:

Table 20. UART Signal Description

Signal	Description
BT_TXD	UART data output active high
BT_RXD	UART data input active high
BT_RTS	UART request to send active low
BT_CTS	UART clear to send active low

6.1.6.2 PCM

The Audio Pulse Code Modulation (PCM) interface supports continuous transmission and reception of PCM-encoded audio data over Bluetooth*.

The PCM interface is used in profiles where raw audio transmission is involved, such as headset and hands-free. The interface consists of 4 lines:

Table 21. Bluetooth* PCM Signal Description

Signal	Description
AUDIO_SSPTXD	PCM data output active high
AUDIO_SSPRXD	PCM data input active high
AUDIO_SSPCLK	Synchronous data clock
AUDIO_SSPFRM	Synchronous frame sync

The BC02 PCM I/F can be configured as either a master or a slave.

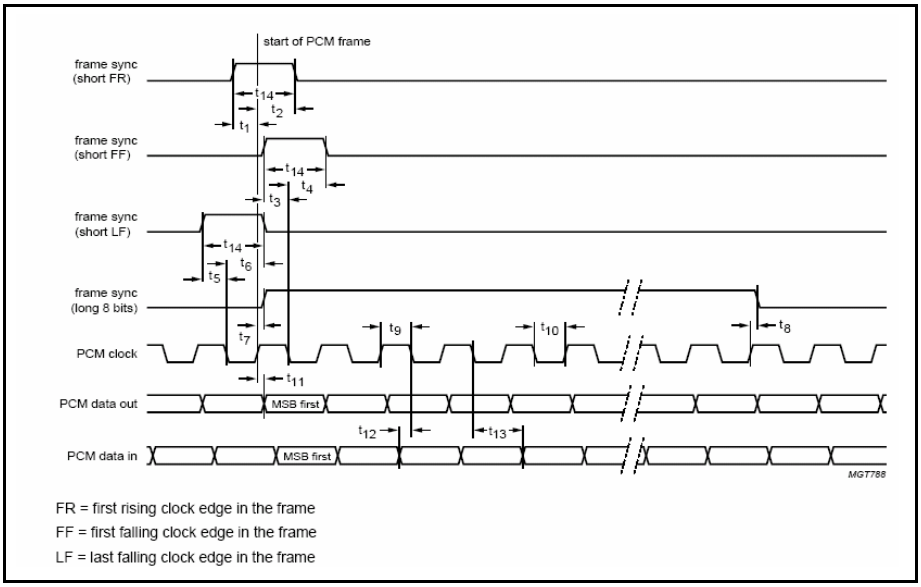
PCM Master Mode

When configured as a master, the BGB201 drives the PCM_CLK signal, at 2.048 MHz.

PCM Format

The PCM format that will be used as the short-sync format as described in **Figure 20**.

Figure 23. BGB201 PCM Short Frame Sync Format



6.1.7 BGB20 Power Consumption

Table 22. BGB201 Power Consumption

Domain	Event	Current Consumption
IDD(BB) baseband supply current	SCO link, HV1 packets, ARM running at 27%	15 mA
IDD(RF) RF supply current		27 mA
IDD(BB) baseband supply current	SCO link, HV2 packets, ARM running at 27%	15 mA
IDD(RF) RF supply current		14 mA
IDD(BB) baseband supply current	SCO link, HV3 packets, ARM running at 27%	15 mA
IDD(RF) RF supply current		10 mA
IDD(BB) baseband supply current	ACL link; DM1 or DH1 bidirectional packets; ARM running at 100%	25 mA
IDD(RF) RF supply current		27 mA
IDD(BB) baseband supply current	ACL link; DM3 or DH3 bidirectional packets; ARM running at 100%	25 mA
IDD(RF) RF supply current		34 mA
IDD(BB) baseband supply current	ACL link; DM5 or DH5 packets both directions; ARM running at 100%	25 mA
IDD(RF) RF supply current		35 mA
IDD(BB) baseband supply current	ACL link; DM5 or DH5 packet transmit, NULL packet receive; ARM running at 100%	25 mA
IDD(RF) RF supply current		27 mA
IDD(BB) baseband supply current	ACL link; DM5 or DH5 packet receive, NULL packet transmit; ARM running at 100%	25 mA
IDD(RF) RF supply current		33 mA
IDD(BB) baseband supply current	low-power scanning	0.55 mA
IDD(RF) RF supply current		0.40 mA

6.1.8 Antenna Filter Definition

A Murata LFB212G45SG8A166 Band Pass Filter is used to minimize the out-of-band interference from the Bluetooth* module. This filter has a center frequency of 2.45GHz and a bandwidth of 50MHz with an insertion loss of 1.40 dB max at 25 Celsius.

6.1.9 Bluetooth* Antenna Design

A Gigaant Rufa 2.4GHz surface mount antenna is used with the following parameters.

6.1.9.1 Master Clock Supply

The BGB201 is clocked with a 13MHz square wave clock coming from the MSL_13MCLK signal coming from the communications processor.

6.1.9.2 Low Power Oscillator

The BGB201 is also provided with a 32KHz clock from the PXA27x processor CLK_TOUT pin.

6.1.10 BGB201 Power Modes

6.1.10.1 Processor Stop

In Processor Stop mode, the processor's clock is stalled from its normal 13 MHz. Because CMOS power consumption is roughly proportional to clock frequency, the stall has a corresponding effect on power consumption. In this mode, the microcontroller can be restarted with little latency overhead by any of the wake-up sources. The stop mode should be used to stall the microcontroller for short periods, such as in the idle loops of the host software code.

6.1.10.2 Sleep

In this mode the main clock is shut down, further reducing power consumption until a wake-up signal or reset condition occurs. The 32KHz clock remains active to maintain the state. Since sleep mode has a longer restart latency than stop mode, it should only be used to halt the complete Bluetooth* system for longer periods of time.

6.2 802.11b WLAN

A wireless LAN (WLAN) allows mobile users to connect to a LAN through a wireless radio connection. Several specifications exist to ensure the compatibility between access points and clients: the most prevalent being the IEEE 802.11b, providing encryption and a bandwidth of 11Mbps. WLAN enables higher productivity, functionality, and convenience by untethering the user from any single wired port and allowing him to access their databases and services remotely.

6.2.1 Intel® PXA27x Processor Reference Platform WLAN Concept

802.11b has been integrated into the Intel® PXA27x Processor Reference Platform as two external chips. One chip is the baseband processor and the other chip is the radio module, utilizing less then 200mm2 of PCB real estate.

6.2.2 Philips SA2443 and BGW100

The Intel® PXA27x Processor Reference Platform uses the Philips's SA2443 baseband/MAC and BGW100 2.4GHz radio chipset. This complete 802.11b chipset offers the lowest standby power, smallest form factor, and highest integration for mobile handheld devices.

6.2.3 SA2443 Hardware Interfaces with Intel® PXA27x Processor Reference Platform

The 802.11b interfaces to the PXA27x processor using a high speed SPI with a throughput of 13Mbps, simplifying board routing by utilizing only 5 signals to the applications processor. It should be noted that this SPI is shared with the primary LCD command and control, which is only used during the power up and power down of the primary LCD. Software drivers will need to ensure that WLAN is not accessed during LCD configuration.

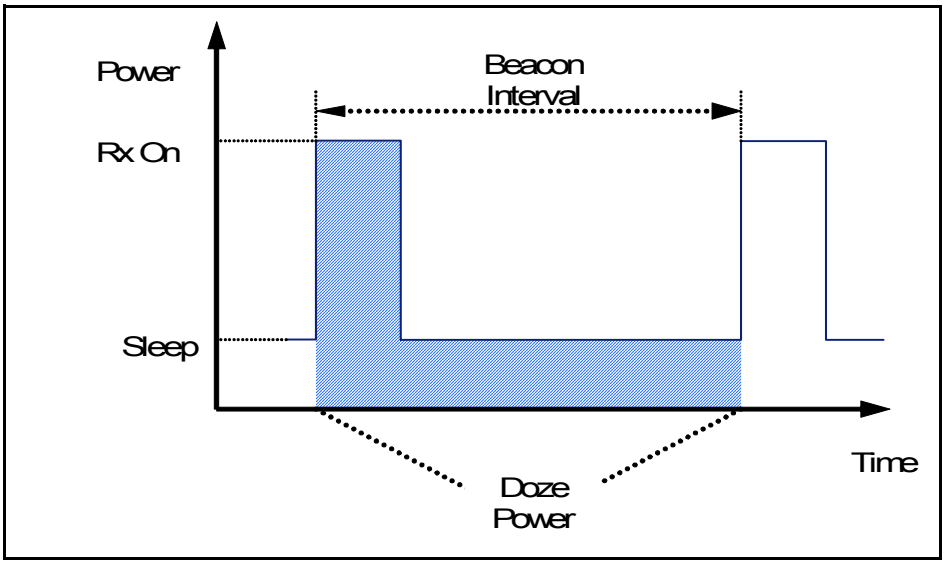
Table 23. WLAN Signals

Signal	Description
WLAN_SSPTXD	Data output active high
WLAN_SSPRXD	Data input active high
WLAN_SSPCLK	Synchronous data clock
WLAN_SS*	Slave Select active low
WLAN_INT*	Interrupt to Intel® PXA27x Processor (sleep-wakeup)

6.2.4 802.11b Power Consumption

- Transmit
  - 350mA @ 2.85V, 100mA @ 1.8V for 19.5 dBm
  - 265mA @ 2.85V, 100mA @ 1.8V for 15 dBm
  - 170mA @ 2.85V, 100mA @ 1.8V for 10 dBm
- Receive
  - < 130 mA @ 1.8V, < 115 mA @ 2.85V
- Idle (doze state as defined in 802.11b specification)
  - 3.3 mA @ 2.85V, 2 mA @ 1.8V, at wake-up interval of 100 msec
  - 1.1 mA @ 2.85V, 0.73 mA @ 1.8V, at wake-up interval of 300 msec
  - 0.37 mA @ 2.85V, 0.29 mA @ 1.8V, at wake-up interval of 1 sec

Figure 24. 802.11b Power Consumption



- Sleep
  - 90 uA @ 1.8V, 25 uA @ 2.85 (see chart below)
- Leakage current (802.11b completely turned off)
  - <10 uA @ 1.8V, <20 uA @ 2.85V

Glossary 7

Term	Definition
ADPCM	Adaptive Digital Pulse Code Modulation
AFE	Analog Front End
APPS	Application Processor
BB	Baseband part of the COMM
BNEP	Bluetooth* Network Encapsulation Protocol
BSP	Board Support Package
BT	Bluetooth*
CCI	Cellular Controller Interface
CCO	Current Controlled Oscillator
CIR	Consumer Infrared
CMOS	Complementary Metal Oxide Semiconductor
COMM	Communication Processor
CS	Chipset
DAC	Digital Analog Converter
DCR	Direct Conversion
DCS	Digital Cellular System
DFC	Dynamic Flow Control (for MSL)
DLL	Data Link Layer
DR	Data Representation Library
DRG	Development RF Group
DSM	Direct Stream Manager
DUN	Dial-Up Network
DVM	Dynamic Voltage Modulation
EGPRS	Enhanced General Packet Radio Service
EL	Electro-Luminescent
ESD	Electrostatic Discharge
FPC	Flexible Printed Circuit
GKI	Generic Kernal Interface
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose IN/OUT
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HCI	Host Control Interface

Term	Definition
HFK	Hands Free Kit
HFP	Hands Free Profile
HSP	Headset Profile
IRC	Interrupt Signal
IrDA	Infrared Data Association
ISP	Internet Service Provider
ISV	Independent Software Vendor
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAC	Multiply and Accumulate
MEMC	Memory Controller
MIDI	Musical Instrument Digital Interface
MSA	Micro Signal Architecture
MSL	Mobile Scalable Link
NAP	Network Access Point
ODM	Original Design Manufacturer
OEM	Original Equipment Manufacturer
OTA	Over the Air
OTG	On-The-Go
PAN	Personal Area Network
PCA	Personal Client Architecture
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCS	Personal Communication Services
PMC	Power Management Chip
PMU	Power Management Unit
PRD	Products Requirement Document
PWM	Pulse Width Modulation
RD	Reference Design
RF	Radio Frequency
RIL	Radio Interface Layer
RPC	Remote Procedure Call
RSSI	Received Signal Strength Indicator
SAC	Service Access Control
SAL	Service Access Layer
SAR	Specific Absorption Rate
SAW	Surface Acoustic Wave

Term	Definition
SDIO	Standard IN/OUT
SIR	Serial Infrared
SIVR	Speaker Independent VR
SM	Service Manager Library
SPI	Serial Peripheral Interface
SPP	Serial Port Profile
SPS	Samples Per Second
SSP	Synchronous Serial Port
TCXO	Temperature Compensated Crystal Oscillator
TS	Time Slot
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VMP	Voice Memo Pad
VOIP	Voice Over IP
VR	Voice Recognition
WCCG	Wireless Communications and Computing Group
WLAN	Wireless Local Area Network
ZIF	Zero Insertion Force