1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O and SRAM (W30)

28F6408W30, 28F3204W30, 28F320W30, 28F640W30

Preliminary Datasheet

Product Features

- **Flash Performance**
  - 70 ns Initial Access Speed
  - 25 ns Page-Mode Read Speed
  - 20 ns Burst-Mode Read Speed
  - Burst and Page Mode in All Blocks and across All Partition Boundaries
  - Enhanced Factory Programming: 3.5 µs per Word Program Time
  - Programmable WAIT Signal Polarity
- **Flash Power**
  - V_{CC} = 1.70 V – 1.90 V
  - V_{CCQ} = 2.20 V – 3.30 V
  - Standby Current = 6 µA (typ.)
  - Read Current = 7 mA (4 word burst, typ.)
- **Flash Software**
  - 5/9 µs (typ.) Program/Erase Suspend Latency Time
  - Intel® Flash Data Integrator (FDI) and Common Flash Interface (CFI) Compatible
- **Quality and Reliability**
  - Operating Temperature: –25 °C to +85 °C
  - 100K Minimum Erase Cycles
  - 0.18 µm ETOX™ VII Process
- **Flash Architecture**
  - Multiple 4-Mbit Partitions
  - Dual Operation: RWW or RWE
  - Parameter Block Size = 4-Kword
  - Main block size = 32-Kword
  - Top and Bottom Parameter Devices
- **Flash Security**
  - 128-bit Protection Register: 64 Unique Device Identifier Bits; 64 User OTP Protection Register Bits
  - Absolute Write Protection with V_{PP} at Ground
  - Program and Erase Lockout during Power Transitions
  - Individual and Instantaneous Block Locking/ Unlocking with Lock-Down
- **SRAM**
  - 70 ns Access Speed
  - 16-bit Data Bus
  - Low Voltage Data Retention
  - S-V_{CC} = 2.20 V – 3.30 V
- **Density and Packaging**
  - 32-Mbit Discrete in VF BGA Package
  - 64-Mbit Discrete in µBGA* Package
  - 56 Active Ball Matrix, 0.75 mm Ball-Pitch in µBGA* and VF BGA Packages
  - 32/4-, 64/8- and 128/TBD- Mbit (Flash + SRAM) in a 80-Ball Stacked-CSP Package (14 mm x 8 mm)
  - 16-bit Data Bus

The 1.8 Volt Intel®Wireless Flash Memory with 3 Volt I/O combines state-of-the-art Intel® Flash technology with low power SRAM to provide the most versatile and compact memory solution for high performance, low power, board constraint memory applications.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O offers a multi-partition, dual-operation flash architecture that enables the device to read from one partition while programming or erasing in another partition. This Read-While-Write or Read-While-Erase capability makes it possible to achieve higher data throughput rates as compared to single partition devices and it allows two processors to interleave code execution because program and erase operations can now occur as background processes.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O incorporates a new Enhanced Factory Programming (EFP) mode to improve 12 V factory programming performance. This new feature helps eliminate manufacturing bottlenecks associated with programming high density flash devices. Compare the EFP program time of 3.5 µs per word to the standard factory program time of 8.0 µs per word and save significant factory programming time for improved factory efficiency.

Additionally, the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O includes block lock-down, programmable WAIT signal polarity and is supported by an array of software tools. All these features make this product a perfect solution for any demanding memory application.

Notice: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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Preliminary

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Revision History

Date of Revision	Version	Description
09/19/00	-001	Original Version
03/14/01	-002	28F3208W30 product references removed (product was discontinued) 28F640W30 product added Revised Table 2, *Signal Descriptions (*$DQ_{15–0}$, ADV#, WAIT, S-UB#, S-LB#, V_{CCQ}) Revised Section 3.1, *Bus Operations* Revised Table 5, *Command Bus Definitions*, Notes 1 and 2 Revised Section 4.2.2, *First Latency Count (*$LC_{2–0}$*);* revised Figure 6, *Data Output with LC Setting at Code 3*; added Figure 7, *First Access Latency Configuration* Revised Section 4.2.3, *WAIT Signal Polarity (WT)* Added Section 4.2.4, *WAIT Signal Function* Revised Section 4.2.5, *Data Output Configuration (DOC)* Added Figure 8, *Data Output Configuration with WAIT Signal Delay* Revised Table 13, *Status Register DWS and PWS Description* Revised entire Section 5.0, *Program and Erase Voltages* Revised entire Section 5.3, *Enhanced Factory Programming (EFP)* Revised entire Section 8.0, *Flash Security Modes* Revised entire Section 9.0, *Flash Protection Register*; added Table 15, *Simultaneous Operations Allowed with the Protection Register* Revised Section 10.1, *Power-Up/Down Characteristics* Revised Section 11.3, *DC Characteristics.* Changed I_{CCS}, I_{CCWS}, I_{CCES} Specs from 18 µA to 21µA; changed I_{CCR} Spec from 12 mA to 15 mA (burst length = 4) Added Figure 20, *WAIT Signal in Synchronous Non-Read Array Operation Waveform* Added Figure 21, *WAIT Signal in Asynchronous Page-Mode Read Operation Waveform* Added Figure 22, *WAIT Signal in Asynchronous Single-Word Read Operation Waveform* Revised Figure 23, *Write Waveform* Revised Section 12.4, *Reset Operations* Clarified Section 13.2, *SRAM Write Operation*, Note 2 Revised Section 14.0, *Ordering Information* Minor text edits

1.0 Product Introduction

1.1 Document Purpose

This document contains information pertaining to the 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O and SRAM. Section 1.0 provides a product introduction. Section 2.0 provides a product description. Section 3.0 describes general device operations. Sections 4.0 through 9.0 describe the flash functionality. Section 10 describes device power and reset considerations. Section 11.0 describes the device electrical specifications. Section 12.0 describes the flash AC characteristics. Section 13.0 describes the SRAM AC characteristics. Section 14.0 describes ordering information.

1.2 Nomenclature

- **Block:** a group of flash bits that share common erase circuitry and erase simultaneously.
- **Partition: Partition** is a group of blocks that share erase and program circuitry and a common status register. If one block is erasing or one word is programming, only the status register, rather than array data, is available when any address within the partition is read.
- **Main Block:** a flash block of 32-Kwords.
- **Parameter Block:** a flash block of 4-Kwords.
- **Main Partition:** a partition that only contains main blocks.
- **Parameter Partition:** a partition that contains both main and parameter blocks.
- **Top/Bottom Parameter Device:** parameter blocks are located at the top/bottom of the flash memory map. A top/bottom parameter partition contains 15 blocks; 7 main blocks and 8 parameter blocks.

2.0 Product Description

2.1 Product Overview

Intel® 1.8 Volt Wireless Flash Memory with 3 Volt I/O and SRAM combines flash and SRAM into one package. The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O divides the flash memory into many separate 4-Mbit partitions. By doing this, the device can perform simultaneous read-while-write or read-while-erase operations. With this new architecture, the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O can read from one partition while programming or erasing in another partition. This read-while-write or read-while-erase capability greatly increases data throughput performance.

Each partition contains eight 32-Kword blocks, called “main blocks.” However, for a top or bottom parameter device, the upper or lower 32-Kword block is segmented into eight, separate 4-Kword blocks, called “parameter blocks.” Parameter blocks are ideally suited for frequently updated variables or boot code storage. Both main and parameter blocks support page and burst mode reads.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O also incorporates a new Enhanced Factory Programming (EFP) mode. In EFP mode, this device provides the fastest NOR flash factory programming time possible at 3.5 µs per data word. This feature can greatly reduce factory flash programming time and thereby increase manufacturing efficiency.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O offers both hardware and software forms of data protection. Software can individually lock and unlock any block for “on-the-fly” run-time data protection. For absolute data protection, all blocks are locked when the V_{PP} voltage falls below the V_{PP} lockout threshold.

Upon initial power up or return from reset, the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O defaults to page mode. To enable burst mode, write and configure the configuration register. While in burst mode, the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O is synchronized with the host CPU. Additionally, a configurable WAIT signal can be used to provide easy flash-to-CPU synchronization.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O maintains compatibility with Intel® Command User Interface (CUI), Common Flash Interface (CFI), and Intel® Flash Data Integrator (FDI) software tools. CUI is used to control the flash device, CFI is used to obtain specific product information, and FDI is used for data management.

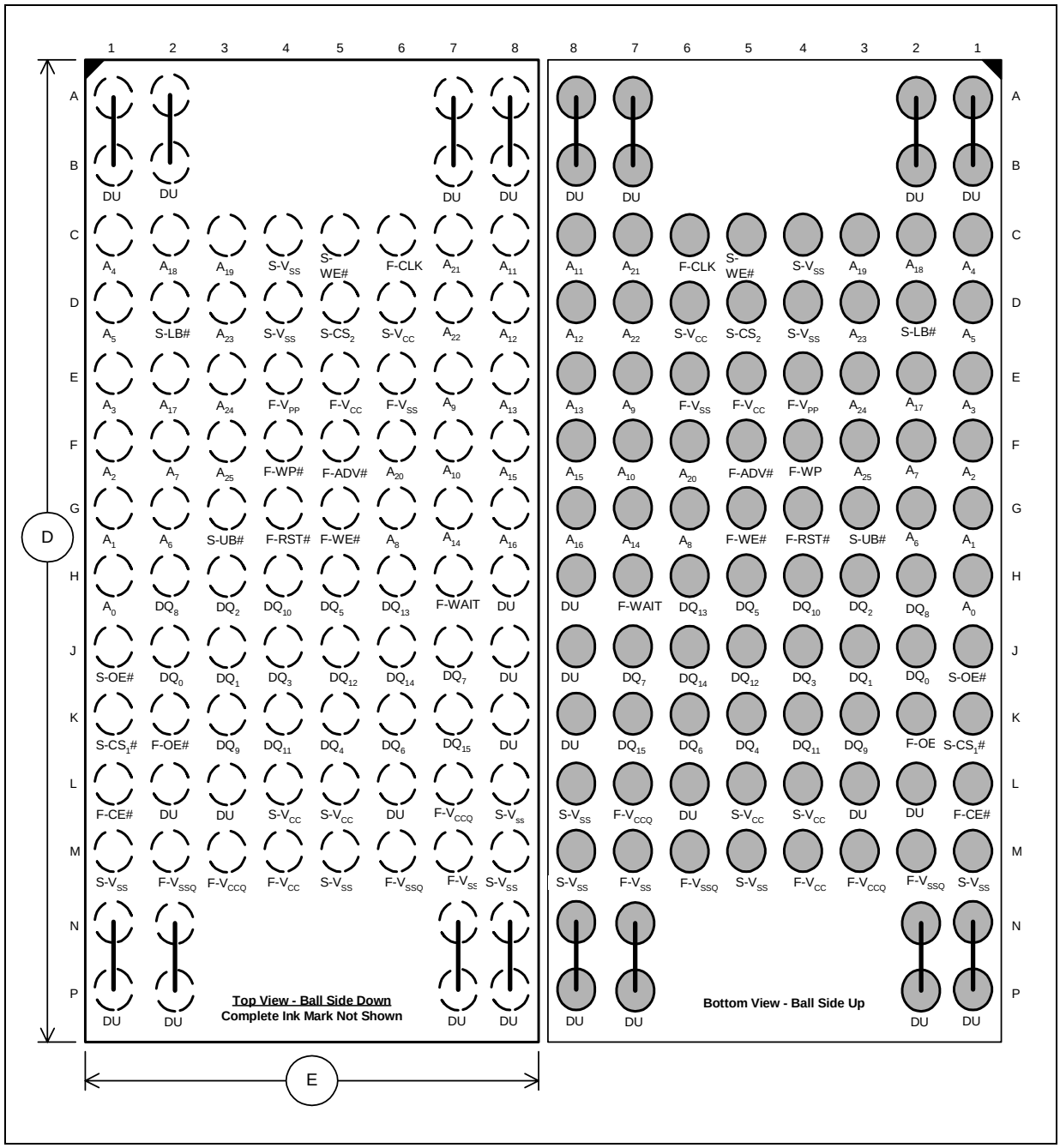
The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O and SRAM offers two low-power savings features: Automatic Power Savings (APS) and standby mode. The flash device automatically enters APS following the completion of any read cycle. Flash and SRAM standby modes are enabled when the appropriate chip select signals are de-asserted.

Finally, the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O provides program and erase suspend/resume operations to allow system software to service higher priority tasks. It offers a 128-bit protection register that can be used for unique device identification and/or system security purposes.

Combined, all these features make the 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O and SRAM an ideal solution for any high-performance, low-power, board-constrained memory application.

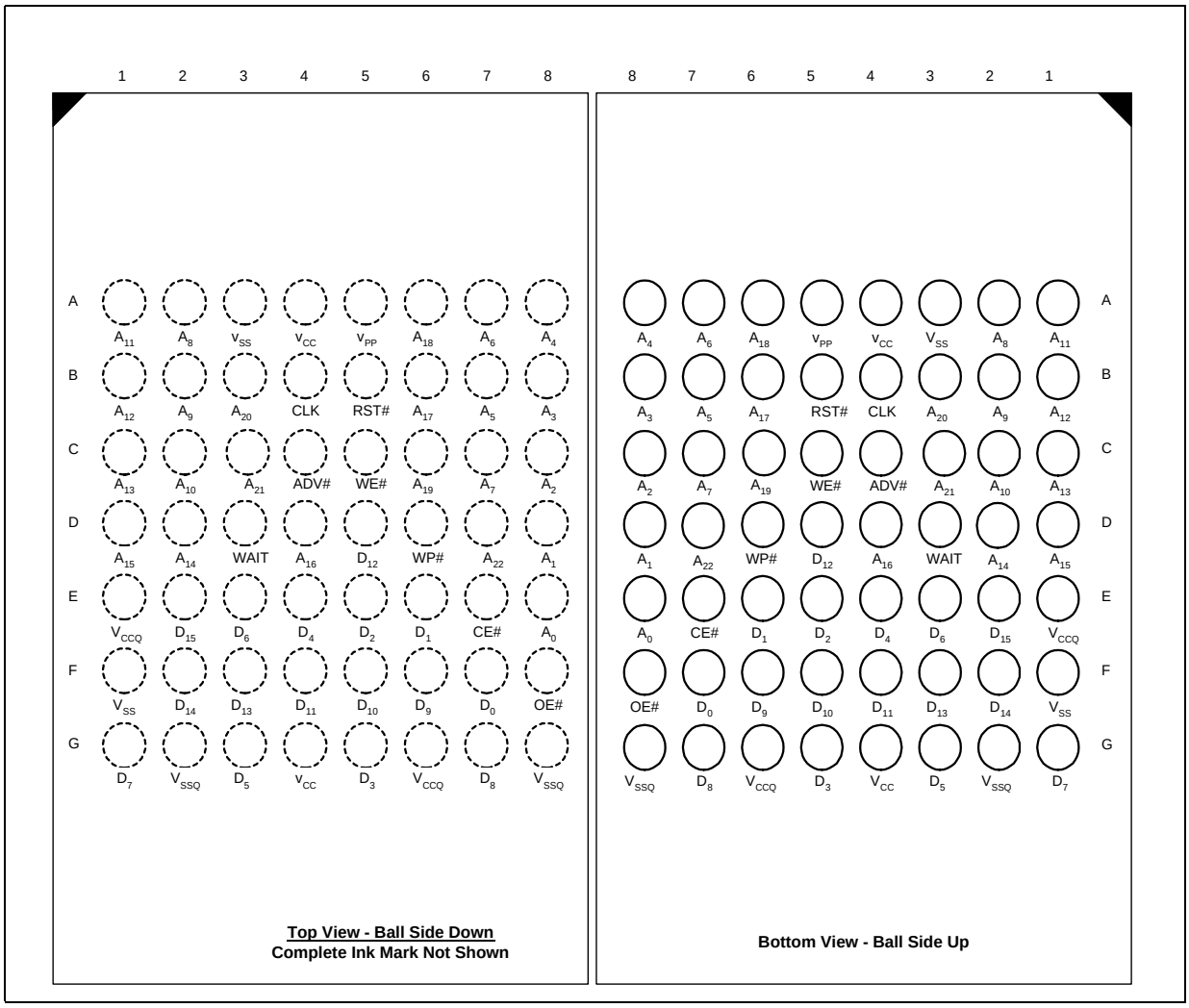
2.2 Package Diagram

Figure 1. 80-Ball Matrix, 0.80 mm Ball Pitch, Stacked-CSP for 32/4-, 64/8- and 128/TBD-Mbit Devices (Flash + SRAM)



NOTES:
1. On lower density devices, upper address balls can be treated as no connects. For example, on a 32-Mbit device, A_{23-21} will be no connects.

Figure 2. 56-Ball Matrix, 0.75 mm Ball Pitch, VF BGA Package and µBGA* Package for the 32-Mbit and 64-Mbit Discrete Devices



NOTE:
1. All balls will be populated; however, addresses A_{21} and A_{22} will be NC.

2.3 Package Dimensions

Table 1. Package Outline Dimensions

Package Type	Device Density	Dimension-D (± 0.1 mm)	Dimension-E (± 0.1 mm)	Height (max.) (mm)
VF BGA	32 Mbit	7.7 mm	9.0 mm	1.0 mm
µBGA*	64 Mbit	7.7 mm	9.0 mm	1.0 mm
Stacked-CSP	32/4, 64/8	14.0 mm	8.0 mm	1.4 mm

2.4 Signal Descriptions

Table 2. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Name and Function
A_{25-0}	I	**ADDRESS:** Device address. Addresses are internally latched during read and write cycles. 32-Mbit flash: A_{20-0}; 64-Mbit flash: A_{21-0}; 128-Mbit flash: A_{22-0}; 4-Mbit SRAM: A_{17-0}; 8-Mbit SRAM: A_{18-0}
DQ_{15-0}	I/O	**DATA INPUT/OUTPUTS:** Inputs data and commands during write cycles, outputs data during query, id reads, memory, status register, protection register, and configuration code reads. Data signals float when the chip or outputs are deselected. Data is internally latched during writes. Query accesses and status register accesses use DQ_0–DQ_7. All other accesses use DQ_0–DQ_{15}.
ADV#	I	**FLASH ADDRESS VALID:** Internally latches addresses. In page mode, addresses are internally latched on the rising edge of ADV#. In burst mode, address internally latched on the rising edge of ADV# or rising/ falling edge of CLK, whichever occurs first. Connect ADV# to GND when the flash device is operating in asynchronous mode only.
CE#	I	**FLASH CHIP ENABLE:** Enables/disables flash device. CE#-low enables the device. CE#-high disables the device and places the device into standby mode. CE# high places data and WAIT signals at a High-Z level.
S-CS_1#	I	**SRAM CHIP SELECT1:** Activates the SRAM internal control logic, input buffers, decoders and sense amplifiers. S-CS_1# is active low. S-CS_1# high deselects the SRAM memory device and reduces power consumption to standby levels.
S-CS_2	I	**SRAM CHIP SELECT2:** Activates the SRAM internal control logic, input buffers, decoders and sense amplifiers. S-CS_2 is active high. S-CS_2 low deselects the SRAM memory device and reduces power consumption to standby levels.
CLK	I	**FLASH CLOCK:** Synchronizes the device to the system bus frequency. (Used only in burst mode.)
OE#	I	**FLASH OUTPUT ENABLE:** Enables/disables device output buffers. OE# low enables the device output buffers. OE# high disables the device output buffers and places all outputs at a High-Z level.
S-OE#	I	**SRAM OUTPUT ENABLE:** Activates the SRAM outputs through the data buffers during a read operation. S-OE# is active low.
RST#	I	**FLASH RESET:** Enables/disables device operation. RST# low initializes internal circuitry and disables device operation. RST# high enables device operation.
WAIT	O	**FLASH WAIT:** Indicates valid data in burst read mode. WAIT is at High-Z until the configuration register bit CR.10 is set, which also determines its polarity when asserted.
WE#	I	**FLASH WRITE ENABLE:** Enables/disables device write buffers. WE# low enables the device write buffers. Data is latched on the rising edge of WE#. WE# high disables the device write buffers.
S-WE#	I	**SRAM WRITE ENABLE:** Controls writes to the SRAM memory array. S-WE# is active low.
S-UB#	I	**SRAM UPPER BYTE ENABLE:** Enables the upper bytes for SRAM (DQ_{15-8}). S-UB# is active low. S-UB# and S-LB# must be tied together to restrict x16 mode.
S-LB#	I	**SRAM LOWER BYTE ENABLE:** Enables the lower bytes for SRAM (DQ_{7-0}). S-LB# is active low. S-UB# and S-LB# must be tied together to restrict x16 mode.
WP#	I	**FLASH WRITE PROTECT:** Enables/disables the device lock-down function. WP# low enables the lock-down mechanism and blocks marked lock-down cannot be unlocked by system software. WP# high disables the lock-down mechanism and blocks marked lock-down can be unlocked by system software.
V_{PP}	Pwr	**FLASH PROGRAM/ERASE POWER:** Hardware erase and program protection. A valid V_{PP} voltage on this ball allows erase or programming. Memory contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{CC}$ for in-system read, program, and erase operations. V_{PP} must remain above V_{PP1}Min to perform in-system operations. V_{PP2} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be V_{PP2} for a cumulative total, not to exceed 80 hours maximum. Extended use of this ball at V_{PP2} may reduce block cycling capability.
V_{CC}	Pwr	**FLASH POWER SUPPLY:** Flash operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Pwr	**FLASH OUTPUT POWER SUPPLY:** Enables all input and output signals to be driven at V_{CCQ}.

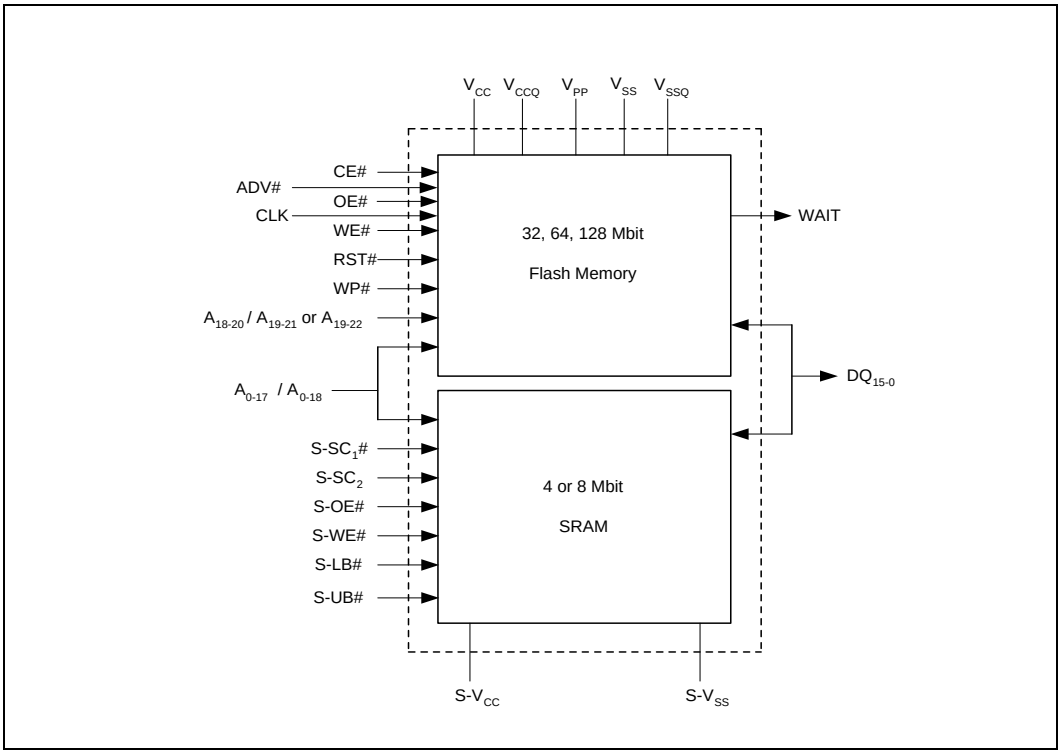
Table 2. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Name and Function
V_{SS}	Pwr	**FLASH POWER SUPPLY GROUND:** Balls for internal device circuitry must be connected to system ground.
V_{SSQ}	Pwr	**FLASH OUTPUT POWER SUPPLY GROUND:** Balls for internal device circuitry must be connected to system ground.
S-V_{CC}	Pwr	**SRAM POWER SUPPLY:** Device operations at invalid S-V_{CC} voltages should not be attempted.
S-V_{SS}	Pwr	**SRAM GROUND:** Balls for all internal device circuitry must be connected to system ground.
DU		**DON'T USE:** Do not use this ball. This ball should not be connected to any power supplies, control signals and/or any other ball and must be floated.
NC		**NO CONNECT:** No internal connection. Can be driven or floated.

NOTE: For non-discrete devices, all flash signals are prefixed with F_ before its signal's name.

2.5 Block Diagram

Figure 3. 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O and SLRAM Block Diagram



2.6 Flash Memory Map

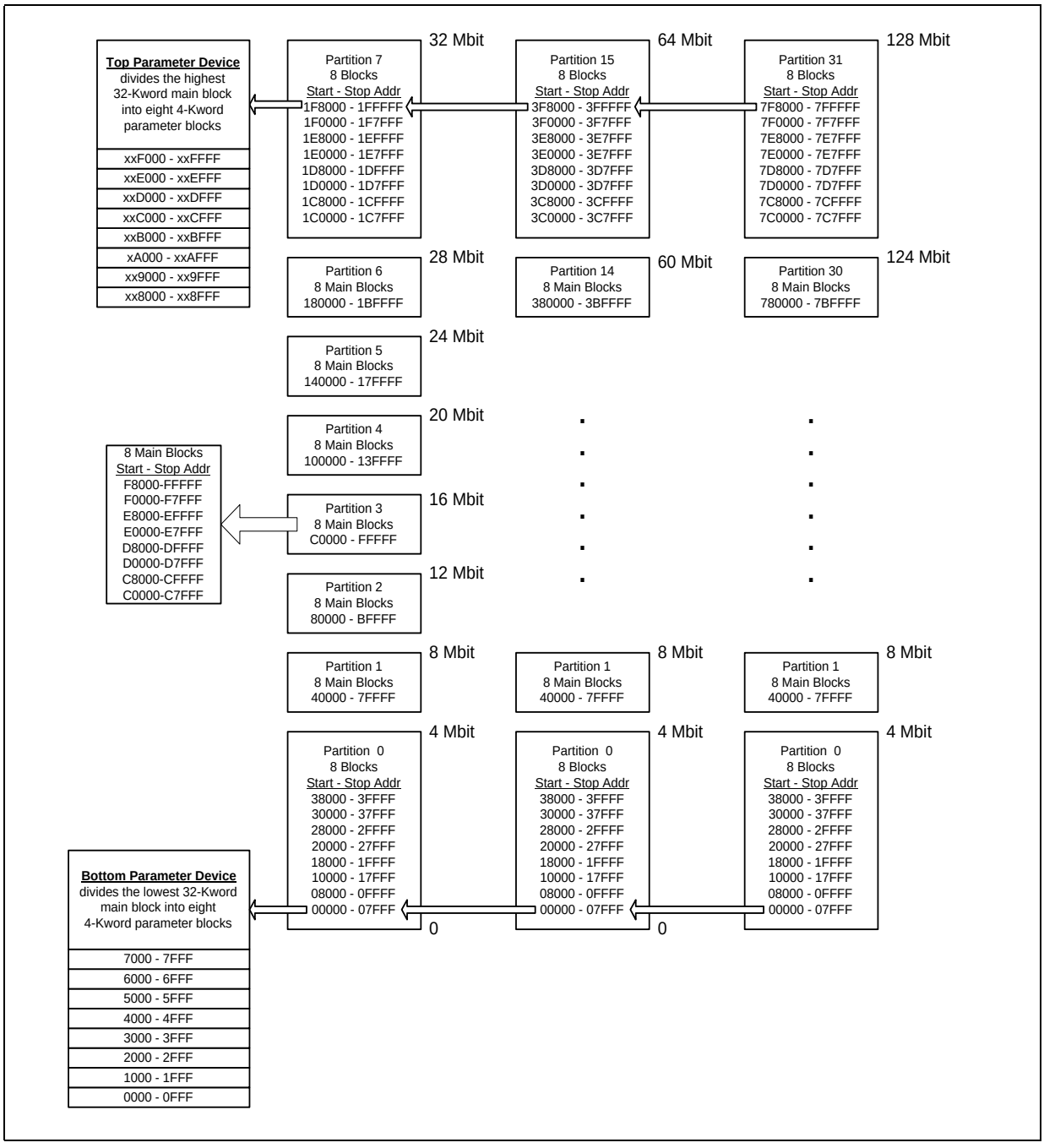
The 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O memory is divided into separate partitions to support the read-while-write/erase function. Each partition is 4-Mbits in size and can operate independently from other partitions.

A 32-Mbit device will have eight partitions; a 64-Mbit device will have 16 partitions; a 128-Mbit device will have 32 partitions. Each main block is 32-Kword in size.

The 1.8 Volt Intel Wireless Flash Memory with 3 Volt I/O supports CPUs that boot from either the top or bottom of the flash memory map. A top parameter flash device has the highest addressable 32-Kword block divided into eight smaller blocks. Conversely, a bottom parameter flash device has the lowest addressable 32-Kword block divided into eight smaller blocks. Each of these eight 4-Kword blocks are called parameter blocks. Parameter blocks are useful for frequently stored data variables. Their smaller block size allows them to erase faster than main blocks. Page- and burst-mode reads are also permitted in all blocks and across all partition boundaries.

It should be mentioned that the SRAM does not adhere to this multi-partition architecture. The SRAM memory is organized as a single memory array.

Figure 4. Flash Memory Map



NOTES:

1. Partition size: 4 Mbit/256 Kword/512 Kbytes.
2. Main block size: 32 Kword/64 Kbytes.
3. Parameter block size: 4 Kword/8 Kbytes.
4. All partitions have 8 main blocks, except for top/bottom parameter partitions.
5. Top/bottom parameter partitions have 15 blocks, 7 main and 8 parameter.

3.0 Product Operations

3.1 Bus Operations

The 1.8 Volt Intel® Wireless Flash Memory's on-chip Write State Machine (WSM) manages erase and program algorithms. The local CPU controls the in-system read, program, and erase operations of the flash device. Bus cycles to and from the flash device conform to standard microprocessor bus operations. RST#, CE#, OE#, WE#, and ADV# signals control the flash. WAIT informs the CPU of valid data during burst reads. S-OE#, S-WE#, S-CS_1#, S-CS_2, S-LB# and S-UB# control the SRAM. S-UB# and S-LB# must be tied together to restrict x16 mode. Table 3 summarizes bus operations.

Table 3. Bus Operations

	Mode	Note	RST#	CE#	OE#	WE#	ADV#	WAIT	S-CS_1#	S-CS_2	S-OE#	S-WE#	S-UB# S-LB#[7]	DQ [15:0]
FLASH	Read	1,2, 5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Valid	SRAM must be in High-Z					D_{OUT}
	Output Disable	3	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	Any Valid SRAM Mode					High-Z
	Standby	3	V_{IH}	V_{IH}	X	X	X	High-Z						High-Z
	Reset	3	V_{IL}	X	X	X	X	High-Z						High-Z
	Write	4, 5	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	SRAM must be in High Z					D_{IN}
SRAM	Read	5	Flash must be in High-Z					High-Z	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{OUT}
	Output Disable	3	Any Valid FLASH Mode						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
	Standby and Data Retention	3, 6							V_{IH}	X	X	X	X	High-Z
									X	V_{IL}	X	X	X	High-Z
	Write	5	Flash must be in High-Z					High-Z	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	D_{IN}

NOTES:
1. Manufacturer and device ID codes are accessed by Read ID Register command.
2. Query and status register accesses use only DQ_{7-0}. All other accesses use DQ_{15-0}.
3. X must be V_{IL} or V_{IH} for control signals and addresses.
4. Refer to Table 5, "Command Bus Definitions" on page 11 for valid D_{IN} during a write operation.
5. Two devices may not drive the memory bus at the same time.
6. The SRAM can be placed into data retention mode by lowering the S-V_{CC} to the V_{DR} limit when in standby mode.
7. Always tie S-UB# and S-LB# together.

3.2 Flash Command Definitions

Device operations are selected by writing specific commands to the Command User Interface (CUI). Table 4, "Command Code and Descriptions" on page 10 lists all possible command codes and descriptions. Table 5, "Command Bus Definitions" on page 11 further defines command bus cycle operations. Since commands are partition-specific, it is important to write commands within the target partition range.

Multi-cycle command writes to the flash memory partition must be issued sequentially without intervening command writes. For example, an Erase Setup command to partition X must be immediately followed by the Erase Confirm command in order to be executed properly. The address given during the Erase Confirm command determines the location of the erase. If the Erase

Confirm command is given to partition X, then the command will be executed, and a block in partition X will be erased. Alternatively, if the Erase Confirm command is given to partition Y, the command will still be executed, and a block in partition Y will be erased. Any other command given to ANY partition prior to the Erase Confirm command will result in a command sequence error, which is posted in the status register. After the erase has successfully started in partition X or Y, read cycles can occur in any other partition.

Table 4. Command Code and Descriptions (Sheet 1 of 2)

Mode	Instruction Code	Command	Description
Read	FFh	Read Array	Places addressed partition in read array mode.
	70h	Read Status Register	Places addressed partition in read status register mode. A partition automatically enters the read status register mode after a valid Program/Erase command is executed.
	90h	Read ID Register, Read Configuration Register	Puts the addressed partition in read device identifier mode. The device outputs manufacturer and device ID codes, configuration register settings, block lock status and protection register data. Data is output on DQ_{15-0}.
	98h	Read Query Register	Puts the addressed partition in read query mode. The device outputs Common Flash Interface (CFI) information on DQ_{7-0}.
	50h	Clear Status Register	Clears status register bits 1, 3, 4 and 5. The WSM can set (1) and reset (0) bits 0, 2, 6 and 7.
Program	40h	Word Program Setup	The preferred first bus cycle program command that prepares the WSM for a program operation. The second bus cycle command latches the address and data. A Read Array command is required to read array data after programming.
	10h	Alternate Word Program Setup	Equivalent to a Word Program Setup command (40h).
	30h	Enhanced Factory Programming Setup	Activates Enhanced Factory Programming mode (EFP). The first bus cycle sets up the command. If the second bus cycle is a Confirm command (D0h), subsequent writes provide program data. All other commands are ignored once EFP mode begins.
	D0h	Enhanced Factory Programming Confirm	If the first command was Enhanced Factory Programming Setup (30h), the CUI latches the address, confirms command data, and prepares the device for EFP mode.
Erase	20h	Block Erase Setup	Prepares the WSM for a block erase operation. The device erases the block addressed by the Erase Confirm command. If the next command is not Erase Confirm, the CUI (a) sets status register bits SR.4 and SR.5 to “1,” (b) places the partition in the read status register mode (c) waits for another command.
	D0h	Erase Confirm	If the first command was Erase Setup (20h), the WSM latches address and data and erases the block indicated by the erase confirm cycle address. During program/erase, the partition responds only to Read Status Register, Program Suspend, and Erase Suspend commands. CE# or OE# toggle updates status register data.
Suspend	B0h	Program or Erase Suspend	This command issued at any device address initiates suspension of the currently executing program/erase operation. The status register, invoked by a Read Status Register command, indicates successful operation suspension by setting (1) status bits SR.2 (program suspend) or SR.6 (erase suspend) and SR.7. The WSM remains in the suspend mode regardless of control signal states, except RST# = V_{IL}.
	D0h	Suspend Resume	This command issued at any device address resumes suspended program or erase operation.
Block Locking	60h	Lock Setup	Prepares the WSM lock configuration. If the next command is not Block-Lock, Unlock, or Lock-Down the WSM sets SR.4 and SR.5 to indicate command sequence error.
	01h	Lock Block	If the previous command was Lock Setup (60h), the CUI locks the addressed block.
	D0h	Unlock Block	After a Lock Setup (60h) command the CUI latches the address and unlocks the addressed block. If previously Locked-down, the operation has no effect.
	2Fh	Lock-Down	After a Lock Setup (60h) command, the CUI latches the address and locks-down the addressed block.

Table 4. Command Code and Descriptions (Sheet 2 of 2)

Mode	Instruction Code	Command	Description
Protection	C0h	Protection Program Setup	Prepares the WSM for a protection register program operation. The second bus cycle latches address and data. To read array data after programming, issue a Read Array command.
Configuration	60h	Configuration Setup	Prepares the WSM for device configuration. If Set Configuration Register is not the next command, the WSM sets SR.4 and SR.5 to indicate command sequence error.
	03h	Set Configuration Register	If the previous command was Configuration Setup (60h), the WSM writes data into the configuration register via A_{15-0}. Following a Set Configuration Register command, subsequent read operations access array data.

NOTE: Unassigned instruction codes should not be used. Intel reserves the right to redefine these codes for future functions.

Table 5. Command Bus Definitions

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr(1)	Data(2,3)	Oper	Addr(1)	Data(2,3)
READ	Read Array	1	Write	PnA	FFh			
	Read ID Register	2	Write	XnA	90h	Read	XnA+IA	IC
	Read Query Register	2	Write	PnA	98h	Read	PnA+QA	QD
	Read Status Register	2	Write	PnA	70h	Read	BA	SRD
	Clear Status Register	1	Write	XX	50h			
PROGRAM ERASE	Block Erase	2	Write	BA	20h	Write	BA	D0h
	Word Program	2	Write	WA	40h/10h	Write	WA	WD
	Enhanced Factory Program	≥2	Write	WA	30h	Write	WA	D0h
	Program/Erase Suspend	1	Write	XX	B0h			
	Program/Erase Resume	1	Write	XX	D0h			
LOCK	Lock Block	2	Write	BA	60h	Write	BA	01h
	Unlock Block	2	Write	BA	60h	Write	BA	D0h
	Lock-Down Block	2	Write	BA	60h	Write	BA	2Fh
PROTEC-TION	Protection Program	2	Write	PA	C0h	Write	PA	PD
	Lock Protection Program	2	Write	LPA	C0h	Write	LPA	FFFDh
CONFIG-URATION	Set Configuration Register	2	Write	CD	60h	Write	CD	03h

NOTES:
1. First cycle command addresses should be the same as the operation's target address. Examples: the first-cycle address for the Read ID Register command should be the same as the Identification Code address (IA); the first cycle address for the Program command should be the same as the word address (WA) to be programmed; the first cycle address for the Erase/Program Suspend command should be the same as the address within the block to be suspended; etc.
   XX = Any valid address within the device.
   IA = Identification code address.
   BA = Address within the block.
   LPA = Lock Protection Address is obtained from the CFI (via the Read Query command). Intel®1.8 Volt

Wireless Flash Memory Flash Memory family's LPA is at 0080h.
PA = User programmable 4-word protection address in the device identification plane.
PnA = Address within the partition.
XnA = Base Address where X can be partition, main block or parameter block. See Figure 11, "Device Identification Codes" on page 21 for details.
QA = Query code address.
WA = Word address of memory location to be written.

2. SRD = Data read from the status register on DQ_{7-0}.
   WD = Data to be written at location WA.
   IC = Identifier code data.
   PD =User programmable 4-word protection data.
   QD = Query code data on DQ_{7-0}.
   CD = Configuration register code data presented on device addresses A_{15-0}. A_{MAX-16} address bits can select any partition. See Table 6, "Configuration Register Bits" on page 13 for configuration register bits descriptions.
3. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

4.0 Flash Read Modes

4.1 Read Array

4.1.1 Asynchronous Mode

The 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O supports asynchronous reads. An asynchronous read is executed by implementing a read operation without the use of the CLK signal. During an asynchronous read operation, the CLK signal is ignored. If asynchronous reads will be the only read mode of operation, it is recommended that the CLK signal be held at a valid V_{IH} level.

Page mode is the default read mode after power-up or reset. A page-mode read outputs 4 words of asynchronous data; however, by manipulating certain control signals, the device can be made to output less than 4 words.

After power-up or reset, it is not necessary to execute the Read Array command before accessing the flash memory. However, to perform a flash read at any other time, it is necessary to execute the Read Array command before accessing the flash memory.

Page mode is permitted in all blocks, across all partition boundaries and operates independent of V_{PP}. A single-word read can be used to access register information. During asynchronous reads, the address is latched on the rising edge of ADV#.

Upon completion of reading the array, the device automatically enters an Automatic Power Savings (APS) mode. APS mode consumes power comparable to standby mode.

4.1.2 Synchronous Mode

The 1.8 Volt Intel® Wireless Flash Memory supports synchronous reads. A synchronous read is executed by implementing a read operation with the use of the CLK signal. During a synchronous read operation, the CLK signal edge (rising or falling) controls flash array access.

A burst-mode read is synchronized to the CLK signal and outputs a 4-, 8- or continuous-word data stream based on configuration register settings. However, by manipulating certain control signals, the device can be made to output less then 4-, 8- or continuous-words.

Burst mode is **not** the default mode after power-up or a device reset. To perform a burst-mode read, the configuration register must be set. To set the configuration register, refer to Section 4.2, "Set Configuration Register (CR)" on page 13. After setting the configuration register, if the first device operation is a burst-mode read, it is not necessary to execute the Read Array command before accessing the flash memory. However, to perform a flash read at any other time, it is necessary to execute the Read Array command before accessing the flash memory array.

Burst mode is permitted in all blocks, across all partition boundaries and operates independently of V_{PP}. A single-word burst-mode read **cannot** be used to access register information. In burst mode, the address is latched by either the rising edge of ADV# or the rising edge of CLK with ADV# low, whichever occurs first.

Upon completion of reading the array, the device automatically enters an Automatic Power Savings (APS) mode. APS mode consumes power comparable to standby mode.

4.2 Set Configuration Register (CR)

The configuration register is 16 bits wide. This register is used to configure the burst mode parameters. Therefore, if using page mode, it is not necessary to set this register.

To set the configuration register, execute the Set Configuration Register command. The 16 bits of data used by this command must be placed on address lines $A_{15–0}$. All other address lines must be held low (V_{IL}).

After setting the configuration register, if the first device operation is a flash burst-mode read, it is not necessary to execute the Read Array command before accessing the flash memory. However, to perform a burst-mode read at any other time, it is necessary to execute the Read Array command before accessing the flash memory.

Table 6. Configuration Register Bits

Configuration Register Bits[2]															
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RM	R^1	LC_{2-0}			WT	DOC	WC	BS	CC	R^1	R^1	BW	BL_{2-0}		
	0									0	0				

NOTES:
1. 'R' bits are reserved bits. These bits and all other address lines must be set low.
2. On power-up or return from reset, all bits are set to "1."

Table 7. Configuration Register Bit Settings

Bit Name	Setting
Read Mode (RM) CR.15	0 = Burst or synchronous mode. 1 = Page or asynchronous mode.
First Latency Count (LC_{2-0}) CR.13 – CR.11	Code 0 = 000. Reserved. Code 1 = 001. Reserved. Code 2 = 010. Code 3 = 011. Code 4 = 100. Code 5 = 101. Code 6 = 110. Reserved. Code 7 = 111. Reserved.
WAIT Polarity (WT) CR.10	0 = active low signal. 1 = active high signal
Data Output Configuration (DOC) CR.9	0 = hold data for one clock cycle. 1 = hold data for two clock cycles.
WAIT Configuration (WC) CR.8	0 = WAIT signal asserted during 16-word row boundary transition. 1 = WAIT signal assert one data cycle before 16-word row boundary transition.
Burst Sequence (BS) CR.7	0 = Intel burst sequence. 1 = linear burst sequence.
Clock Configuration (CC) CR.6	0 = falling edge of clock. 1 = rising edge of clock.
Burst Wrap (BW) CR.3	0 = Wrap enabled. 1 = Wrap disabled.
Burst Length (BL_{2-0}) CR.2 – CR.0	001 = 4 Word burst mode. 010 = 8 Word burst mode. 011 = Reserved. 111 = Continuous burst mode.

4.2.1 Read Mode (RM)

CR.15 sets the flash read mode. The two read modes are page mode (default mode) and burst mode. The flash device can only be configured for one of these modes at any one time.

4.2.2 First Latency Count (LC_{2-0})

The First Access Latency Count configuration tells the device how many clocks must elapse from ADV#-high (V_{IH}) before the first data word should be driven onto its data pins. The input clock frequency determines this value. See Table 6, “Configuration Register Bits” on page 13 for latency values. Figure 7, “First Access Latency Configuration” on page 16 shows data output latency from ADV#-active for different latencies.

Use these equations to calculate First Access Latency Count:

$$\{1/\text{ Frequency}\} = \text{CLK Period} \quad (1)$$

$$n\ (\text{CLK Period}) \geq t_{AVQV}\ (\text{ns}) + t_{ADD\text{-}DELAY}\ (\text{ns}) + t_{DATA}\ (\text{ns}) \quad (2)$$

$$n\text{-}2 = \text{First Access Latency Count (LC)}\ * \quad (3)$$

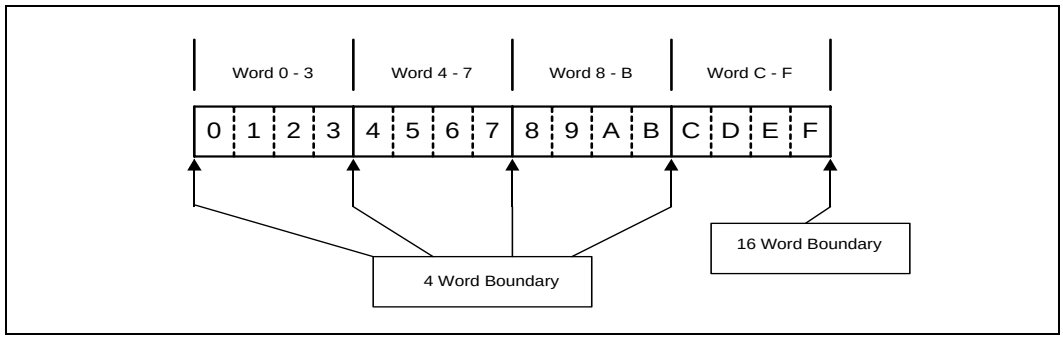
n: # of Clock periods (rounded up to the next integer)

*Must use LC = n - 1 when the starting address is **not** aligned to a four-word boundary and CR.3 = 1 (No Wrap).

Table 8. First Latency Count (LC)

LC Setting	Mode	Wrap	Aligned to 4-word Boundary	Wait Asserted on 16-Word Boundary Crossing
n-1	4 or 8	disabled	no	yes, occurs on every occurrence
n-2	4 or 8	disabled	yes	no
n-2	4 or 8	enabled	no	no
n-2	4 or 8	enabled	yes	no
n-1	continuous	X	X	yes, occurs once

Figure 5. Word Boundary



NOTE:
1. The 16-word boundary is the end of device word-line.

Parameters defined by CPU:

$t_{ADD-DELAY}$ = Clock to CE#, ADV#, or Address Valid whichever occurs last.
t_{DATA} = Data set up to Clock.

Parameters defined by flash:

t_{AVQV} = Address to Output Delay.

Example:

CPU Clock Speed = 52 MHz
$t_{ADD-DELAY}$ = 6 ns (typical speed from CPU) (max)
t_{DATA} = 4 ns (typical speed from CPU) (min)
t_{AVQV} = 70 ns (from AC Characteristic - Read Only Operations Table)
From Eq. (1): 1/52 (MHz) = 19.2 ns
From Eq. (2) $n(19.2\text{ ns}) \geq 70\text{ ns} + 6\text{ ns} + 4\text{ ns}$
$n(19.2\text{ ns}) \geq 80\text{ ns}$
$n \geq 80/19.2 = 4.17 = 5$ (Integer)
From Eq. (3) $n - 2 = 5 - 2 = 3$
First Access Latency Count Setting to the CR is Code 3.
(Figure 6, “Data Output with LC Setting at Code 3” on page 16 displays example data)

The formula t_{AVQV} (ns) + $t_{ADD-DELAY}$ (ns) + t_{DATA} (ns) is also known as initial access time.

Figure 6 shows the data output available and valid after four clocks from ADV# going low in the first clock period with the LC setting at 3.

Figure 6. Data Output with LC Setting at Code 3

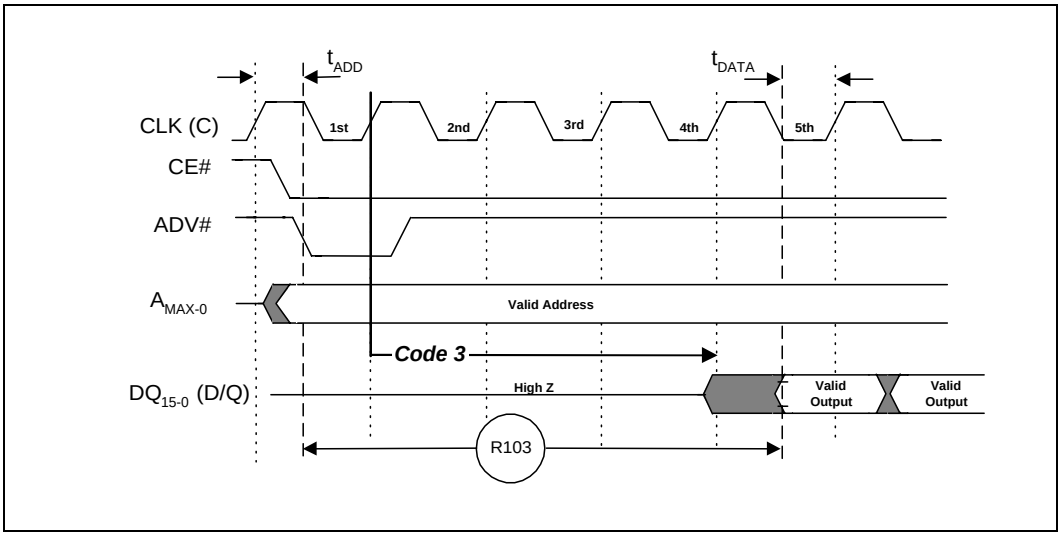
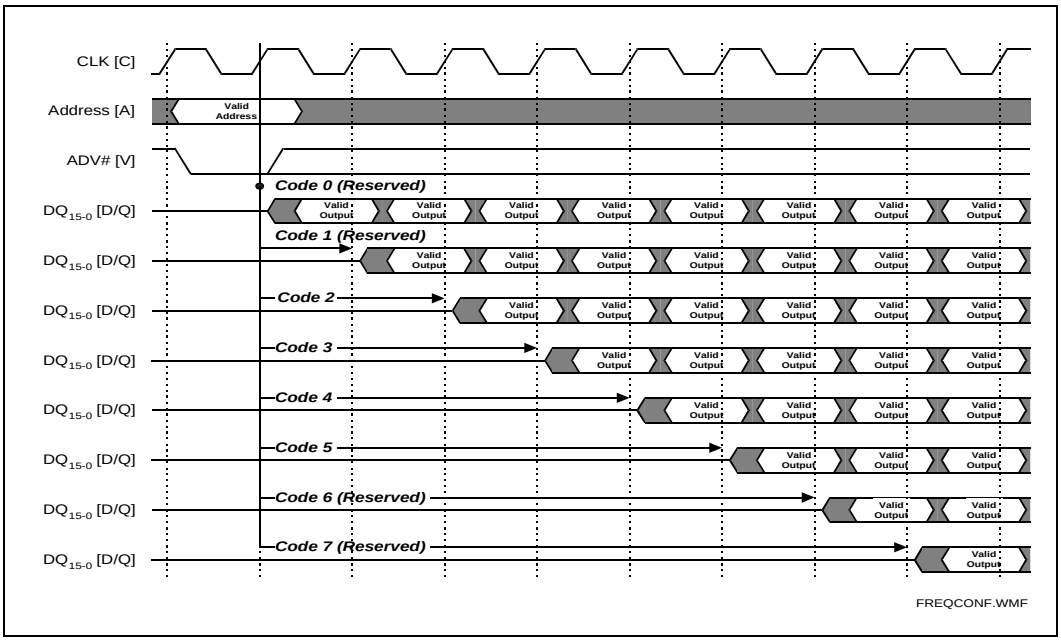


Figure 7. First Access Latency Configuration



4.2.3 WAIT Signal Polarity (WT)

The WAIT signal polarity is set by register bit CR.10 (WT).

- When CR.10 = 0, WAIT is active low. A ‘0’ on the WAIT signal indicates the “asserted” state.

- When CR.10 = 1, WAIT is active high. A ‘1’ on the WAIT signal indicates the “asserted” state.
- WAIT signal “asserted” means that the WAIT signal is indicating a “wait” condition.
- WAIT signal “deasserted” means that the WAIT signal is NOT indicating a “wait” condition (i.e., the bus is valid).

WAIT is High-Z until the device is active (CE# = V_{IL}). In synchronous read array mode, when the device is active (CE# = V_{IL}) and data is valid, CR.10 (WT) determines if WAIT goes to V_{OH} or $V_{OL.}$ The WAIT signal is only “deasserted” when data is valid on the bus. Invalid data drives the WAIT signal to “asserted” state. In asynchronous page mode, WAIT is always set to an “asserted” state (CR.10 = 1)

4.2.4 WAIT Signal Function

The WAIT signal indicates data valid when the device is operating in synchronous burst mode (CR.15 is set to “0”), and when addressing a partition that is currently in read array mode. The WAIT signal is only “deasserted” when data is valid on the bus. The WAIT signal polarity is set by CR.10.

When the device is operating in synchronous non-read-array mode, such as read status, read ID, or read query, WAIT is set to an “asserted” state as determined by CR.10. Figure 20 on page 46 displays WAIT Signal in Synchronous Non-Read Array Operation Waveform.

When the device is operating in asynchronous page mode or asynchronous single word read mode, WAIT is set to an “asserted” state as determined by CR.10. See Figure 21, “WAIT Signal in Asynchronous Page-Mode Read Operation Waveform” on page 47 and Figure 22, “WAIT Signal in Asynchronous Single-Word Read Operation Waveform” on page 48.

From a system perspective, the WAIT signal will be in the asserted state (based on CR.10) when the device is operating in synchronous non-read array mode (such as Read ID, Read Query, or Read Status), or if the device is operating in asynchronous mode (CR.15 is set to “1”). In these cases, the system software should ignore (mask) the WAIT signal, as it does not convey any useful information about the validity of what is appearing on the data bus.

Systems may tie several components’ WAIT signals together.

4.2.5 Data Output Configuration (DOC)

The Data Output Configuration bit (CR.9) determines whether a data word remains valid on the data bus for one or two clock cycles. The processor’s minimum data set-up time and the flash memory’s clock-to-data output delay determine whether one or two clocks are needed.

If the Data Output Configuration is set at one-clock data hold, this corresponds to a one-clock data cycle; if the Data Output Configuration is set at two-clock data hold, this corresponds to a two-clock data cycle. This configuration bit’s setting depends on the system and CPU characteristics. Refer to Figure 8, “Data Output Configuration with WAIT Signal Delay” on page 18 for clarification.

A method for determining what this configuration should be set at is shown below:

To set the device at one clock data hold for subsequent reads, the following condition must be satisfied:

$$t_{CHQV}\ (ns) + t_{DATA}\ (ns) \leq \text{One CLK Period (ns)}$$

As an example, a clock frequency of 52 MHz will be used. The clock period is 19.2 ns. This data is applied to the formula above for the subsequent reads assuming the data output hold time is one clock:

$$14\ ns + 4\ ns \leq 19.2\ ns$$

This equation is satisfied and data output will be available and valid at every clock period.

If t_{DATA} is long, hold for two cycles.

Now assume the clock frequency is 66 MHz. This corresponds to a 15 ns period. The initial access time is calculated to be 80 ns (LC 4). This condition satisfies t_{AVQV} (ns) + $t_{ADD\text{-}DELAY}$ (ns) + t_{DATA} (ns) = 70 ns + 6 ns + 4 ns = 80 ns, as shown above in the First Access Latency Count equations. However, the data output hold time of one clock violates the one-clock data hold condition:

$$t_{CHQV}\ (ns) + t_{DATA}\ (ns) \leq \text{One CLK Period}$$

14 ns + 4 ns = 18 ns is not less than one clock period of 15 ns. To satisfy the formula above, the data output hold time must be set at 2 clocks to correctly allow for data output setup time. This formula is also satisfied if the CPU has t_{DATA} (ns) ≤ 1 ns, which yields:

$$14\ ns + 1\ ns \leq 15\ ns$$

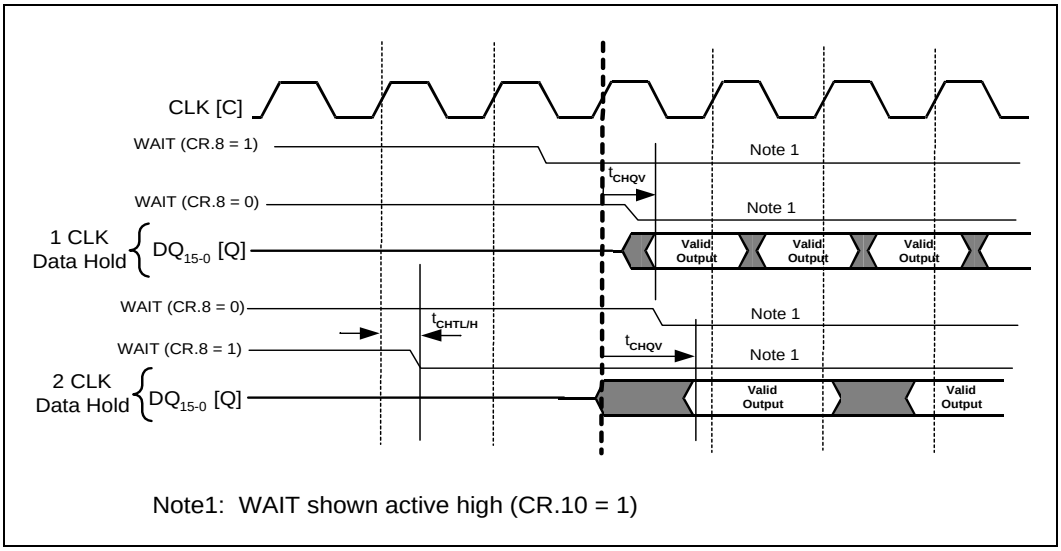
In page mode reads, the initial access time can be determined by the formula:

$$t_{ADD\text{-}DELAY}\ (ns) + t_{DATA}\ (ns) + t_{AVQV}\ (ns)$$

and subsequent reads in page mode are defined by:

$$t_{APA}\ (ns) + t_{DATA}\ (ns) \qquad \text{(minimum time)}$$

Figure 8. Data Output Configuration with WAIT Signal Delay



Note1: WAIT shown active high (CR.10 = 1)

4.2.6 WAIT Configuration (WC)

CR.8 sets the WAIT signal delay. The WAIT signal delay determines when the WAIT signal is asserted. The WAIT signal can be asserted either one clock before or at the time of the misaligned 16-word boundary crossing. An asserted WAIT signal indicates invalid data on the data bus.

In synchronous mode, WAIT is active when CE# is asserted. The WAIT signal is asserted if a burst-mode read is misaligned to a 4-word boundary. By misaligned, we imply that the address must be on a mod-4 boundary; such as xx00h, xx04h, xx08h or xx0Ch. If the address is aligned to a 4-word boundary, the “delay” will never be seen. Also, a “delay” will only occur once per burst-mode read sequence. When a misaligned burst-mode read crosses a 16-word boundary, the device must deselect one row in order to select the next row. It is this selecting/de-selecting (or energizing/de-energizing) of memory rows that causes the device to “delay” output data. It is the assertion of the WAIT signal that informs the interfacing processor of this pending flash “delay.” During the “delay,” subsequent data reads are prohibited.

The WAIT signal is asserted depending on the burst starting address and latency count. If the starting address is aligned to the 4-word boundary, a delay will not occur. If the starting address is aligned to the end of a 4-word boundary, a delay equal to one clock cycle less than the latency count will occur (worst case scenario). See Table 9, “WAIT Delay” on page 19. If the starting address falls between, the delay will be dependent upon the latency count value and the starting address as indicated in Table 9.

In 4- and 8-word burst modes with burst wrap enabled, the device will not assert the WAIT signal. However, with the burst wrap disabled, the flash device will assert the WAIT signal if a burst-mode read is misaligned and crosses a 16-word boundary. With wrap disabled, the burst mode will read 4 or 8 consecutive words based on the initial address. If the initial address is aligned on a mod-4 boundary, the WAIT signal will not be asserted. However, if the initial address is misaligned on a mod-4 boundary and crosses the 16-word boundary limit, the WAIT signal will be asserted.

In continuous-word burst mode, the burst wrap feature does not apply and the WAIT signal is only asserted on the first 16-word boundary crossing. The WAIT signal is inactive or at a High-Z state when accessing register information.

Table 9. WAIT Delay

Starting Burst Address	WAIT Delay in Clock Cycles After Crossing 16-Word Boundary	4-Word Boundary
xx0h, xx4h, xx8h, xxCh	No Delay	Start of Boundary
xx1h, xx5h, xx9h, xxDh	LC - 3	
xx2h, xx6h, xxAh, xxEh	LC - 2	
xx3h, xx7h, xxBh, xxFh	LC - 1	End of Boundary

4.2.7 Burst Sequence (BS)

CR.7 sets the burst sequence. The burst sequence determines the 4- or 8-word output order. In 4- or 8-word burst modes, the burst sequence is defined as either linear or Intel. In continuous burst mode, the burst sequence is always linear. The burst sequence depends on the interfacing processor’s characteristics.

Table 10. Sequence and Burst Length

Start Addr (Decimal)	Wrap (CR.3)	Burst Addressing Sequence (Decimal)				
		4-Word Burst Length (CR_{2-0} = 001)		8-Word Burst Length (CR_{2-0} = 010)		Continuous Burst (CR_{2-0} = 111)
		Linear	Intel	Linear	Intel	Linear
0	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-...
1	0	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-...
2	0	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-...
3	0	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-...
4	0			4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-...
5	0			5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-...
6	0			6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-...
7	0			7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-...
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	0					14-15-16-17-18-19-20-...
15	0					15-16-17-18-19-20-21-...
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	NA	0-1-2-3-4-5-6-7	NA	0-1-2-3-4-5-6-...
1	1	1-2-3-4	NA	1-2-3-4-5-6-7-8	NA	1-2-3-4-5-6-7-...
2	1	2-3-4-5	NA	2-3-4-5-6-7-8-9	NA	2-3-4-5-6-7-8-...
3	1	3-4-5-6	NA	3-4-5-6-7-8-9-10	NA	3-4-5-6-7-8-9-...
4	1			4-5-6-7-8-9-10-11	NA	4-5-6-7-8-9-10-...
5	1			5-6-7-8-9-10-11-12	NA	5-6-7-8-9-10-11-...
6	1			6-7-8-9-10-11-12-13	NA	6-7-8-9-10-11-12-...
7	1			7-8-9-10-11-12-13-14	NA	7-8-9-10-11-12-13-...
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	1					14-15-16-17-18-19-20-...
15	1					15-16-17-18-19-20-21-...

4.2.8 Clock Configuration (CC)

CR.6 sets the clock configuration. The clock configuration determines which edge of the clock the flash device will respond to while in burst mode. The device can be configured to either track on the rising or falling edge of the clock.

4.2.9 Burst Wrap (BW)

CR.3 sets the burst wrap. The burst wrap determines how the device will handle a burst-mode read that crosses a 16-word row boundary. Wrap can be set to have either the burst mode wrap around to the same row or have the burst read consecutive addresses.

Wrap applies to 4- and 8-word burst modes only. Wrap has no effect in continuous burst mode. In 4- and 8-word burst mode with wrap enabled, the WAIT signal will not be asserted. In 4- and 8-word burst mode with wrap disabled, the WAIT signal will be asserted only if a 16-word row boundary is crossed.

4.2.10 Burst Length (BL_{2-0})

CR.2–CR.0 sets the burst length. The burst length determines the maximum number of consecutive words the device will output during a burst-mode read. 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O supports 4-, 8- and continuous-word burst lengths.

4.3 Read Query Register

The query plane comes to the foreground and occupies a 4-Mbit address range at the partition supplied by the Read Query command address. The mode outputs Common Flash Interface (CFI) data when partition addresses are read. Appendix C, “Common Flash Interface” on page 68 shows query mode information and addresses. Issuing a Read Query command to a partition that is programming or erasing places that partition’s outputs in read query mode while the partition continues to program or erase in the background. The Read Query command is subject to read restrictions dependent on the parameter partition availability. Refer to Table 15, “Simultaneous Operations Allowed with the Protection Register” on page 32 for details.

4.4 Read ID Register

The Identification (ID) Register contains various product information, such as manufacturer ID, device ID, block lock status, protection register information, and configuration register settings. To obtain any information from the ID register, execute the Read ID Register command. Information contained in this register can only be accessed by executing a single-word asynchronous read.

Table 11. Device Identification Codes

Item			Address[1,2,3]	Data
Manufacturer Code			PBA + 000000h	0089h
Device Code:	32 Mbit	- T	PBA + 000001h	8852h
		- B		8853h
	64 Mbit	- T	PBA + 000001h	8854h
		- B		8855h
	128 Mbit	- T	PBA + 000001h	8856h
		- B		8857h
Block Lock Configuration[4] • Block Is Unlocked • Block Is Locked • Block Is Not Locked-Down • Block Is Locked-Down			MBBA + 000002h or PBBA + 000002h, depends on block	 $DQ_0 = 0$ $DQ_0 = 1$ $DQ_1 = 0$ $DQ_1 = 1$

Table 11. Device Identification Codes

Item	Address[1,2,3]	Data
Configuration Register Settings	PBA + 000005h	CD[5]
Protection Register Lock Status	PBA + 000080h	PR-LK[6]
Protection Register Data	PBA +000081h - 000088h	PR[7]

NOTES:
1. PBA = Partition Base Address. PBA = $A_{MAX - 18}$.
2. MBBA = Main Block Base Address. MBBA = $A_{MAX - 15}$.
3. PBBA = Parameter Block Base Address. PBBA = $A_{MAX - 12}$.
4. See the Block Lock Status section for valid lock status.
5. CD = Configuration Register Settings.
6. PR-LK = Protection Register Lock status.
7. PR = Protection Register data.

4.5 Read Status Register

The status register is 8 bits wide. The status register contains information pertaining to the current condition of the flash device and its partitions. To determine a partition's status, execute the Read Status Register command. To read status register data, execute a signal-word asynchronous read. A status register bit is considered set if its value is a one (1) and cleared if its value is a zero (0). Status register data is output on DQ_{7-0}; DQ_{15-8} outputs 00h. Each partition has its own status register data. Information contained in this register can only be accessed by executing a single-word asynchronous read.

Table 12. Status Register Definitions

DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
DWS	ESS	ES	PS	VPPS	PSS	DPS	PWS
SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0

SR bit	Bit Name	NOTES
SR.7	Device WSM Status (DWS)	0 = Device busy with a program or erase operation. 1 = Device ready. For EFP, see Table 13.
SR.6	Erase Suspend Status (ESS)	0 = No erase operation, if any, is being suspended. 1 = An erase operation is being suspended.
SR.5	Erase Suspend (ES)	0 = Block erase successful. 1 = Block erase error. One of three bits set to indicate a command sequence error.
SR.4	Program Status (PS)	0 = Word program successful. 1 = Word program error. One of three bits set to indicate a command sequence error.
SR.3	V_{PP} Status (VPPS)	0 = V_{PP} voltage level > V_{PPLK}. 1 = V_{PP} voltage level ≤ V_{PPLK}. Hardware program/erase lockout. Note: This bit does not provide continuous V_{PP} feedback. Signal functionality is not guaranteed when $V_{PP} \neq V_{PP1}$ or V_{PP2}.
SR.2	Program Suspend Status (PSS)	0 = No program operation, if any, is being suspended. 1 = A program operation is being suspended.
SR.1	Device Protect Status (DPS)	0 = Block unlocked. 1 = An erase or program operation was attempted on a locked block. WP# = V_{IL}.
SR.0	Partition Write/Erase Status (PWS)	0 = No other partition is busy. 1 = Another partition is busy performing an erase or program operation. For EFP, see Table 13.

Table 13. Status Register DWS and PWS Description

DWS (SR.7)	PWS (SR.0)	Description
0	0	The addressed partition is performing a program/erase operation. No other partition is active. Enhanced Factory Programming: device is finished programming or verifying data or is ready for data.
0	1	A partition other than the one currently addressed is performing a program/erase operation. Enhanced Factory Programming: the device is either programming or verifying data.
1	0	No program/erase operation is in progress in any partition. Erase and Program suspend bits (SR.6 and SR.2) indicate whether other partitions are suspended. Enhanced Factory Programming: the device has exited EFP mode.
1	1	Won't occur in standard program or erase modes. Enhanced Factory Programming: this combination will not occur.

4.5.1 Clear Status Register

To clear the status register, execute the Clear Status Register command. When the status register is cleared, only bits 1, 3, 4, and 5 are cleared. A status register bit is considered set if its value is a one (1) and cleared if its value is a zero (0). Since bits 0, 2, 6 and 7 indicated different error conditions and/or device states, these bits can only be set and cleared by the WSM and are not cleared when a Clear Status Register command is given. The status register should be cleared before implementing any program or erase operations. After executing the Clear Status Register command, the device returns to read array mode. A device reset also clears the status register.

4.6 Read-While-Write/Erase

1.8 Volt Intel® Wireless Flash Memory supports a new flash multi-partition architecture. By dividing the flash memory into many separate partitions, the device is capable of reading from one partition while programing or erasing in another partition; hence the terms, Read-While-Write (RWW) and Read-While-Erase (RWE). These features greatly enhance flash data storage performance.

To perform a RWW operation, execute the Word Program command to one partition. While this operation is being performed by the flash WSM, execute the Read Array command to another partition.

To perform a RWE operation, execute the Block Erase command to one partition. While this operation is being performed by the flash WSM, execute the Read Array command to another partition.

1.8 Volt Intel Wireless Flash Memory does not support simultaneous program and erase operations. Attempting to perform operations such as these will result in a command sequence error. Only one partition may be programming or erasing while another is reading.

5.0 Program and Erase Voltages

The 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O and SRAM memory provides in-system program and erase at V_{PP1}. For factory programming, it also includes a low-cost, backward-compatible 12 V programming feature. It also includes an Enhanced Factory Programming (EFP) feature.

5.1 Factory Program Mode

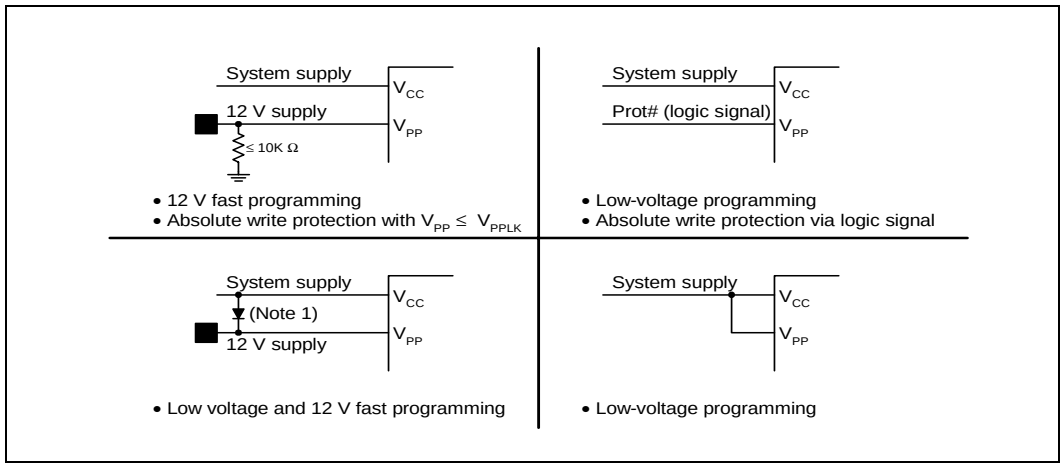
The standard factory programming mode uses the same commands and algorithm as the Word Program mode (40h/10h). When V_{PP} is at V_{PP1}, program and erase currents are drawn through the V_{CC} pin. Note that if V_{PP} is driven by a logic signal, V_{PP1} must remain above the V_{PP1}Min value to perform in-system flash modifications. When V_{PP} is connected to a 12 V power supply, the device draws program and erase current directly from the V_{PP} pin. This eliminates the need for an external switching transistor to control the V_{PP} voltage. Figure 9, “Example of V_{PP} Power Supply Configurations shows examples of flash power supply usage in various configurations.

The 12 V V_{PP} mode enhances programming performance during the short time period typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during program and erase operations as specified in Section 11.2, “Extended Temperature Operation” on page 35. V_{PP} may be connected to 12 V for a total of t_{PPH} hours maximum. Stressing the device beyond these limits may cause permanent damage.

5.2 Programming Voltage Protection (V_{PP})

In addition to the flexible block locking, holding the V_{PP} programming voltage low can provide absolute hardware write protection of all flash-device blocks. If V_{PP} is below V_{PPLK}, program or erase operations will result in an error displayed in the status register bit SR.3 (set to 1).

Figure 9. Example of V_{PP} Power Supply Configurations



NOTE: If the V_{CC} supply can sink adequate current, an appropriately valued resistor can be used.

5.3 Enhanced Factory Programming (EFP)

EFP substantially improves device programming performance via a number of enhancements to the conventional 12-volt word program algorithm. EFP's more efficient WSM algorithm eliminates the traditional overhead delays of conventional word program mode in both the host programming system and the flash device. Changes to the flowchart and internal routine were developed because of today's beat-rate-sensitive manufacturing environments; a balance between programming speed and cycling performance was struck.

After a single command sequence, host programmer bus cycles write data words followed by status checks to determine when the next data word is ready to be accepted. This modification essentially cuts write bus cycles in half. Following each internal program pulse, the WSM automatically increments the device's address to the next physical location. Now, programming equipment can sequentially stream program data throughout an entire block without having to setup and present each new address. In combination, these enhancements reduce much of the host programmer overhead, enabling more of a data streaming approach to device programming.

Additionally, EFP speeds up programming by performing internal code verification. With this, PROM programmers can rely on the device to verify that it's been programmed properly. From the device side, EFP streamlines internal overhead by eliminating the delays previously associated to switch voltages between programming and verify levels at each memory-word location.

EFP consists of four phases: setup, program, verify and exit. Refer to Figure 32, “Enhanced Factory Program Flowchart” on page 63 for a detailed graphical representation on how to implement EFP.

5.3.1 EFP Requirements and Considerations

EFP requirements:

- Ambient temperature: T_A= 25 °C ±5 °C
- V_{CC} within specified operating range
- V_{PP} within specified V_{PP2} range
- Target block unlocked

EFP considerations:

- Block cycling below 10 erase cycles(1)
- RWW not supported(2)
- EFP programs one block at a time
- EFP cannot be suspended

(1)Recommended for optimum performance. Some degradation in performance may occur if this limit is exceeded, but the internal algorithm will continue to work properly.

(2)Code or data cannot be read from another partition during EFP.

5.3.2 Setup Phase

After receiving the EFP Setup (30h) and Confirm (D0h) command sequence, device SR.7 transitions from a ‘1’ to a ‘0’ indicating that the WSM is busy with EFP algorithm startup. A delay before checking SR.7 is required to allow the WSM time to perform all of its setups and checks (V_{PP} level and block lock status). If an error is detected, status register bits SR.4, SR.3 and/or SR.1 are set and EFP operation terminates.

5.3.3 Program Phase

After setup completion, the host programming system must check SR.0 to determine “data-stream ready” status (SR.0=0). Each subsequent write after this is a program-data write to the flash array. Each cell within the memory word to be programmed to ‘0’ will receive one WSM pulse; additional pulses, if required, occur in the verify phase. SR.0=1 indicates that the WSM is busy applying the program pulse.

The host programmer must poll the device's status register for the “program done” state after each data-stream write. SR.0=0 indicates that the appropriate cell(s) within the accessed memory location have received their single WSM program pulse, and that the device is now ready for the next word. Although the host may check full status for errors at any time, it is only necessary on a block basis, after EFP exit.

Addresses must remain within the target block. Supplying an address outside the target block immediately terminates the program phase; the WSM then enters the EFP verify phase.

The address can either hold constant or it can increment. The device compares the incoming address to that stored from the setup phase (WA_0); if they match, the WSM programs the new data word at the next sequential memory location. If they differ, the WSM jumps to the new address location.

The program phase concludes when the host programming system writes to a different block address; data supplied must be FFFFh. Upon program phase completion, the device enters the EFP verify phase.

5.3.4 Verify Phase

A high percentage of the flash bits program on the first WSM pulse. However, for those cells that do not completely program on their first attempt, EFP internal verification identifies them and applies additional pulses as required.

The verify phase is identical in flow to that of the program phase, except that instead of programming incoming data, the WSM compares the verify-stream data to that which was previously programmed into the block. If the data compares correctly, the host programmer proceeds to the next word. If not, the host waits while the WSM applies an additional pulse(s).

The host programmer must reset its initial verify-word address to the same starting location supplied during the program phase. It then reissues each data word in the same order it did during the program phase. Like programming, the host may write each subsequent data word to WA_0 or it may increment up through the block addresses.

The verification phase concludes when the interfacing programmer writes to a different block address; data supplied must be FFFFh. Upon verify phase completion, the device enters the EFP exit phase.

5.3.5 Exit Phase

SR.7=1 indicates that the device has returned to normal operating conditions. A full status check should be performed at this time to ensure the entire block programmed successfully. After EFP exit, any valid CUI command can be issued.

5.4 Write Protection ($V_{PP} < V_{PPLK}$)

If the V_{PP} voltage is below the V_{PP} lockout threshold, word programming is prohibited. To ensure proper word program operation, V_{PP} must be set to one of the two valid V_{PP} ranges. To determine program status, poll the status register and analyze the bits.

When V_{PP} is at V_{PP1}, program currents are drawn through the V_{CC} supply. If V_{PP} is driven by a logic signal, V_{PP1} must remain above the V_{PP1} minimum value in order to program erase mode.

6.0 Flash Erase Mode

6.1 Block Erase

Flash erasing is performed on a block-by-block basis; therefore, only one block may be erased at any given time. Once a block is erased, all bits within that block will read as a logic level one (1).

To erase a block, execute the Block Erase command. To determine the status of a block erase, poll the status register and analyze the bits.

If the device is put in standby mode during an erase operation, the device will continue to erase until to operation is complete; then it will enter standby mode.

Refer to Figure 33, "Block Erase Flowchart" on page 64 for a detailed flow on how to implement a block erase operation.

6.2 Erase Protection ($V_{PP} < V_{PPLK}$)

If the V_{PP} voltage is below the V_{PP} lockout threshold voltage, block erasure is prohibited. To ensure proper block erase operation, V_{PP} must be set to one of the two valid V_{PP} levels. To determine block erase status, poll the status register and analyze the bits.

When V_{PP} is at V_{PP1}, erase currents are drawn through the V_{CC} supply. If V_{PP} is driven by a logic signal, V_{PP1} must remain above the V_{PP1} minimum value in order to erase a block.

7.0 Flash Suspend/Resume Modes

7.1 Program/Erase Suspend

To suspend program or erase, execute the suspend command. Suspend halts any in-progress word programming or block erase operation. The Suspend command can be written to any device address, and the partition being addressed remains in its previous command state. A Suspend command allows data to be accessed from any memory location other than those suspended.

A program operation can be suspended to allow a read. An erase operation can be suspended to allow word programming or device reads within any except the suspended block. A program operation nested within an erase suspend can be suspended to read the flash device. Once the program/erase process starts, a suspend can only occur at certain points in the program/erase algorithm. Erase cannot resume until program operations initiated during the erase suspend are complete. All device read functions are permitted during suspend.

During a suspend, V_{PP} must remain at a valid program level and WP# must not change. Also, a minimum time is required between issuing a Program or Erase command and then issuing a Suspend command.

7.2 Program/Erase Resume

The Resume command (D0H) instructs the WSM to continue programming/erasing and automatically clears status register bits SR.2 (or SR.6) and SR.7. The Resume command can be written to any partition. If status register error bits are set, the status register can be cleared before issuing the next instruction. RST# must remain at V_{IH}. See Figure 31, "Program Suspend/Resume Flowchart" on page 62 and Figure 34, "Erase Suspend/Resume Flowchart" on page 65.

If a suspended partition was placed in read array, read status register, read identifier (ID), or read query mode during the suspend, the device will remain in that mode and output data corresponding to that mode after the program or erase operation is resumed. After resuming a suspend operation,

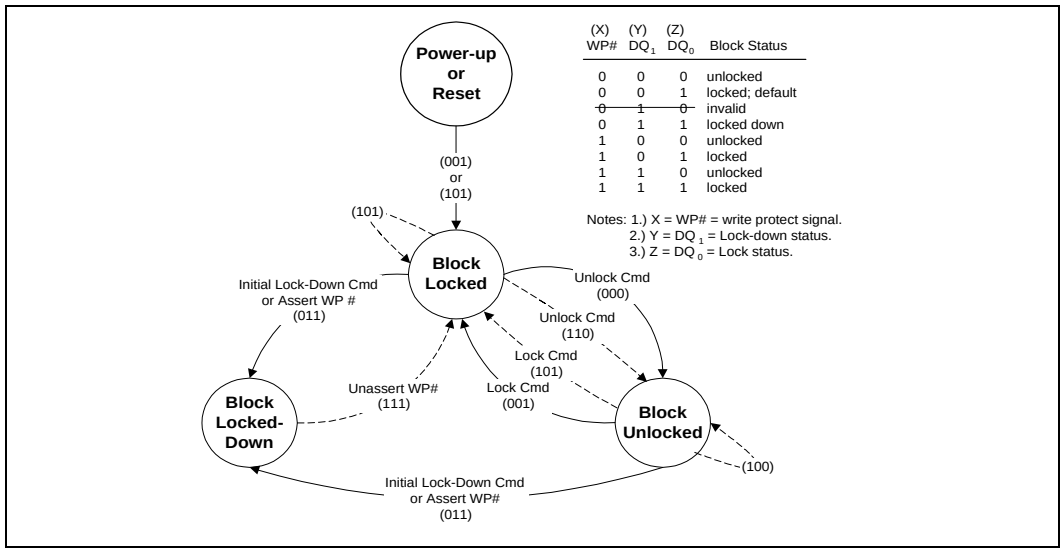
always issue the Read Mode command appropriate to the read operation. To read status after resuming a suspended operation, issue a Read Status Register command (70H) to return the suspended partition to status mode.

8.0 Flash Security Modes

The 1.8 Volt Intel® Wireless Flash Memory with 3 Volt I/O offers both hardware and software security features to protect the flash data. The software security feature is used by executing the Lock Block command. The hardware security feature is used by executing the Lock-Down Block command AND by asserting the WP# and V_{PP} signals.

For details on V_{PP} data security, refer to Section 5.4, “Write Protection ($V_{PP} < V_{PPLK}$)” on page 27 and Section 6.2, “Erase Protection ($V_{PP} < V_{PPLK}$)” on page 28. Refer to Figure 10, “Block Locking State Diagram for a state diagram of the flash security features. Also see Figure 35, “Locking Operations Flowchart” on page 66.

Figure 10. Block Locking State Diagram



NOTES:
1. The notation (X,Y,Z) denotes the locking state of a block, The current locking state of a block is defined by the state of WP# and the two bits of the block-lock status DQ_{1-0}.
2. Solid line indicates WP# asserted (low). Dashed line indicates WP# unasserted (high).

8.1 Block Lock

All blocks default to locked (states [001] or [101]) upon power-up or reset. Locked blocks are fully protected from alteration. Attempted program or erase operations to a locked block will return an error in status register bit SR.1. A locked block’s status can be changed to unlocked or lock-down using the appropriate software commands. Writing the Lock Block command sequence can lock an unlocked block.

8.2 Block Unlock

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to locked when the device is reset or powered down. An unlocked block can be locked or locked-down using the appropriate software commands. If it's not locked-down, a locked block can be unlocked by writing the Unlock Block command sequence.

8.3 Lock-Down Block

Locked-down blocks (state [011]) are protected from program and erase operations, but unlike locked blocks, software commands alone cannot change their protection status. A locked-down block can only be unlocked when WP# is high. When WP# is low, all locked-down blocks revert to locked. A locked or unlocked block can be locked-down by writing the Lock-Down Block command sequence. Locked-down blocks revert to the locked state at device reset or power-down.

8.4 Block Lock Operations during Erase Suspend

Block lock configurations can be performed during an erase suspend by using the standard locking command sequences to unlock, lock, or lock-down a block. Useful when another block requires immediate updating.

To change block locking during an erase operation, first write the Erase Suspend command. After checking SR.6 to determine that the erase operation has suspended, write the desired lock command sequence to a block; the lock status will be changed. After completing lock, unlock, read, or program operations, resume the erase operation with the Erase Resume command (D0h).

If a block is locked or locked-down during a suspended erase of the same block, the locking status bits will change immediately. But when resumed, the erase operation will complete.

Locking operations cannot occur during program suspend. Appendix A, "Flash Write State Machine (WSM)" shows valid commands during erase suspend.

8.5 WP# Lock-Down Control

WP# allows block lock-down to be overridden. Table 14 defines device write protection methodology.

WP# controls the lock-down function. WP# = V_{IL}(0) protects locked-down blocks [011] from program, erase, and lock status changes. When WP# = V_{IH}(1), the locked-down blocks revert to locked [111]. A software command can then individually unlock a block [110] for erase or program. These blocks can then be re-locked [111] while WP# remains high. When WP# returns low, previously locked-down blocks revert to the lock-down state [011] regardless of changes made while WP# was high. Device reset or power-down resets all blocks to the locked state [101] or [001].

Table 14. Write Protection Truth Table

V_{PP}	WP#	RST#	Write Protection
X	X	V_{IL}	Reset mode, device Inaccessible
V_{IL}	X	V_{IH}	Program and Erase Prohibited
> V_{PPLK}	V_{IL}	V_{IH}	All Lock-down Blocks are Locked
>V_{PPLK}	V_{IH}	V_{IH}	All Lock-down Blocks are Unlockable

9.0 Flash Protection Register

The 1.8 Volt Intel® Wireless Flash Memory includes a 128-bit protection register. This protection register can be used to increase system security and/or for identification purposes. The protection register value can match the flash component to the system's CPU or ASIC to prevent device substitution.

The lower 64-bit segments within the protection register are programmed by Intel with a unique number in each flash device. The upper 64-bit segments within the protection register are left for the customer to program. Once programmed, the customer segment can be locked to prevent further reprogramming.

The protection register shares some of the same internal flash resources as the parameter partition. Therefore, read-while-write is only allowed between the protection register and main partitions. Table 15 describes the operation allowed using read-while-write/erase with the protection register.

Table 15. Simultaneous Operations Allowed with the Protection Register

Protection Register	Parameter Partition Array Data	Main Partition	Notes
Read	Conditional–See Notes	Write/Erase	While programming or erasing in a main partition, the protection register may be read from any other partition. Reading the parameter partition data is not allowed if the protection register is being read from addresses within the parameter partition.
Conditional–See Notes	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers from parameter partition addresses is not allowed.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers in a partition that is *different* from the one being programed/erased, and also *different* from the parameter partition, is allowed.
Write	No Access Allowed	Read	While programming the protection register, reads are only allowed in the other main partitions. Access to the parameter partition is not allowed. This is because programming of the protection register can only occur in the parameter partition, so it will exist in status mode.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the protection registers are not allowed in *any* partition. Reads in other main partitions are supported.

9.1 Protection Register Read

Writing the Read Identifier command allows the protection register data to be read 16 bits at a time from addresses shown in Table 11, "Device Identification Codes" on page 21. The ID plane, containing the protection registers, appears over partition addresses corresponding to the partition address supplied with the command. Writing the Read Array command returns the device to read array mode.

9.2 Program Protection Register

The Protection Program command should be issued only at the bottom partition followed by the data to be programed at the specified location. It programs the 64-bit user protection register 16 bits at a time. Table 11, "Device Identification Codes" on page 21 and Table 16, "Protection Register

Addressing" on page 33 show allowable addresses. See also Figure 36, "Protection Register Programming Flowchart" on page 67. Issuing a Protection Program command outside the register's address space results in a status register error (SR.4 = 1).

Table 16. Protection Register Addressing

Word	Use	ID Offset	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word
LOCK	Both	PBA+000080h	1	0	0	0	0	0	0	0	LOCK
0	Intel	PBA+000081h	1	0	0	0	0	0	0	1	0
1	Intel	PBA+000082h	1	0	0	0	0	0	1	0	1
2	Intel	PBA+000083h	1	0	0	0	0	0	1	1	2
3	Intel	PBA+000084h	1	0	0	0	0	1	0	0	3
4	Customer	PBA+000085h	1	0	0	0	0	1	0	1	4
5	Customer	PBA+000086h	1	0	0	0	0	1	1	0	5
6	Customer	PBA+000087h	1	0	0	0	0	1	1	1	6
7	Customer	PBA+000088h	1	0	0	0	1	0	0	0	7

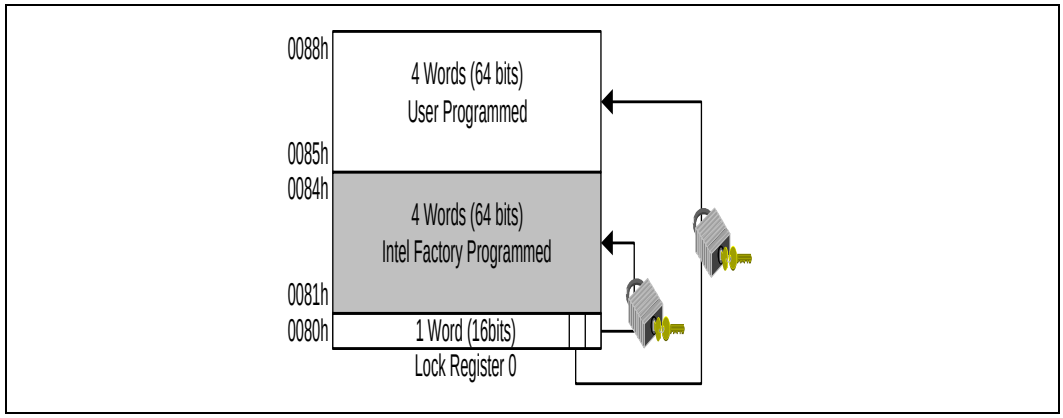
NOTE: Addresses A_{17}–A_8 should be set to zero. A_{MAX}–A_{18} = partition base address (PBA).

9.3 Protection Register Lock

The protection register's user-programmable segment is lockable by programming "0" to the PR-LOCK register bits "1" using the Protection Program command (Figure 11). PR-LOCK register bit "0" is programmed to 0 at the Intel factory to protect the unique device number. PR-LOCK register bit "1" can be programmed by the user to lock the 64-bit user register. This bit is set using the Protection Program command to program "FFFDh" into PR-LOCK register 0.

After PR-LOCK register bits have been programmed, no further changes can be made to the protection register's stored values. Protection Program commands written to a locked section result in a status register error (program error bit SR.4 and lock error bit SR.1 are set to 1). Once locked, protection register states are not reversible.

Figure 11. Protection Register Locking



10.0 Power and Reset Considerations

10.1 Power-Up/Down Characteristics

In order to prevent any condition that may result in a spurious write or erase operation, it is recommended to power-up V_{CC}, V_{CCQ} and S-V_{CC} together. Conversely, V_{CC}, V_{CCQ} and S-V_{CC} must power-down together.

It is also recommended to power-up V_{PP} with or slightly after V_{CC}. Conversely, V_{PP} must power-down with or slightly before V_{CC}.

If V_{CCQ} and/or V_{PP} are not connected to the V_{CC} supply, then V_{CC} should attain V_{CC}Min before applying V_{CCQ} and V_{PP}. Device inputs should not be driven before supply voltage = V_{CC}Min. Power supply transitions should only occur when RST# is low.

10.2 Power Supply Decoupling

When the device is accessed, many internal conditions change. Circuits are enabled to charge pumps and voltages are switched. All this internal activity produces transient signals. The magnitude of these transient signals depends on the device and the system capacitive and inductive loading. To minimize the effect of these transient signals, a 0.1 µF ceramic decoupling capacitor is required across each V_{CC}, V_{CCQ}, V_{PP}, S-V_{CC} to system ground. Capacitors should also be placed as close as possible to the package balls.

10.3 Flash Reset Characteristics

By holding the flash device in reset during power-up/down transitions, invalid bus conditions can be masked. The flash device enters a reset mode when RST# is driven low. In reset mode, internal flash circuitry is turned off and outputs are placed in a high-impedance state.

After return from reset, a certain amount of time is required before the flash device is capable of performing normal operations. Upon return from reset, the flash device defaults to page mode.

If RST# is driven low during a program or erase operation, the operation will be aborted and the memory contents at the aborted block or address are no longer valid. See Figure 24, “Reset Operations Waveforms” on page 52 for detailed information regarding reset timings.

11.0 Electrical Specifications

11.1 Absolute Maximum Ratings

Parameter	Note	Maximum Rating
Temperature under Bias		–25 °C to +85 °C
Storage Temperature		–65 °C to +125 °C
Voltage On Any Signals (except V_{CC}, V_{CCQ}, V_{PP} and S-V_{CC})	1	–0.5 V to +3.80 V
V_{PP} Voltage	1,2,3	–0.2 V to +14 V
V_{CC} Voltage	1	–0.2 V to +2.40 V
V_{CCQ} and S-V_{CC} Voltage	1	–0.2 V to +3.36 V
Output Short Circuit Current	4	100 mA

NOTES:
1. All specified voltages are with respect to V_{SS}. Minimum DC voltage is –0.5 V on input/output signals and –0.2 V on V_{CC} and V_{PP} supplies. During transitions, this level may undershoot to –2.0 V for periods <20 ns which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns.
3. V_{PP} program voltage is normally V_{PP1}. V_{PP} can be V_{PP2} for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase.
4. Output shorted for no more than one second. No more than one output shorted at a time.

NOTICE: This datasheet contains preliminary information on new products in production. Specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

11.2 Extended Temperature Operation

Symbol	Parameter		Note	Min	Max	Unit
T_A	Operating Temperature			–25	85	°C
V_{CC}	V_{CC} Supply Voltage			1.70	1.90	V
V_{CCQ}, S-V_{CC}	Flash I/O and SRAM Supply Voltages		2	2.20	3.30	V
V_{PP1}	V_{PP} Voltage Supply (Logic Level)		1	0.90	1.90	V
V_{PP2}	Factory Programming V_{PP}		1	11.4	12.6	
t_{PPH}	Maximum V_{PP} Hours	$V_{PP} = V_{PP2}$	1		80	Hours
Block Erase Cycles	Main and Parameter Blocks	$V_{PP} = V_{CC}$	1	100,000		Cycles
	Main Blocks	$V_{PP} = V_{PP2}$	1		1000	
	Parameter Blocks	$V_{PP} = V_{PP2}$	1		2500	

NOTES:
1. In normal operation, the V_{PP} program voltage is V_{PP1}. V_{PP} can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles at extended temperature on parameter blocks.
2. V_{CCQ} and S-V_{CC} must be tied together, except when in Data Retention Mode.

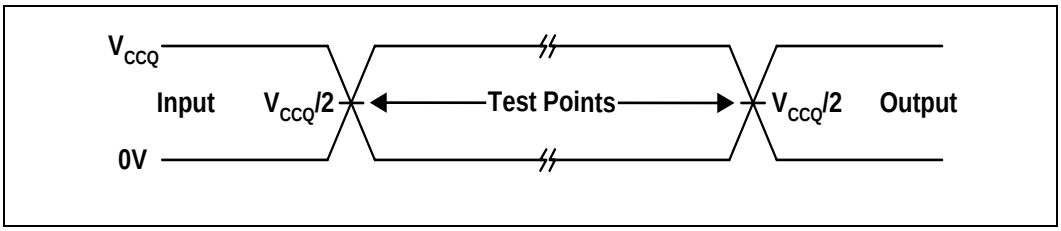
11.3 DC Characteristics

Sym	Parameter (1)		Device	Note	Min	Typ	Max	Unit	Test Condition	
I_{LI}	Input Load Current		Flash/ SRAM	1			±2	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max S-V_{CC} = S-V_{CC}Max Inputs = V_{CCQ} or V_{SS}	
I_{LO}	Output Leakage Current	DQ_{15-0}, WAIT	Flash/ SRAM	1			±10	µA		
I_{CCS}	Standby Current		Flash	1		6	21	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max CE# = V_{CC} RST# =V_{CC} or V_{SS}	
			4-Mbit SRAM	1			20	µA	S-V_{CC} = S-V_{CC}Max S-CS_1# = S-V_{CC} S-CS_2 = S-V_{CC} or S-V_{SS} Inputs = S-V_{CC} or S-V_{SS}	
			8-Mbit SRAM	1			40	µA		
I_{CC}	Operating Power Supply Current (cycle time = 1 µs)		4-Mbit SRAM	1			10	mA	I_{IO} = 0 mA, S-CS_1# = V_{IL} S-SC_2 = S-WE# = V_{IH} Inputs = V_{IL} or V_{IH}	
			8-Mbit SRAM	1			20	mA		
I_{CC2}	Operating Power Supply Current (min cycle time)		4-Mbit SRAM	1			45	mA	Cycle time = min 100% duty I_{IO} = 0 mA, S-CS_1# = V_{IL} S-SC_2 = V_{IH} Inputs = V_{IL} or V_{IH}	
			8-Mbit SRAM	1			65	mA		
I_{CCR}	Average V_{CC} Read Current	Asynchronous Page Mode Read	Flash	2		4	7	mA	4-Word Read	$V_{CC} = V_{CC}$Max CE# = V_{IL} OE# = V_{IH} Inputs = V_{IH} or V_{IL}
		Synchronous CLK = 40 MHz	Flash	2, 3		7	15	mA	4 -Word Burst	
						9	16	mA	8-Word Burst	
						12	22	mA	Continuous Burst	
I_{CCW}	V_{CC} Program Current		Flash	4, 5		18	40	mA	$V_{PP} = V_{PP1}$	
						8	15	mA	$V_{PP} = V_{PP2}$	
I_{CCE}	V_{CC} Block Erase Current		Flash	4, 6		18	40	mA	$V_{PP} = V_{PP1}$	
						8	15	mA	$V_{PP} = V_{PP2}$	
I_{CCWS}	V_{CC} Program Suspend Current		Flash	4		6	21	µA	CE# = V_{CCQ}	
I_{CCES}	V_{CC} Erase Suspend Current		Flash	4, 7		6	21	µA	CE# = V_{CC}	

Sym	Parameter [1]	Device	Note	Min	Typ	Max	Unit	Test Condition
I_{PPS} (I_{PPWS}, I_{PPES})	V_{PP} Standby Current V_{PP} Program Suspend Current V_{PP} Erase Suspend Current	Flash	4		0.2	5	µA	$V_{PP1} \le V_{CC}$
I_{PPR}	V_{PP} Read Current	Flash			2	15	µA	$V_{PP} \le V_{CC}$
I_{PPW}	V_{PP} Program Current	Flash	4		0.05	0.10	mA	$V_{PP} = V_{PP1}$
					8	22		$V_{PP} = V_{PP2}$
I_{PPE}	V_{PP} Erase Current	Flash	4		0.05	0.10	mA	$V_{PP} = V_{PP1}$
					8	22		$V_{PP} = V_{PP2}$
V_{IL}	Input Low Voltage	Flash/ SRAM	9	0		0.4	V	
V_{IH}	Input High Voltage	Flash/ SRAM	9	V_{CCQ} - 0.4		V_{CCQ}	V	
V_{OL}	Output Low Voltage	Flash/ SRAM				0.1	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OL} = 100 µA
V_{OH}	Output High Voltage	Flash/ SRAM		V_{CCQ} - 0.1			V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	Flash	8			0.4	V	
V_{LKO}	V_{CC} Lock Voltage	Flash		1.0			V	
V_{LKOQ}	V_{CCQ} Lock-Out Voltage	Flash		0.90			V	

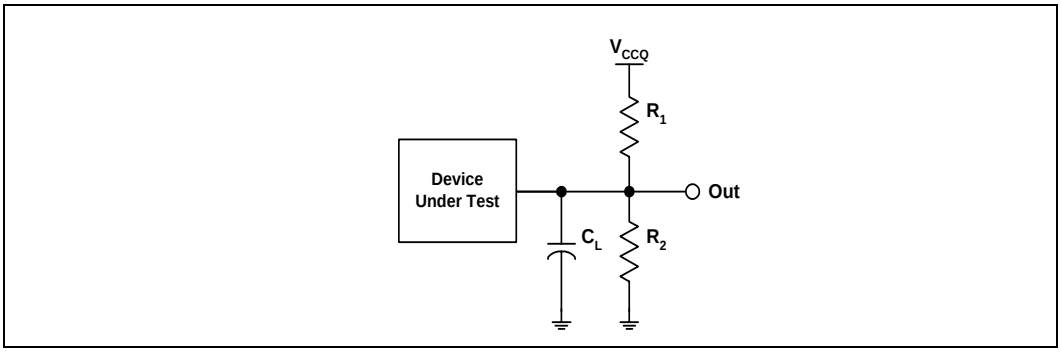
NOTES:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_A = +25 °C.
2. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation.
3. The burst wrap bit (CR.3) determines whether 4-, or 8-word burst accesses wrap within the burst-length boundary, or whether they cross word-length boundaries to perform linear accesses. In the no-wrap mode (CR.3 = 1), the device operates similar to continuous linear burst mode, but consumes less power.
4. Sampled, not 100% tested.
5. V_{CC} read + program current is the summation of V_{CC} read and V_{CC} program currents.
6. V_{CC} read + erase current is the summation of V_{CC} read and V_{CC} block erase currents.
7. I_{CCES} is specified with device deselected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}.
8. Erase and program operations are inhibited when $V_{PP} \le V_{PPLK}$ and not guaranteed outside valid V_{PP1} and V_{PP2} ranges.
9. V_{IL} can undershoot to –0.4 V and V_{IH} can overshoot to V_{CCQ} + 0.4 V for durations of 20 ns or less. AC I/O Test Conditions

Figure 12. AC Input/Output Reference Waveform



NOTES:
1. AC test inputs are driven at V_{CCQ} for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed conditions are when $V_{CC} = V_{CC}$Min.
2. Timing conditions apply to both flash and SRAM.

Figure 13. Transient Equivalent Testing Load Circuit



NOTES:
1. See table for component values.
2. Test configuration component value for worst case speed conditions.
3. C_L includes jig capacitance.

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
V_{CCQ}Min Standard Test	30	25K	25K

11.4 Discrete Capacitance (32-Mbit VF BGA Package)

T_A = +25°C, f = 1 MHz

Sym	Parameter[1]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V
C_{CE}	CE# Input Capacitance	10	12	pF	V_{IN} = 0.0 V

NOTE: 1. Sampled, not 100% tested.

11.5 Stacked Capacitance (32/4 and 64/8 Stacked-CSP Package)

T_A = +25°C, f = 1 MHz

Sym	Parameter[1]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	16	18	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	18	22	pF	V_{OUT} = 0.0 V
C_{CE}	CE# Input Capacitance	10	12	pF	V_{IN} = 0.0 V

NOTE: 1. Sampled, not 100% tested.

12.0 Flash AC Characteristics

12.1 Flash Read Operations

#	Sym	Parameter [1,2]	Speed	–70		–85		Unit
			Note	Min	Max	Min	Max	
R1	t_{AVAV}	Read Cycle Time	3	70		85		ns
R2	t_{AVQV}	Address to Output Delay	3		70		85	ns
R3	t_{ELQV}	CE# Low to Output Delay			70		85	ns
R4	t_{GLQV}	OE# Low to Output Delay	5		30		30	ns
R5	t_{PHQV}	RST# High to Output Delay			150		150	ns
R7	t_{GLQX}	OE# Low to Output in Low-Z	5, 6	0		0		ns
R8	t_{EHQZ}	CE# High to Output in High-Z	6		25		25	ns
R9	t_{GHQZ}	OE# High to Output in High-Z	5, 6		25		25	ns
R10	t_{OH}	CE#, (OE#) High to Output in Low-Z	5, 6	0		0		ns
R101	t_{AVVH}	Address Setup to ADV# High		10		10		ns
R102	t_{ELVH}	CE# Low to ADV# High		10		10		ns
R103	t_{VLQV}	ADV# Low to Output Delay			70		85	ns
R104	t_{VLVH}	ADV# Pulse Width Low		10		10		ns
R105	t_{VHVL}	ADV# Pulse Width High	6	10		10		ns
R106	t_{VHAX}	Address Hold from ADV# High	4	9		9		ns
R108	t_{APA}	Page Address Access Time	4		25		25	ns
R200	f_{CLK}	CLK Frequency			40		33	MHz
R201	t_{CLK}	CLK Period		25		30		ns
R202	$t_{CH/L}$	CLK High or Low Time		9.5		9.5		ns
R203	t_{CHCL}	CLK Fall or Rise Time			3		5	ns
R301	t_{AVCH}	Address Valid Setup to CLK		9		9		ns
R302	t_{VLCH}	ADV# Low Setup to CLK		10		10		ns
R303	t_{ELCH}	CE# Low Setup to CLK		9		9		ns
R304	t_{CHQV}	CLK to Output Delay			20		22	ns
R305	t_{CHQX}	Output Hold from CLK		5		5		ns
R306	t_{CHAX}	Address Hold from CLK	4	10		10		ns
R307	$t_{CHTL/H}$	CLK to WAIT Asserted			20		22	ns
R308	t_{ELTL}	OE# Low to WAIT Active	7		20		22	ns
R309	t_{EHTZ}	CE# (OE#) High to WAIT High-Z	6, 7		25		25	ns
R310	t_{EHEL}	CE# Pulse Width High	7	20		20		ns

NOTES:
1. See Figure 12, “AC Input/Output Reference Waveform” on page 38 for timing measurements and maximum allowable input slew rate.
2. AC specifications assume the data bus voltage is less than or equal to V_{CCQ} when a read operation is initiated.
3. t_{AVAV} = 85 ns for 128-Mbit device.
4. Address hold in synchronous burst-mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
5. OE# may be delayed by up to $t_{ELQV} – t_{GLQV}$ after the falling edge of CE# without impact to t_{ELQV}.
6. Sampled, not 100% tested.
7. Applies only to subsequent synchronous reads.

Figure 14. Single Word Asynchronous Read Waveform

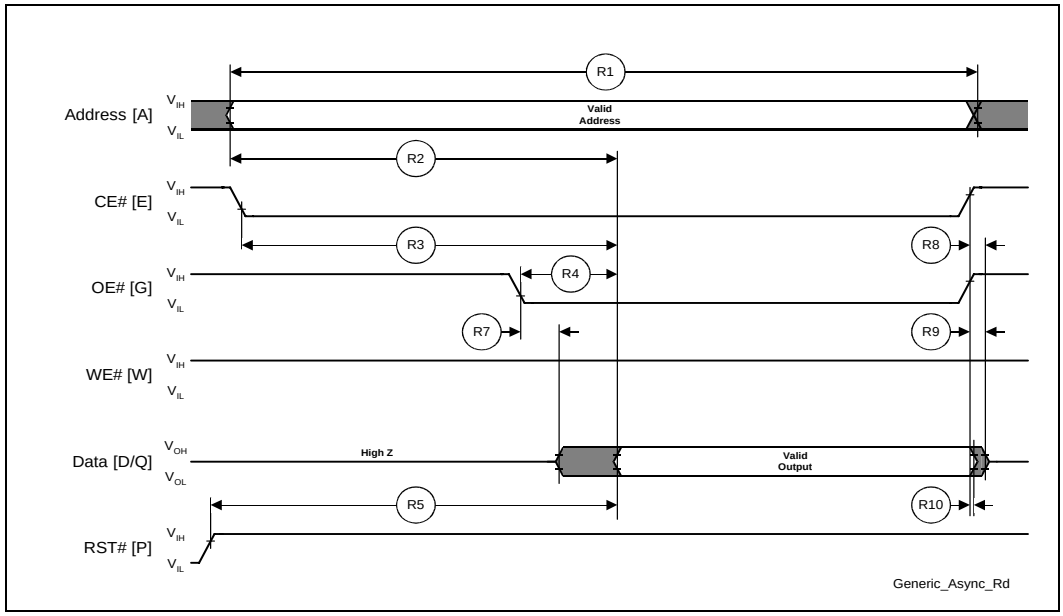


Figure 15. Single Word Latched Asynchronous Read Waveform

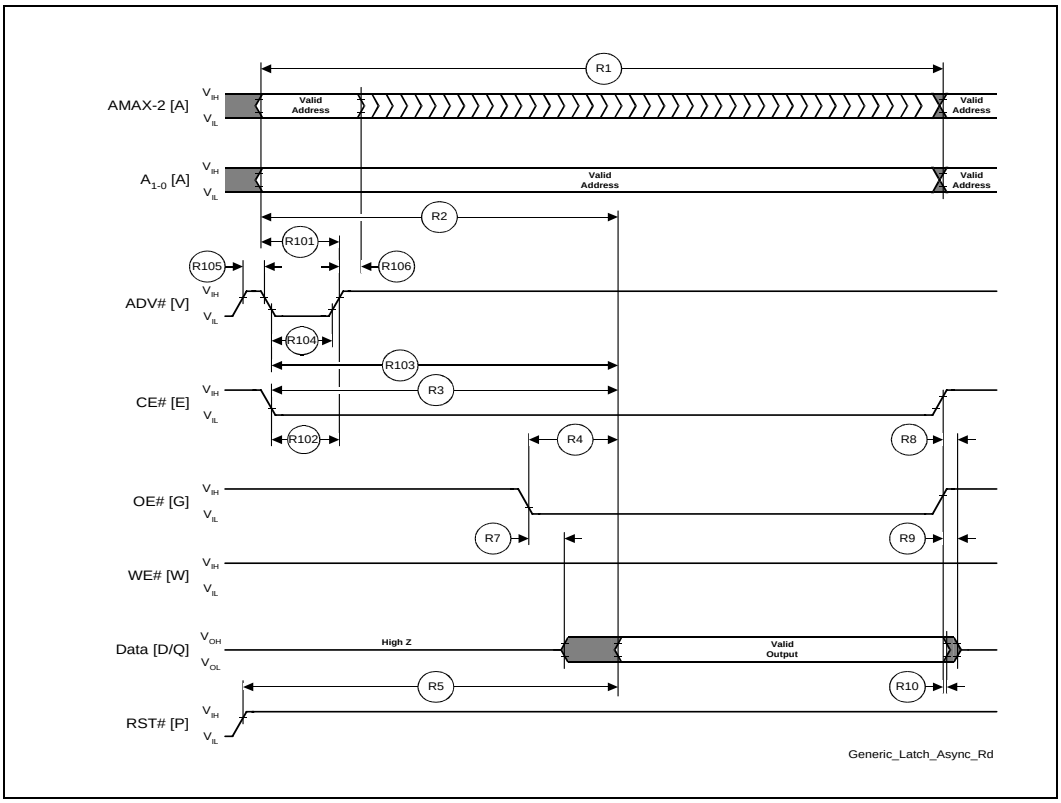


Figure 16. Page Mode Read Waveform

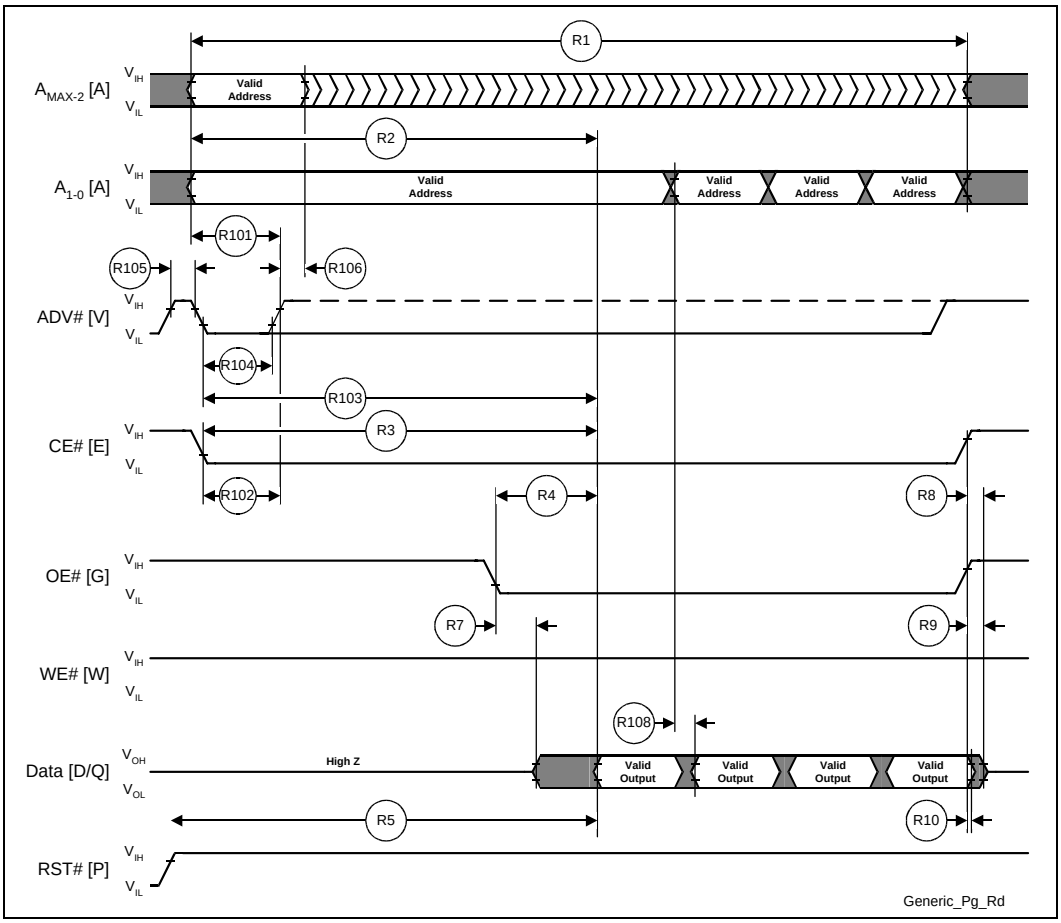
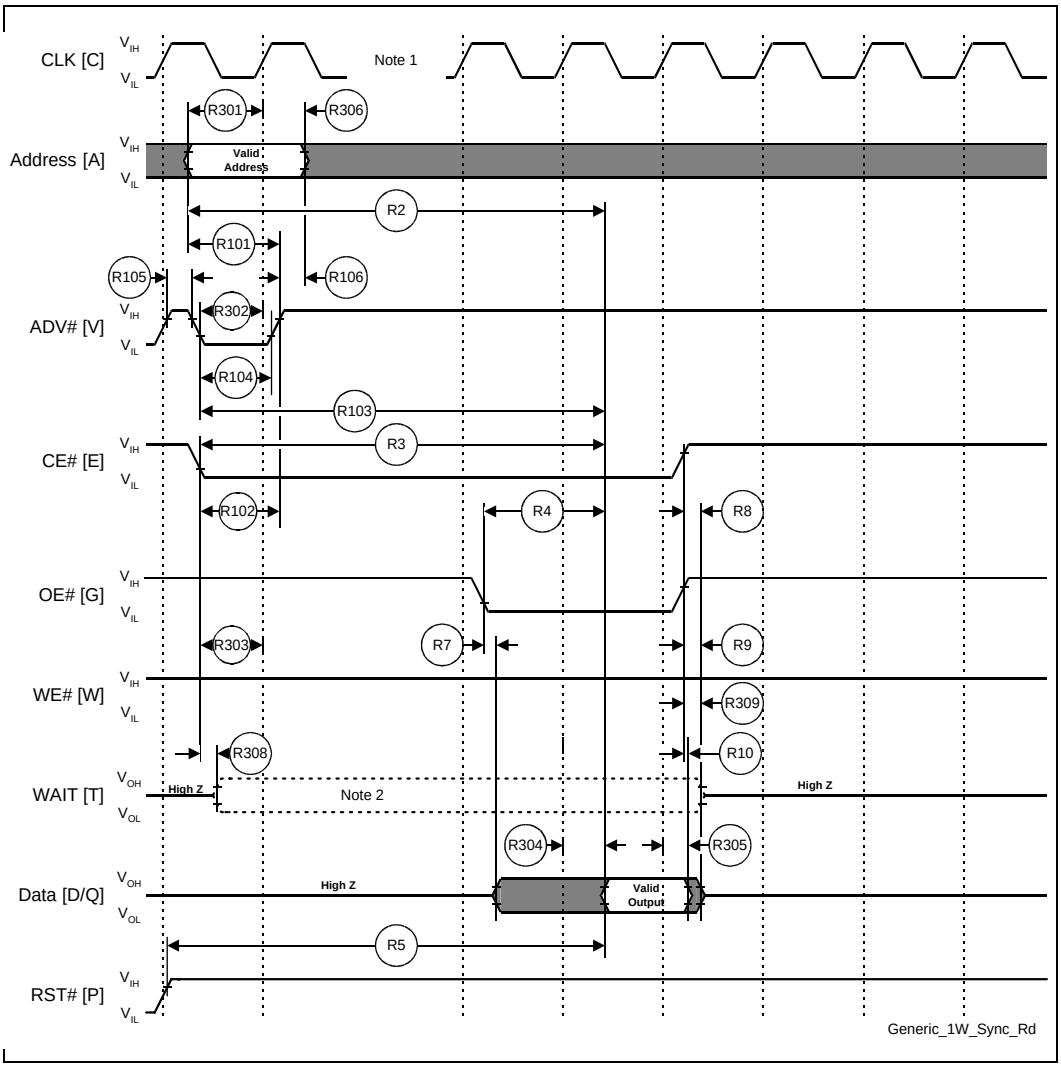


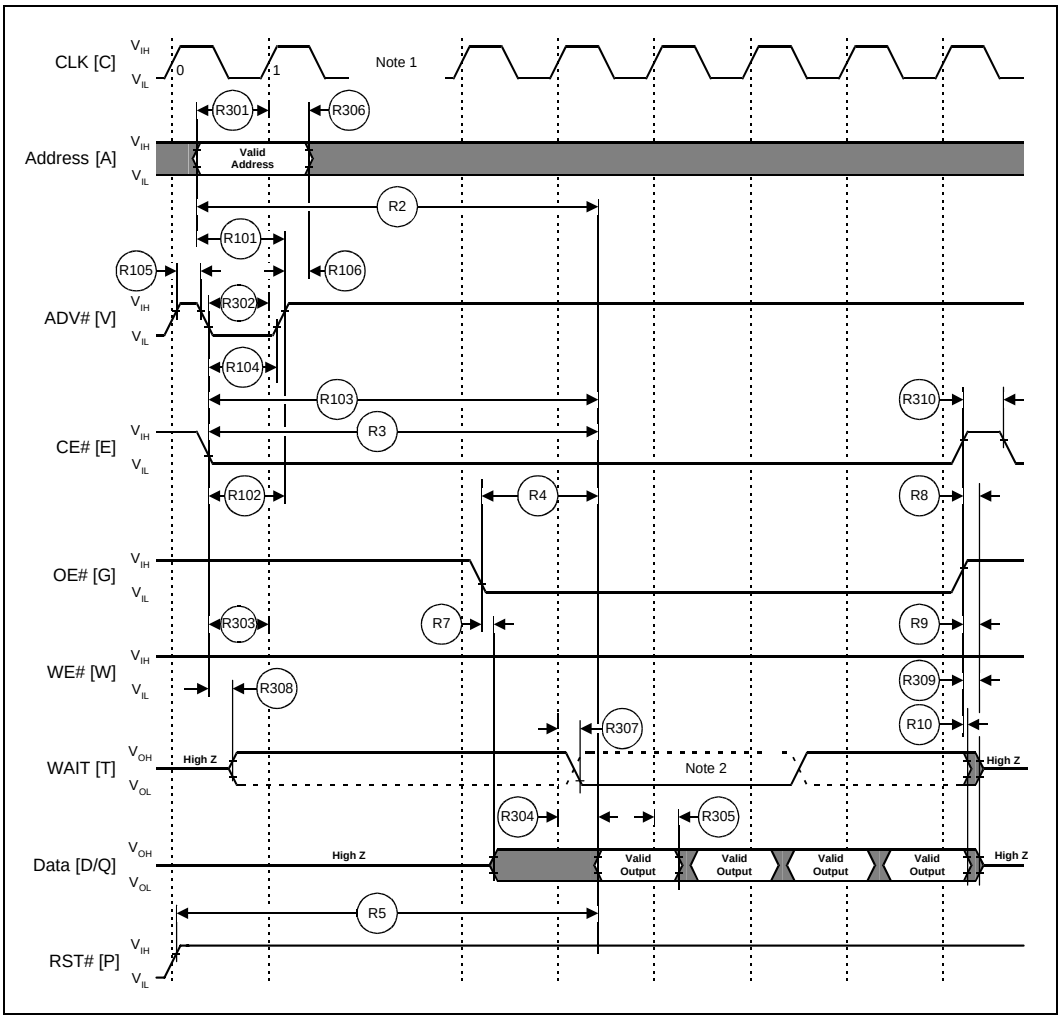
Figure 17. Single Word Burst Read Waveform



NOTES:

1. Section 4.2.2, “First Latency Count (LC2–0)” on page 14 describes how to insert clock cycles during the initial access.
2. WAIT (shown active low) can be configured to assert either during or one data cycle before valid data.

Figure 18. 4 Word Burst Read Waveform



NOTES:

1. Section 4.2.2, “First Latency Count (LC2–0)” on page 14 describes how to insert clock cycles during the initial access.
2. WAIT (shown active low) can be configured to assert either during or one data cycle before valid data.

Figure 19. Clock Input AC Waveform

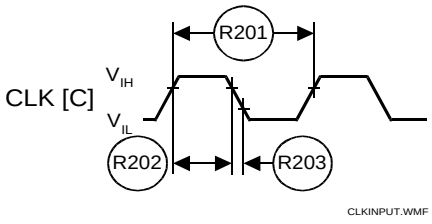
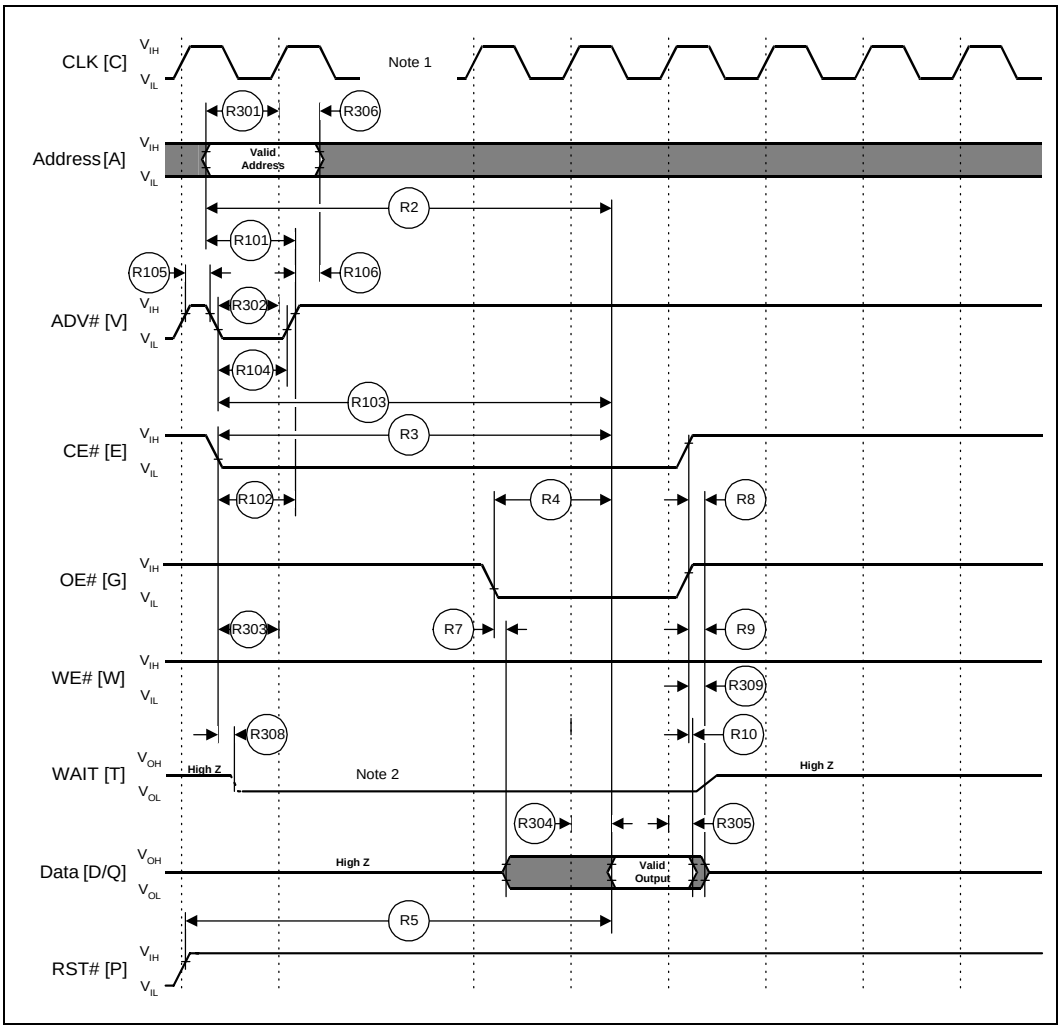
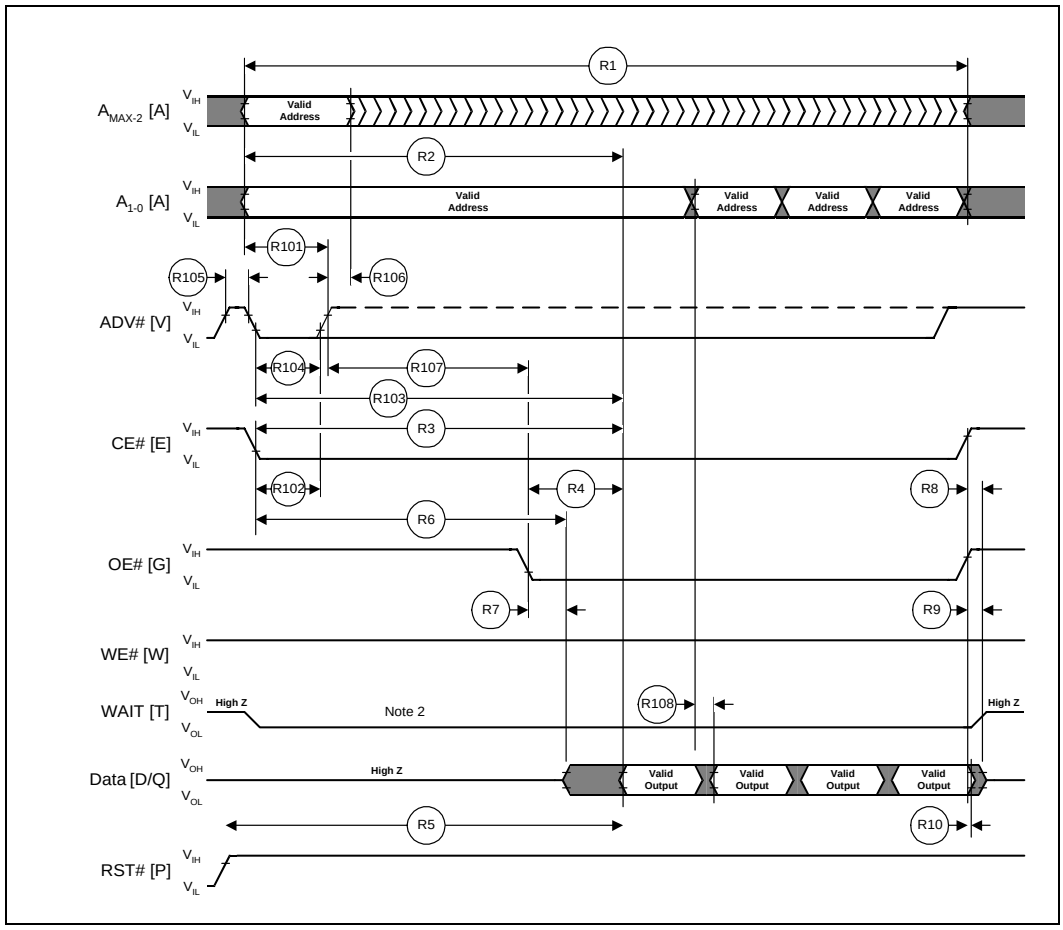


Figure 20. WAIT Signal in Synchronous Non-Read-Array Operation Waveform



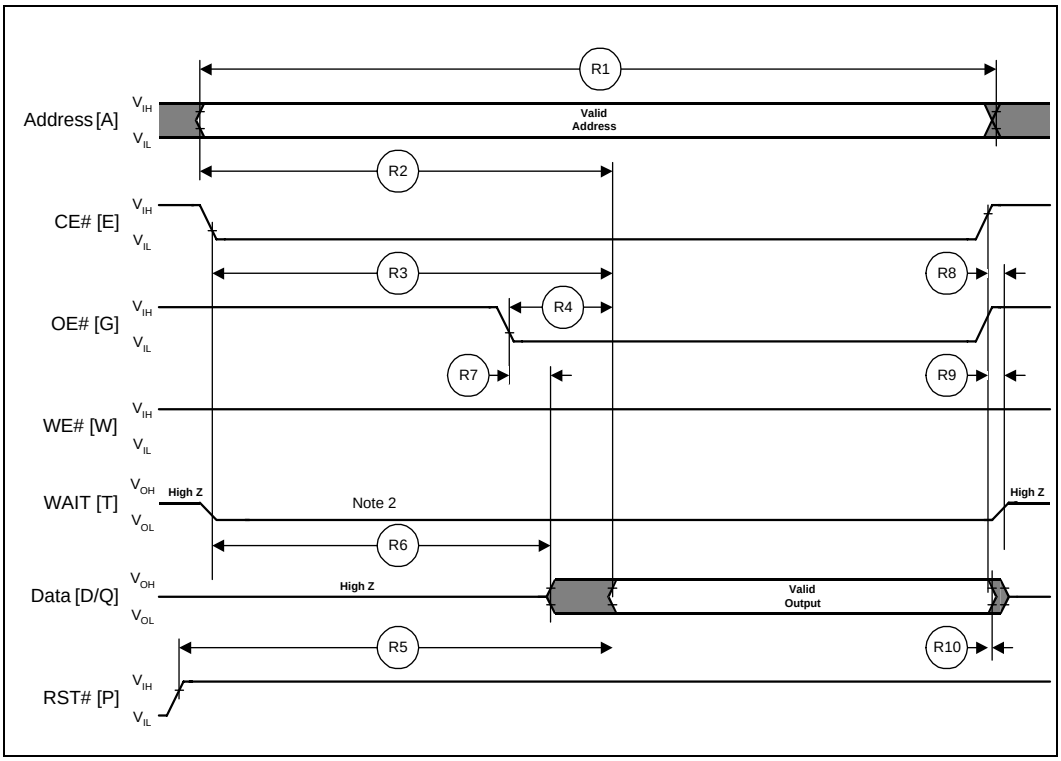
NOTES:
1. WAIT signal is in “asserted” state.
2. WAIT shown active low.

Figure 21. WAIT Signal in Asynchronous Page-Mode Read Operation Waveform



NOTES:
1. WAIT signal is in “asserted” state.
2. WAIT shown active low.

Figure 22. WAIT Signal in Asynchronous Single-Word Read Operation Waveform



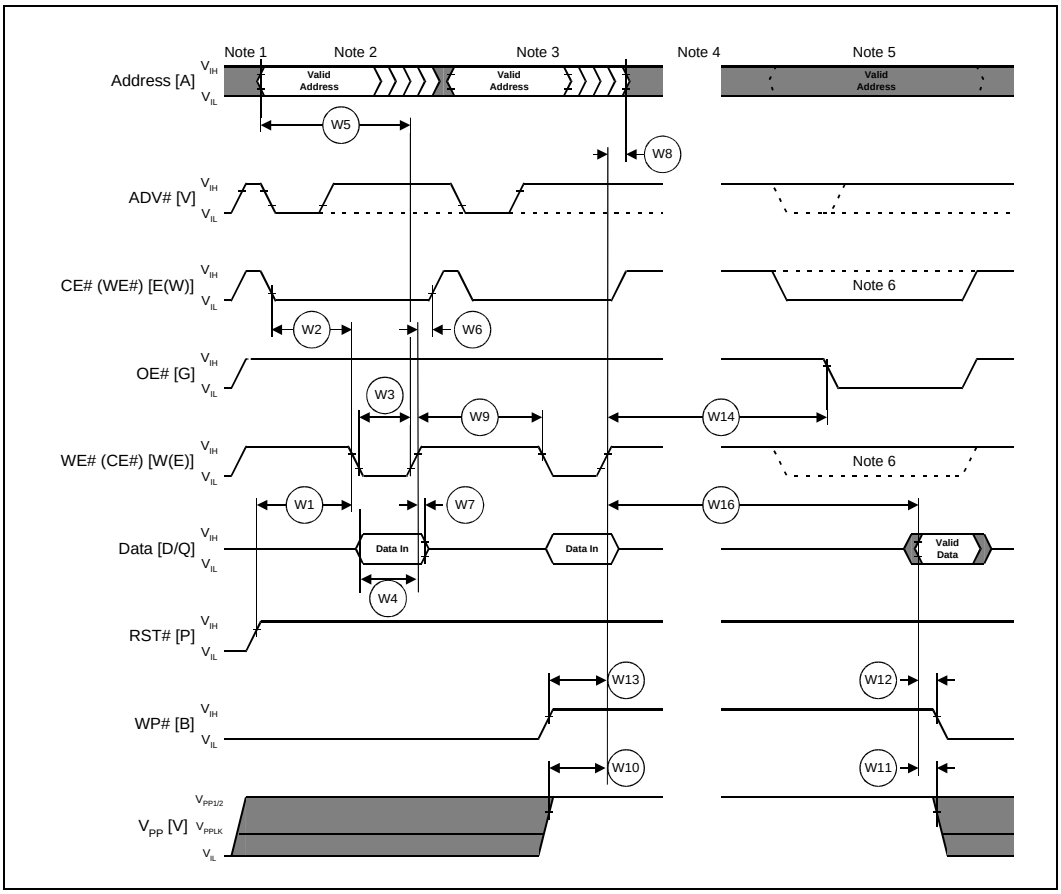
NOTES:
1. WAIT signal is in “asserted” state.
2. WAIT shown active low.

12.2 Flash Write Operations

#	Sym	Parameter [1,2]	Speed	–70		–85		Unit
			Note	Min	Max	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Low		150		150		ns
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Low		0		0		ns
W3	t_{WLWH} (t_{ELEH})	WE# (CE#) Write Pulse Width Low	4	45		60		ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) High		45		60		ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) High		45		60		ns
W6	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		0		ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		0		ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		0		ns
W9	t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5, 6, 7	25		25		ns
W10	t_{VPWH} (t_{VPEH})	V_{PP} Setup to WE# (CE#) High	3	200		200		ns
W11	t_{QVVL}	V_{PP} Hold from Valid Status Register Data	3, 8	0		0		ns
W12	t_{QVBL}	WP# Hold from Valid Status Register Data	3, 8	0		0		ns
W13	t_{BHWH} (t_{BHEH})	WP# Setup to WE# (CE#) High	3	200		200		ns
W14	t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		0		ns
W16	t_{WHQV}	WE# High to Valid Data	6	t_{AVQV} + 40		t_{AVQV} + 50		ns

NOTES:
1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first); hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever is first) to CE# or WE# low (whichever is last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
6. System designers should take this into account and may insert a software No-Op instruction to delay the first read after issuing a command.
7. For commands other than resume commands.
8. V_{PP} should be held at V_{PP1} or V_{PP2} until block erase or program success is determined.

Figure 23. Write Waveform



NOTE:

1. V_{CC} power-up and standby.
2. Write Program or Erase Setup command.
3. Write valid address and data (for program) or Erase Confirm command.
4. Automated program/erase delay.
5. Read status register data (SRD) to determine program/erase operation completion.
6. OE# and CE# must be driven active (low) and WE# must be de-asserted (high) for read operations.

12.3 Flash Program and Erase Operations

Extended Temperatures						F-V_{PP1}		F-V_{PP2}		Unit
#	Operation	Symbol	Parameter		Notes	Typ	Max	Typ	Max	
W0	Program Time	t_{WHQV1}/ t_{EHQV1}	Word	1-Word	1,2,3,4	12	150	8	130	µs
				Enhanced Factory Programming Mode	1,3,4	N/A	N/A	3.5	16	
		t_{BWPB}	Block	4-KW Parameter	1,2,3,4	0.05	0.23	0.03	0.07	s
		t_{BWMB}		32-KW Main	1,2,3,4	0.4	1.8	0.24	0.6	s
		t_{BWPB}	EFP Mode	4-KW Parameter	1,2,3,4, 5	n/a	n/a	0.015	n/a	s
		t_{BWMB}		32-KW Main	1,2,3,4, 5	n/a	n/a	0.12	n/a	s
	Erase Time	t_{WHQV2}/ t_{EHQV2}	Block	4-KW Parameter	1,2,3,4	0.3	2.5	0.25	2.5	s
				32-KW Main	1,2,3,4	0.7	4	0.4	4	s
	Suspend Latency	t_{WHRH1}/ t_{EHRH1}	Program Suspend		1,2,3,4	5	10	5	10	µs
		t_{WHRH2}/ t_{EHRH2}	Erase Suspend		1,2,3,4	9	20	9	20	
	EFP Latency	$t_{EFP-SETUP}$	EFP Setup		1,3,4	N/A	N/A	N/A	5	µs
		$t_{EFP-TRAN}$	Program to Verify Transition		1,3,4	N/A	N/A	2.7	5.6	
		$t_{EFP-VERIFY}$	Verify		1,3,4	N/A	N/A	1.7	130	

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages.
2. Excludes external system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, not 100% tested.
5. Exact results may vary based on system overhead.

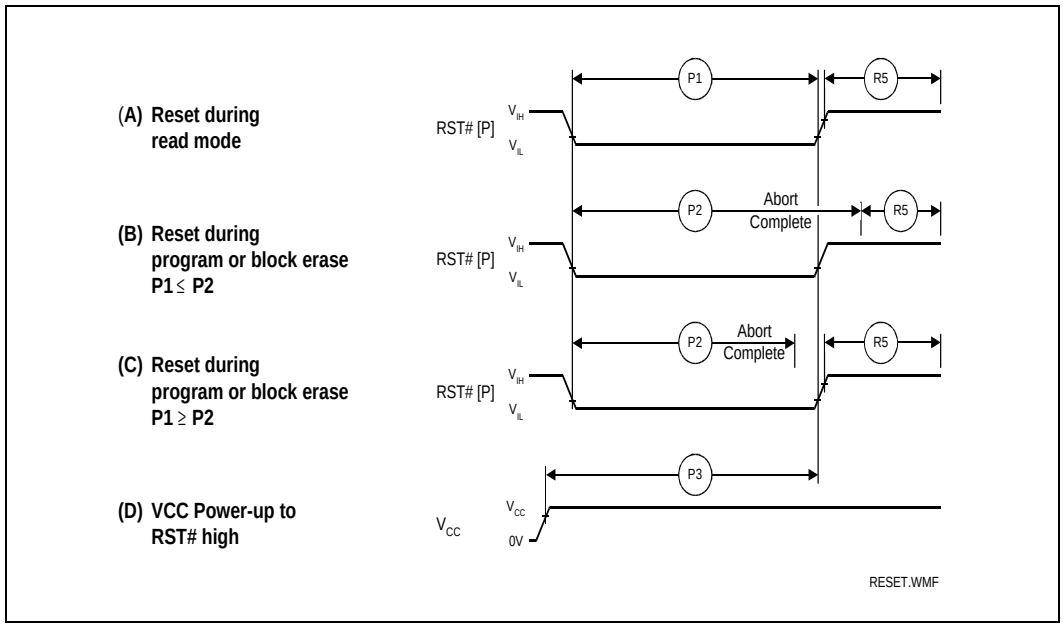
12.4 Reset Operations

#	Symbol	Parameter	Note	Min	Max	Unit
P1	t_{PLPH}	RST# Low to Reset during Read	1, 2, 3, 4	100		ns
P2	t_{PLRH}	RST# Low to Reset during Block Erase	1, 3, 4, 5		20	µs
		RST# Low to Reset during Program	1, 3, 4, 5		10	
P3	t_{VCCPH}	V_{CC} Power Valid to RST# High	1, 3, 4, 5, 6	60		

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. The device may reset if t_{PLPH} is <t_{PLPH}Min, but this is not guaranteed.
3. Not applicable if RST# is tied to V_{CC}.
4. Sampled, not 100% tested.
5. If RST# tied to V_{CC} supply, device not ready until “P3”µs after V_{CC} >=V_{CC}Min.

6. If RST# tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until after V_{CC} >=V_{CC}Min.

Figure 24. Reset Operations Waveforms



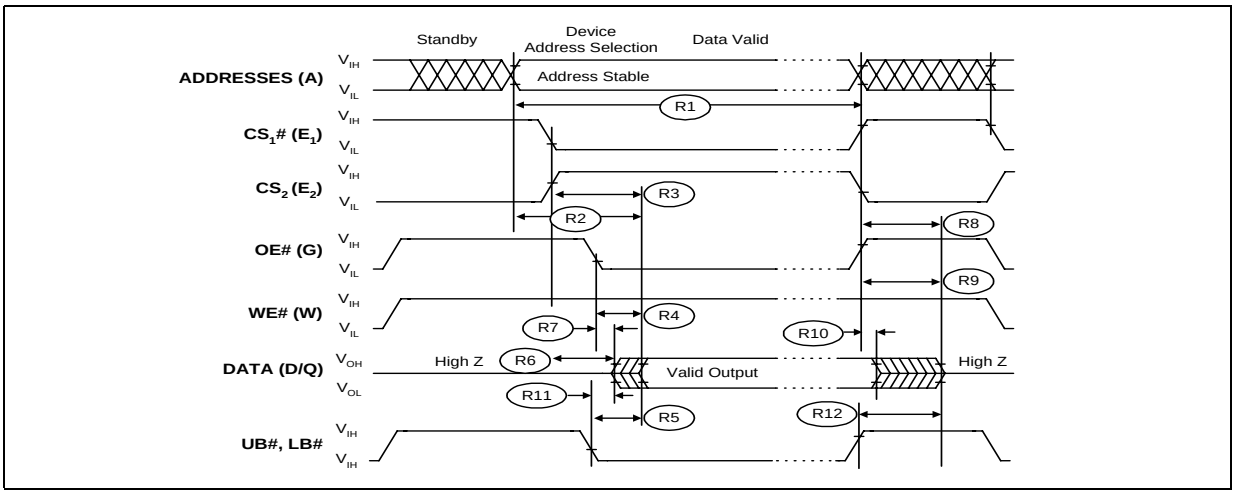
13.0 SRAM AC Characteristics

13.1 SRAM Read Operation

#	Sym	Parameter[1]	Density	4/8 Mbit				Unit
			S-V_{CC}	2.2 V – 3.3 V				
			Speed	-70		-85		
			Note	Min	Max	Min	Max	
R1	t_{RC}	Read Cycle Time		70	–	85	–	ns
R2	t_{AA}	Address to Output Delay		–	70	–	85	ns
R3	t_{CO1}, t_{CO2}	S-CS_1#, S-CS_2 to Output Delay		–	70	–	85	ns
R4	t_{OE}	S-OE# to Output Delay		–	35	–	40	ns
R5	t_{BA}	S-UB#, S-LB# to Output Delay		–	70	–	85	ns
R6	t_{LZ1}, t_{LZ2}	S-CS_1#, S-CS_2 to Output in Low-Z	2, 3	5	–	5	–	ns
R7	t_{OLZ}	S-OE# to Output in Low-Z	2	0	–	0	–	ns
R8	t_{HZ1}, t_{HZ2}	S-CS_1#, S-CS_2 to Output in High-Z	2, 3, 4	0	25	0	30	ns
R9	t_{OHZ}	S-OE# to Output in High-Z	2, 4	0	25	0	30	ns
R10	t_{OH}	Output Hold from Address, S-CS_1#, S-CS_2, or S-OE# Change, Whichever Occurs First		0	–	0	–	ns
R11	t_{BLZ}	S-UB#, S-LB# to Output in Low-Z	2	0	–	0	–	ns
R12	t_{BHZ}	S-UB#, S-LB# to Output in High-Z	2	0	25	0	30	ns

NOTE:
1. See Figure 25, “AC Waveform: SRAM Read Operation” on page 54.
2. Sampled, but not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) for a given device and from device-to-device interconnection.
4. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 25. AC Waveform: SRAM Read Operation

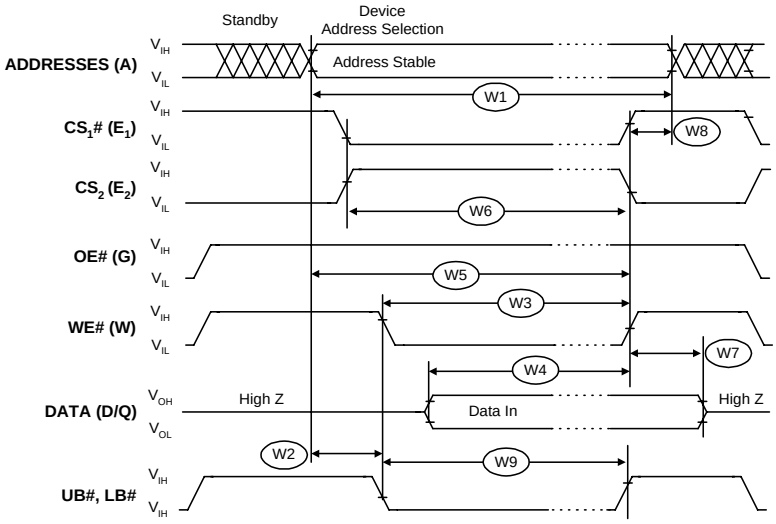


13.2 SRAM Write Operation

#	Sym	Parameter[1]	Density	4/8 Mbit				Unit
			S-V_{CC}	2.2 V – 3.3 V				
			Speed	-70		-85		
			Note	Min	Max	Min	Max	
W1	t_{WC}	Write Cycle Time	2	70	–	85	–	ns
W2	t_{AS}	Address Setup to S-WE# (S-CS_1#) and S-UB#, S-LB# Going Low	4	0	–	0	–	ns
W3	t_{WP}	S-WE# (S-CS_1#) Pulse Width	3	55	–	60	–	ns
W4	t_{DW}	Data to Write Time Overlap		30	–	35	–	ns
W5	t_{AW}	Address Setup to S-WE# (S-CS_1#) Going High		60	–	70	–	ns
W6	t_{CW}	S-SC_1# (S-WE#) Setup to S-WE# (S-CS_1#) Going High and S-SC_2 Going Low		60	–	70	–	ns
W7	t_{DH}	Data Hold Time from S-WE# (S-CS_1#) High		0	–	0	–	ns
W8	t_{WR}	Write Recovery	5	0	–	0	–	ns
W9	t_{BW}	S-UB#, S-LB# Setup to S-WE# (S-CS_1#) Going High		60	–	70	–	ns

NOTES:
1. See Figure 26, “AC Waveform: SRAM Write Operation” on page 56.
2. A write occurs during the overlap (t_{WP}) of low S-CS_1# and low S-WE#. A write begins when S-CS_1# goes low and S-WE# goes low with asserting S-UB# and S-LB# for x16 operation. S-UB# and S-LB# must be tied together to restrict x16 mode. A write ends at the earliest transition when S-CS_1# goes high and S-WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from S-CS_1# going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change; t_{WR} applied in case a write ends as S-CS_1# or S-WE# going high.

Figure 26. AC Waveform: SRAM Write Operation

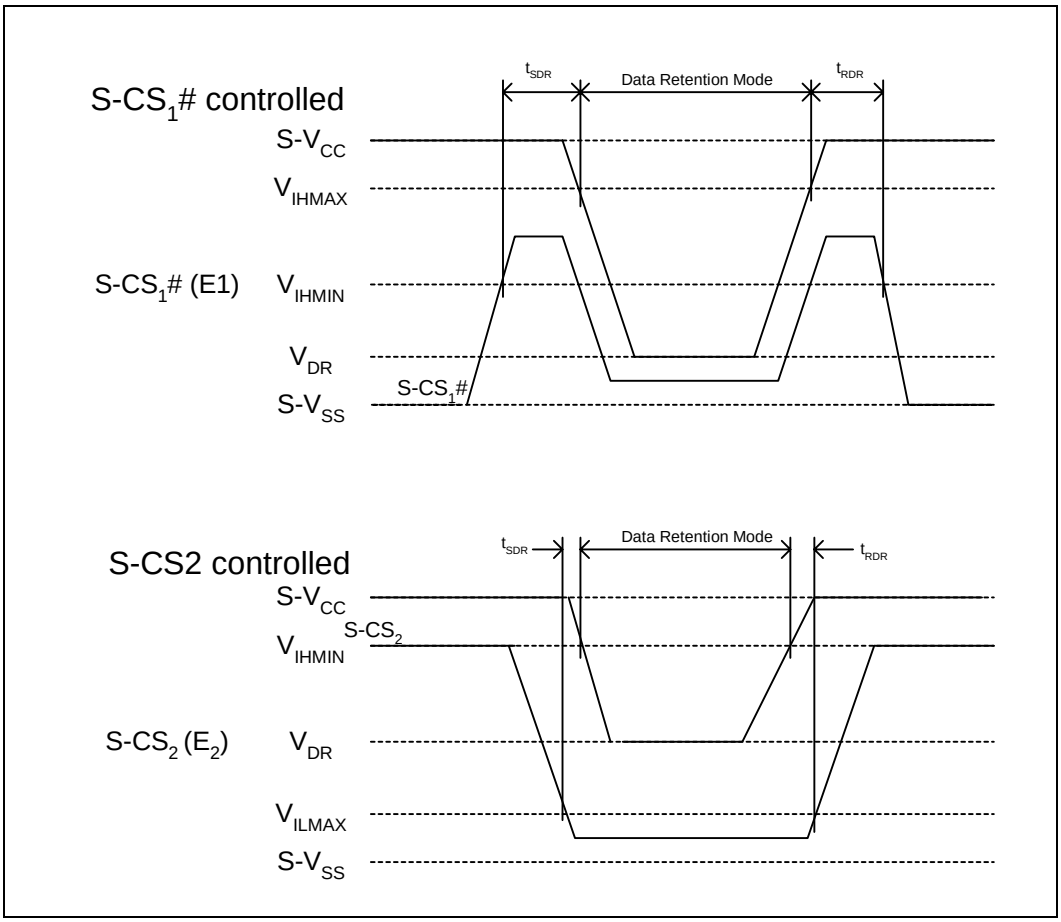


13.3 SRAM Data Retention Operation

Sym	Parameter	Device	Note	Min	Typ	Max	Unit	Test Conditions
V_{DR}	S-V_{CC} for Data Retention	4/8-Mbit	1, 2	1.5	–	3.3	V	S-CS_1# ≥ S-V_{CC} – 0.2 V
I_{DR}	Data Retention Current	4-Mbit	1, 2	–	–	5	µA	S-VCC = 1.5 V S-CS_1# ≥ S-V_{CC} – 0.2 V
		8-Mbit		–	–	25		
t_{SDR}	Data Retention Setup Time	4/8-Mbit	1	0	–	–	ns	See Data Retention Waveform
t_{RDR}	Recovery Time	4/8-Mbit	1	t_{RC}	–	–	ns	

NOTES:
1. Typical values at nominal S-V_{CC}, T_A = +25 °C.
2. S-CS_1# ≥ S-V_{CC} – 0.2 V, S-CS_2 ≥ S-V_{CC} – 0.2 V (S-CS_1# controlled) or S-CS_2 ≤ 0.2 V (S-CS_2 controlled).

Figure 27. SRAM Data Retention Waveform



14.0 Ordering Information

Figure 28. Component Ordering Breakdown

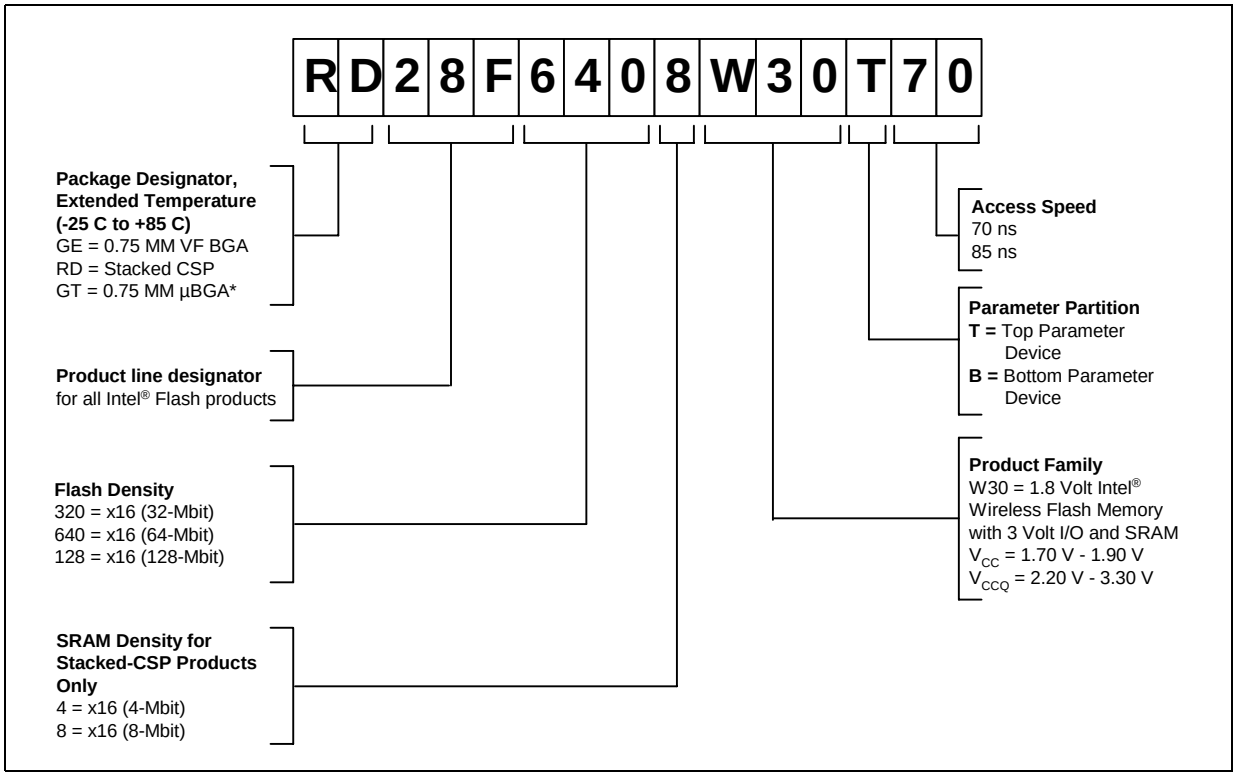


Table 17. Valid Component Combinations

	Stacked-CSP	VF BGA	µBGA*
32M	RD28F3204W30T70 RD28F3204W30B70 RD28F3204W30T85 RD28F3204W30B85	GE28F320W30T70 GE28F320W30B70 GE28F320W30T85 GE28F320W30B85	
64 M	RD28F6408W30T70 RD28F6408W30B70 RD28F6408W30T85 RD28F6408W30B85		GT28F640W30T70 GT28F640W30B70 GT28F640W30T85 GT28F640W30B85
128 M	TBD		TBD

Appendix A Flash Write State Machine (WSM)

This table shows the command state transitions based on incoming commands. Only one partition can be actively programming or erasing at a time. Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the partition's output state.

Figure 29. Write State Machine — Next State Table (Sheet 1 of 2)

***Chip* Next State after Command Input**

Write State Machine (WSM) Next State Table

Current Chip State[8]		Read Array[3] (FFH)	Program Setup[4,5] (10H/40H)	Erase Setup[4,5] (20H)	Enhanced Factory Pgm Setup[4] (30H)	BE Confirm, P/E Resume, ULB Confirm[9] (D0H)	Program/ Erase Suspend (B0H)	Read Status (70H)	Clear Status Register[6] (50H)	Read ID/Query (90H, 98H)
Ready		Ready	Program Setup	Erase Setup	EFP Setup	Ready				
Lock/CR Setup		Ready (Lock Error)				Ready	Ready (Lock Error)			
OTP	Setup	OTP Busy								
	Busy									
Program	Setup	Program Busy								
	Busy	Program Busy					Pgm Susp	Program Busy		
	Suspend	Program Suspend				Pgm Busy	Program Suspend			
Erase	Setup	Ready (Error)				Erase Busy	Ready (Error)			
	Busy	Erase Busy					Erase Susp	Erase Busy		
	Suspend	Erase Suspend	Pgm in Erase Susp Setup	Erase Suspend		Erase Busy	Erase Suspend			
Program in Erase Suspend	Setup	Program in Erase Suspend Busy								
	Busy	Program in Erase Suspend Busy					Pgm Susp in Erase Susp	Program in Erase Suspend Busy		
	Suspend	Program Suspend in Erase Suspend				Pgm in Erase Susp Busy	Program Suspend in Erase Suspend			
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)				Erase Susp	Erase Suspend (Lock Error)			
Enhanced Factory Program	Setup	Ready (Error)				EFP Busy	Ready (Error)			
	EFP Busy	EFP Busy[7]								
	EFP Verify	Verify Busy[7]								

***Output* Next State after Command Input**

Output Next State Table[1]

Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status							
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status							
OTP Busy	Array[3]	Status	Output does not change	Status	Output does not change	Status		
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp						ID/Query		

Figure 29. Write State Machine — Next State Table (Sheet 2 of 2)

Write State Machine (WSM) Next State Table

Current Chip State[8]		*Chip* Next State after Command Input: Lock, Unlock, Lock-down, CR setup[5] (60H)	OTP Setup[5] (C0H)	Lock Block Confirm[9] (01H)	Lock-Down Block Confirm[9] (2FH)	Write CR Confirm[9] (03H)	Enhanced Fact Pgm Exit (blk add <> WA0) (XXXXH)	Illegal commands or EFP data[2] (other codes)	WSM Operation Completes
Ready		Lock/CR Setup	OTP Setup	Ready					N/A
Lock/CR Setup		Ready (Lock Error)		Ready	Ready	Ready	Ready (Lock Error)		N/A
OTP	Setup	OTP Busy							N/A
	Busy	OTP Busy							Ready
Program	Setup	Program Busy							N/A
	Busy	Program Busy							Ready
	Suspend	Program Suspend							N/A
Erase	Setup	Ready (Error)							N/A
	Busy	Erase Busy						Erase Busy	Ready
	Suspend	Lock/CR Setup in Erase Susp	Erase Suspend						N/A
Program in Erase Suspend	Setup	Program in Erase Suspend Busy							N/A
	Busy	Program in Erase Suspend Busy							Erase Suspend
	Suspend	Program Suspend in Erase Suspend							N/A
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)		Erase Susp	Erase Susp	Erase Susp	Erase Suspend (Lock Error)		N/A
Enhanced Factory Program	Setup	Ready (Error)							N/A
	EFP Busy	EFP Busy[7]					EFP Verify	EFP Busy[7]	N/A
	EFP Verify	Verify Busy[7]					Ready	EFP Verify[7]	Ready

Output Next State Table[1]

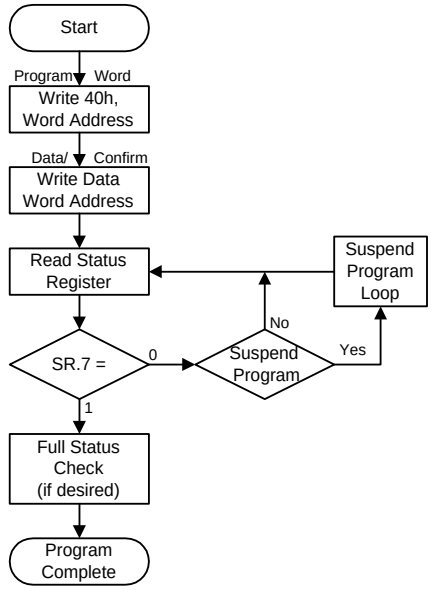
	Output Next State after Command Input						
Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status						Output does not change
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status				Array	Status	
OTP Busy	Status	Output does not change			Array	Output does not change	
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp							

NOTES:

1. The output state shows the type of data that appears at the outputs if the partition address is the same as the command address. A partition can be placed in Read Array, Read Status or Read ID/CFI, depending on the command issued. Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the partition's output state. For example, if partition #1's output state is Read Array and partition #4's output state is Read Status, every read from partition #4 (without issuing a new command) outputs the Status register.
2. Illegal commands are those not defined in the command set.
3. All partitions default to Read Array mode at power-up. A Read Array command issued to a busy partition results in undermined data when a partition address is read.
4. Both cycles of 2-cycle commands should be issued to the same partition address. If they are issued to different partitions, the second write determines the active partition. Both partitions will output status information when read.
5. If the WSM is active, both cycles of a 2-cycle command are ignored. This differs from previous Intel devices.
6. The Clear Status command clears status register error bits except when the WSM is running (Pgm Busy, Erase Busy, Pgm Busy In Erase Suspend, OTP Busy, EFP modes) or suspended (Erase Suspend, Pgm Suspend, Pgm Suspend In Erase Suspend).
7. EFP writes are allowed only when status register bit SR.0 = 0. EFP is busy if Block Address = address at EFP Confirm command. Any other commands are treated as data.
8. The "current state" is that of the WSM, not the partition.
9. Confirm commands (Lock Block, Unlock Block, Lock-down Block, Configuration Register) perform the operation and then move to the Ready State.

Appendix B Flowcharts

Figure 30. Programming Flowchart

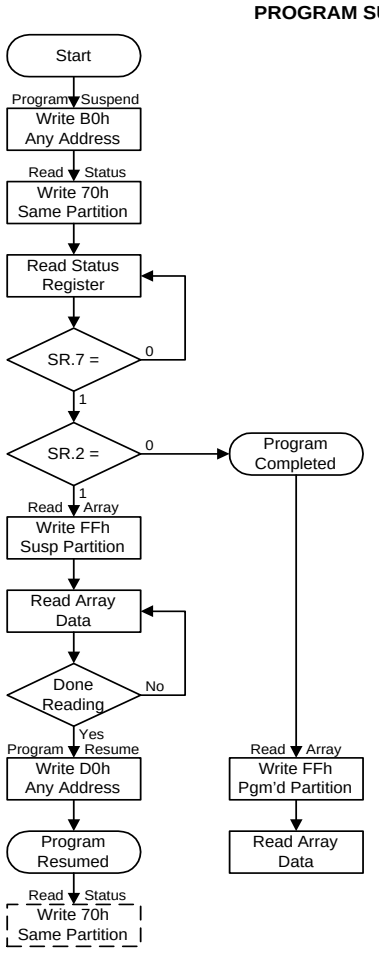


Bus Operation	Command	Comments
Write	Program Setup	Data = 40h Addr = Location to program (WA)
Write	Data	Data = Data to program (WD) Addr = Location to program (WA)
Read		Status register data. Toggle CE# or OE# to update Status register
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Repeat for subsequent programming operations. Full Status register check can be done after each program or after a sequence of program operations. Write FFh after the last operation to enter read array mode.		

Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} error
Standby		Check SR.4 1 = Data program error
Standby		Check SR.1 1 = Attempted program to locked block Program aborted
SR.3 MUST be cleared before the Write State Machine will allow further program attempts Only the Clear Staus Register command clears SR.1, 3, 4. If an error is detected, clear the status register before attempting a program retry or other error recovery.		

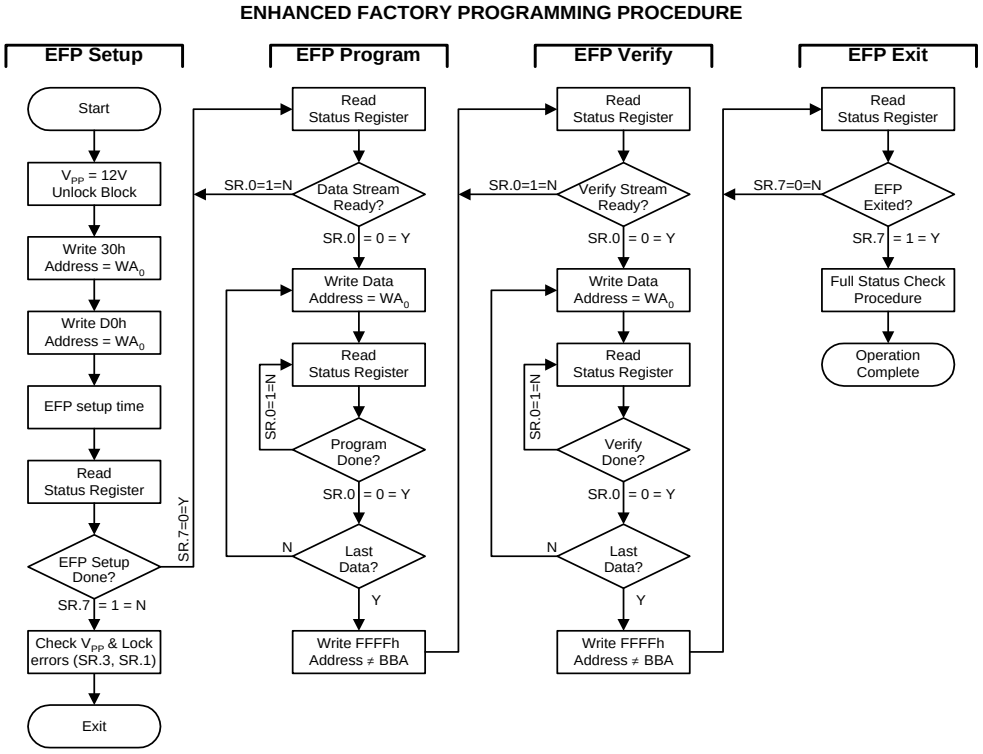
PGM_WRD.WMF

Figure 31. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0h Addr = Block to suspend (BA)
Write	Read Status	Data = 70h Addr = Same partition
Read		Status register data Toggle CE# or OE# to update Status register Addr = Suspended block (BA)
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FFh Addr = Block address to read (BA)
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = D0h Addr = Suspended block (BA)
If the suspended partition was placed in Read Array mode:		
Write	Read Status	Return partition to Status mode: Data = 70h Addr = Same partition

Figure 32. Enhanced Factory Program Flowchart



EFP Setup		
Bus State		**Comments**
Write	Unlock Block	V_{PP} = 12V Unlock block
Write	EFP Setup	Data = 30h Address = WA_0
Write	EFP Confirm	Data = D0h Address = WA_0
Standby	Setup Time	Refer to Program and Erase Operations Table.
Read		Status Register
Standby	EFP Setup Done?	Check SR.7 0 = EFP ready 1 = EFP not ready
Standby	Error Condition Check	If SR.7 = 1: Check SR.3, SR.1 SR.3 = 1 = V_{PP} error SR.1 = 1 = locked block

EFP Program		
Bus State		**Comments**
Read		Status Register
Standby	Data Stream Ready?	Check SR.0 0 = Ready for data 1 = Not ready for data
Write (note 1)		Data = Data to program Address = WA_0
Read		Status Register
Standby	Program Done?	Check SR.0 0 = Program done 1 = Program not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Program Phase	Data = FFFFh Address not within same BBA

EFP Verify		
Bus State		**Comments**
Read		Status Register
Standby	Verify Stream Ready?	Check SR.0 0 = Ready for verify 1 = Not ready for verify
Write (note 2)		Data = Word to verify Address = WA_0
Read		Status Register
Standby (note 3)	Verify Done?	Check SR.0 0 = Verify done 1 = Verify not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Verify Phase	Data = FFFFh Address not within same BBA

EFP Exit		
Read		Status Register
Standby	EFP Exited?	Check SR.7 0 = Exit not finished 1 = Exit completed
Repeat for subsequent operations. After EFP exit, a Full Status Check can determine if any program error occurred. See the Full Status Check procedure in the Word Program flowchart.		

1. WA_0 = first Word Address to be programmed within the target block. The BBA (Block Base Address) must remain constant throughout the program phase data stream; WA can be held constant at the first address location, or it can be written to sequence up through the addresses within the block. Writing to a BBA not equal to that of the block currently being written to terminates the EFP program phase, and instructs the device to enter the EFP verify phase.
2. For proper verification to occur , the verify data stream must be presented to the device in the same sequence as that of the program phase data stream. Writing to a BBA not equal to WA terminates the EFP verify phase, and instructs the device to exit EFP .
3. Bits that did not fully program with the single WSM pulse of the EFP program phase receive additional program-pulse attempts during the EFP verify phase. The device will report any program failure by setting SR.4=1; this check can be performed during the full status check after EFP has been exited for that block, and will indicate any error within the entire data stream.

Figure 33. Block Erase Flowchart

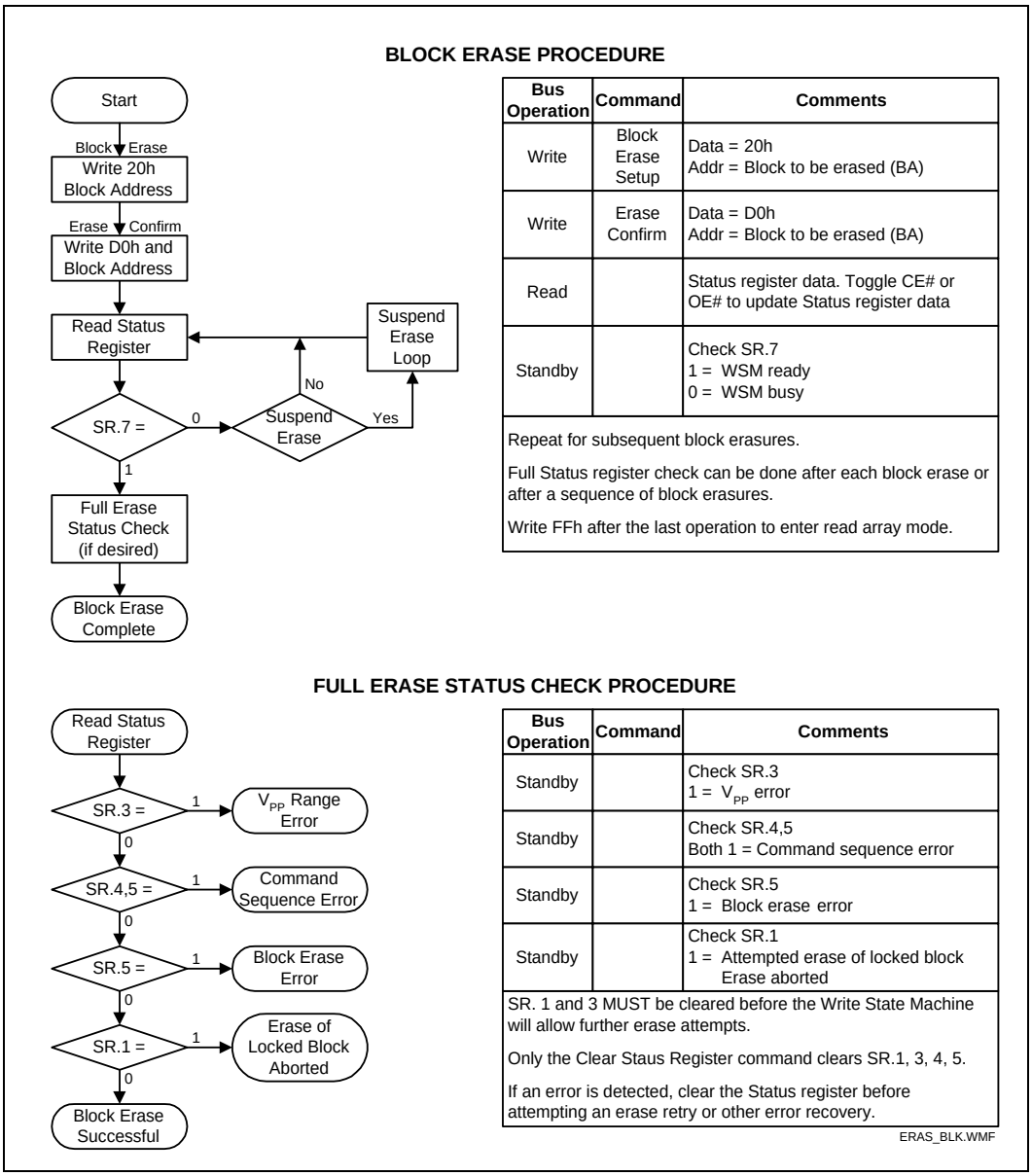
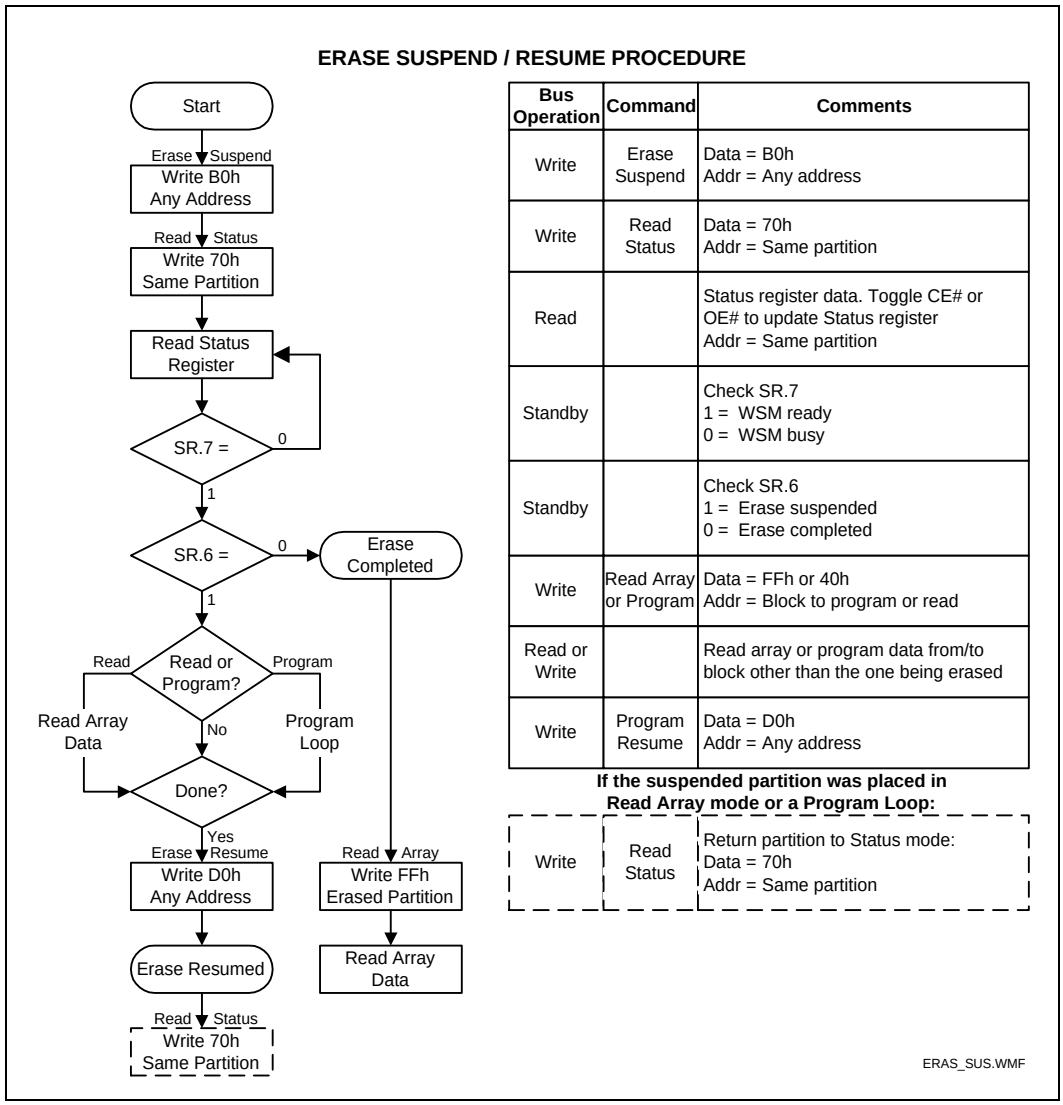
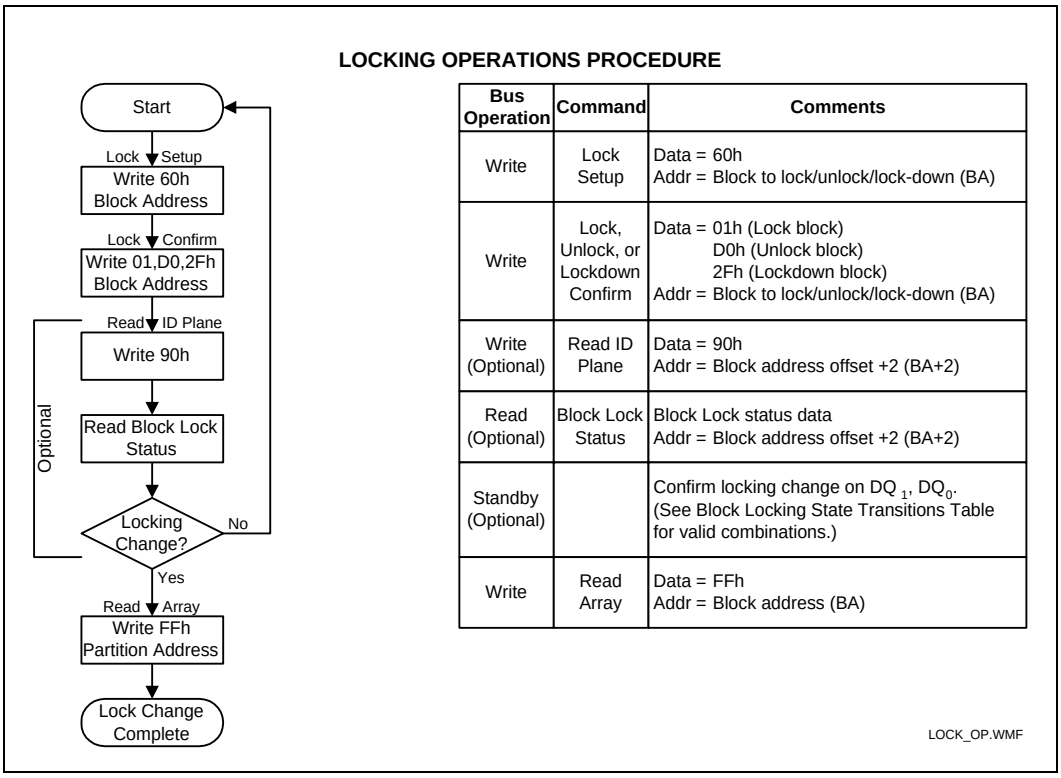


Figure 34. Erase Suspend/Resume Flowchart



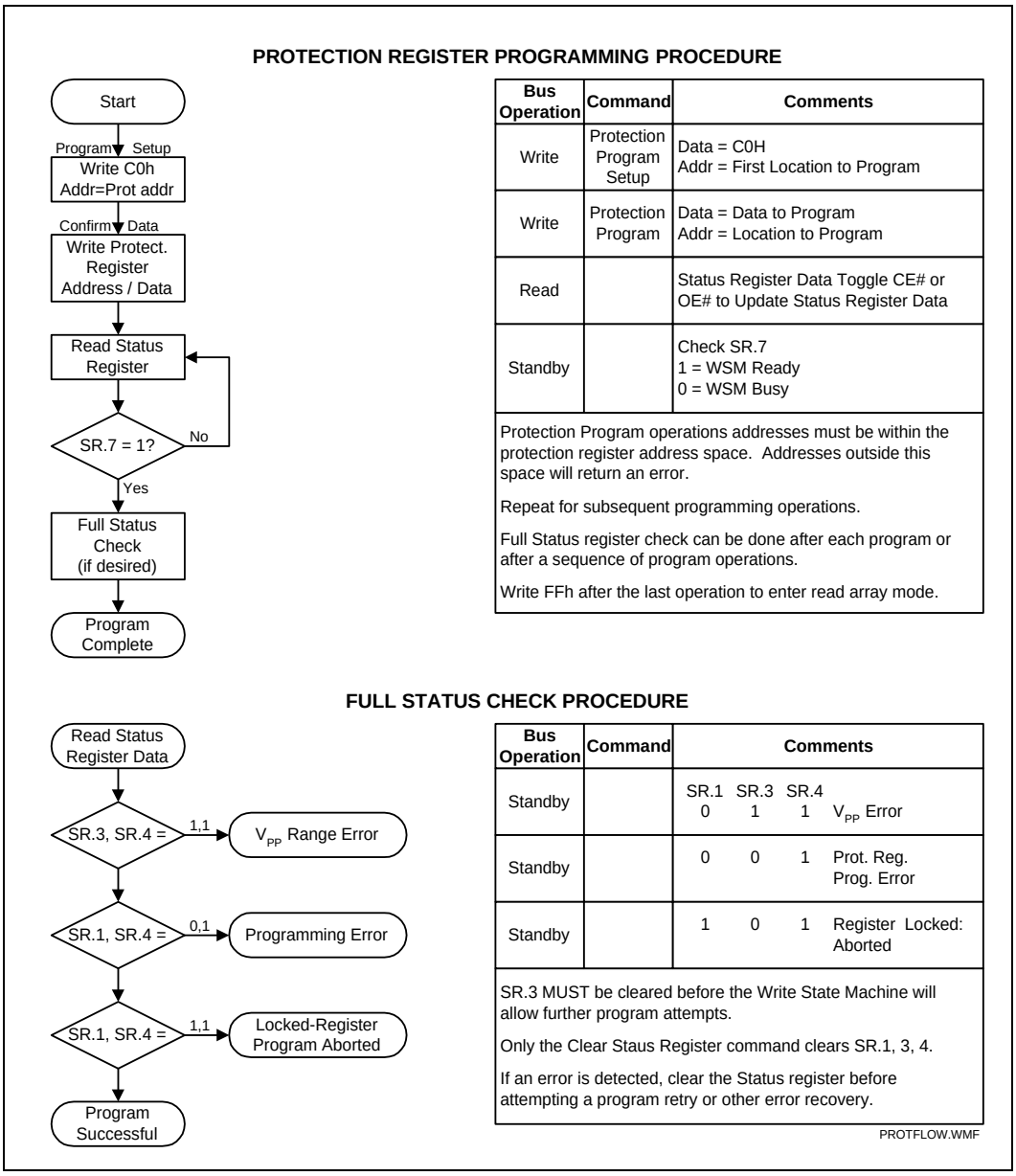
Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0h Addr = Any address
Write	Read Status	Data = 70h Addr = Same partition
Read		Status register data. Toggle CE# or OE# to update Status register Addr = Same partition
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.6 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = FFh or 40h Addr = Block to program or read
Read or Write		Read array or program data from/to block other than the one being erased
Write	Program Resume	Data = D0h Addr = Any address
If the suspended partition was placed in Read Array mode or a Program Loop:		
Write	Read Status	Return partition to Status mode: Data = 70h Addr = Same partition

Figure 35. Locking Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 60h Addr = Block to lock/unlock/lock-down (BA)
Write	Lock, Unlock, or Lockdown Confirm	Data = 01h (Lock block) D0h (Unlock block) 2Fh (Lockdown block) Addr = Block to lock/unlock/lock-down (BA)
Write (Optional)	Read ID Plane	Data = 90h Addr = Block address offset +2 (BA+2)
Read (Optional)	Block Lock Status	Block Lock status data Addr = Block address offset +2 (BA+2)
Standby (Optional)		Confirm locking change on DQ_1, DQ_0. (See Block Locking State Transitions Table for valid combinations.)
Write	Read Array	Data = FFh Addr = Block address (BA)

Figure 36. Protection Register Programming Flowchart



Appendix C Common Flash Interface

This appendix defines the data structure or "database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

C.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the device's CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (DQ0-7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two Query-structure bytes, ASCII "Q" and "R," appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes. The device outputs ASCII "Q" in the low byte (DQ_{0-7}) and 00h in the high byte (DQ_{8-15}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table C1. Summary of Query Structure Output as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII Value
Device Addresses	00010:	51	"Q"
	00011:	52	"R"
	00012:	59	"Y"

Table C2. Example of Query Structure Output of x16- and x8 Devices

Word Addressing:			Byte Addressing:		
Offset	Hex Code	Value	Offset	Hex Code	Value
A –A	D –D		A –A	D –D	
00010h	0051	"Q"	00010h	51	"Q"
00011h	0052	"R"	00011h	52	"R"
00012h	0059	"Y"	00012h	59	"Y"
00013h	P_ID	PrVendor	00013h	P_ID	PrVendor
00014h	P_ID	ID #	00014h	P_ID	ID #
00015h	P	PrVendor	00015h	P_ID	ID #
00016h	P	TblAdr	00016h	...	...
00017h	A_ID_{LO}	AltVendor	00017h		
00018h	A_ID_{HI}	ID #	00018h		
...	...	...	...		

C.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The structure subsections and address locations are summarized below.

Table C3. Query Structure

Offset	Sub-Section Name	(1)
00000h		Manufacturer Code
00001h		Device Code
(2)	Block Status register	Block-specific information
00004-Fh	Reserved	Reserved for vendor-specific information
00010h	CFI query identification string	Command set ID and vendor data offset
0001Bh	System interface information	Device timing & voltage information
00027h	Device geometry definition	Flash device layout
P(3)	Primary Intel-specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

NOTES:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block Address beginning location (i.e., 08000h is block 1's beginning location when the block size is 32K-word).
3. Offset 15 defines "P" which points to the Primary Intel-specific Extended Query Table.

C.3 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. BSR.1 can be used just after power-up to verify that the V_{CC} supply was not accidentally removed during an erase operation. Only issuing another operation to the block resets this bit. The Block Status Register is accessed from word address 02h within each block.

Table C4. Block Status Register

Offset	Length	Description	Add.	Value
(BA+2)h(1)	1	Block Lock Status Register	BA+2	--00 or --01
		BSR.0 Block lock status 0 = Unlocked 1 = Locked	BA+2	(bit 0): 0 or 1
		BSR.1 Block lock-down status 0 = Not locked down 1 = Locked down	BA+2	(bit 1): 0 or 1
		BSR 2–7: Reserved for future use	BA+2	(bit 2–7): 0

NOTE: BA = The beginning location of a Block Address (i.e., 008000h is block 1's (64KB block) beginning location in word mode).

C.4 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table C5. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string “QRY“	10: 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--03 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--39 --00	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

Table C6. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--19	1.9V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--B4	11.4V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--C6	12.6V
1Fh	1	“n” such that typical single word program time-out = 2^n µ-sec	1F:	--04	16µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µ-sec	20:	--00	NA
21h	1	“n” such that typical block erase time-out = 2^n m-sec	21:	--0A	1s
22h	1	“n” such that typical full chip erase time-out = 2^n m-sec	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--04	256µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--00	NA
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--03	8s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

C.5 Device Geometry Definition

Table C7. Device Geometry Definition

Offset	Length	Description	Code		
27h	1	"n" such that device size = 2^n in number of bytes	27:	See table below	
28h	2	Flash device interface code assignment: "n" such that n+1 specifies the bit field that represents the flash device width capabilities as described in the table: 7 6 5 4 3 2 1 0 x1K x512 x256 x128 x64 x32 x16 x8 15 14 13 12 11 10 9 8 — — — — — — — —	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--00 --00	0
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2C:	See table below	
2Dh	4	Erase Block Region 1 Information - Bottom paramenter device Erase Block Region x-3 Information - Top Paramenter device bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:	See table below	
31h	4	Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	31: 32: 33: 34:	See table below	
35h	4	Erase Block Region 3-x Information for Bottom parameter device Erase Block Region 1 Information for Top paramenter device bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	35: 36: 37: 38:	See table below	

Address	16 Mbit		32 Mbit		64 Mbit		128 Mbit	
	–B	–T	–B	–T	–B	–T	–B	–T
27:	--15	--15	--16	--16	--17	--17	--18	--18
28:	--01	--01	--01	--01	--01	--01	--01	--01
29:	--00	--00	--00	--00	--00	--00	--00	--00
2A:	--00	--00	--00	--00	--00	--00	--00	--00
2B:	--00	--00	--00	--00	--00	--00	--00	--00
2C:	--05	--05	--09	--09	--11	--11	--21	--21
2D:	--07	--07	--07	--07	--07	--07	--07	--07
2E:	--00	--00	--00	--00	--00	--00	--00	--00
2F:	--20	--00	--20	--00	--20	--00	--20	--00
30:	--00	--01	--00	--01	--00	--01	--00	--01
31:	--06	--06	--06	--06	--06	--06	--06	--06
32:	--00	--00	--00	--00	--00	--00	--00	--00
33:	--00	--00	--00	--00	--00	--00	--00	--00
34:	--01	--01	--01	--01	--01	--01	--01	--01
35:	--07	--07	--07	--07	--07	--07	--07	--07
36:	--00	--00	--00	--00	--00	--00	--00	--00
37:	--00	--20	--00	--20	--00	--20	--00	--20
38:	--01	--00	--01	--00	--01	--00	--01	--00

C.6 Intel-Specific Extended Query Table

Table C8. Primary Vendor-Specific Extended Query

(1) P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	39:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	3A:	--52	"R"
(P+2)h			3B:	--49	"I"
(P+3)h	1	Major version number, ASCII	3C:	--31	"1"
(P+4)h	1	Minor version number, ASCII	3D:	--33	"3"
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	3E:	--E6	
(P+6)h		*bits 10–31 are reserved; undefined bits are "0." If bit 31 is*	3F:	--03	
(P+7)h		*"1" then another 31 bit field of Optional features follows at*	40:	--00	
(P+8)h		*the end of the bit–30 field.*	41:	--00	
		bit 0 Chip erase supported	bit 0	= 0	No
		bit 1 Suspend erase supported	bit 1	= 1	Yes
		bit 2 Suspend program supported	bit 2	= 1	Yes
		bit 3 Legacy lock/unlock supported	bit 3	= 0	No
		bit 4 Queued erase supported	bit 4	= 0	No
		bit 5 Instant individual block locking supported	bit 5	= 1	Yes
		bit 6 Protection bits supported	bit 6	= 1	Yes
		bit 7 Pagemode read supported	bit 7	= 1	Yes
		bit 8 Synchronous read supported	bit 8	= 1	Yes
		bit 9 Simultaneous operations supported	bit 9	= 1	Yes
(P+9)h	1	Supported functions after suspend: read Array, Status, Query	42:	--01	
		Other supported operations are:			
		bits 1–7 reserved; undefined bits are "0"			
		bit 0 Program supported after erase suspend	bit 0	= 1	Yes
(P+A)h	2	Block status register mask	43:	--03	
(P+B)h		*bits 2–15 are Reserved; undefined bits are "0"*	44:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0	= 1	Yes
		bit 1 Block Lock-Down Bit Status active	bit 1	= 1	Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage	45:	--18	1.8V
		bits 0–3 BCD value in 100 mV			
(P+D)h	1	V_{PP} optimum program/erase supply voltage	46:	--C0	12.0V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 HEX value in volts			

Table C9. Protection Register Information

(1) P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection fields are available	47:	--01	1
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0–7 = Lock/bytes Jedec-plane physical low address bits 8–15 = Lock/bytes Jedec-plane physical high address bits 16–23 = "n" such that 2n = factory pre-programmed bytes bits 24–31 = "n" such that 2n = user programmable bytes	48: 49: 4A: 4B:	--80 --00 --03 --03	80h 00h 8 byte 8 byte

Table C10. Burst Read Information

(1) P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no	4C:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	4D:	--03	3
(P+15)h	1	Synchronous mode read capability configuration 1 Bits 3–7 = Reserved bits 0–2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the Read Configuration Register bits 0–2 if the device is configured for its maximum word width. See offset 28h for	4E:	--01	4
(P+16)h	1	Synchronous mode read capability configuration 2	4F:	--02	8
(P+17)h	1	Synchronous mode read capability configuration 3	50:	--07	Cont

Table C11. Partition and Erase-block Region Information

Bottom (1) P = 39h	Top (1) P = 39h	Description (Optional flash features and commands)	See table below		
			Len	Address Bot	Address Top
(P+18)h	(P+18)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	51:	51:

Partition Region 1 Information

P = 39h[1] Bottom	P = 39h[1] Top	Description (Optional flash features and commands)	See table below: Len	See table below: Address Bot	See table below: Address Top
(P+19)h (P+1A)h	(P+19)h (P+1A)h	Number of identical partitions within the partition region	2	52: 53:	52: 53:
(P+1B)h	(P+1B)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Read mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	54:	54:
(P+1C)h	(P+1C)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	55:	55:
(P+1D)h	(P+1D)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	56:	56:
(P+1E)h	(P+1E)h	Partitions' erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in "bulk" x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one	1	57:	57:
(P+1F)h (P+20)h (P+21)h (P+22)h	(P+1F)h (P+20)h (P+21)h (P+22)h	Partition Region 1 Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	58: 59: 5A: 5B:	58: 59: 5A: 5B:
(P+23)h (P+24)h	(P+23)h (P+24)h	Partition 1 (Erase Region 1) Minimum block erase cycles x 1000	2	5C: 5D:	5C: 5D:
(P+25)h	(P+25)h	Partition 1 (erase region 1) bits per cell; internal error correction bits 0–3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1=yes, 0=no) bits 5–7 = reserve for future use	1	5E:	5E:
(P+26)h	(P+26)h	Partition 1 (erase region 1) page mode and synchronous mode capabilities defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no)	1	5F:	5F:
(P+27)h (P+28)h (P+29)h (P+2A)h		Partition Region 1 Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes (bottom parameter device only)	4	60: 61: 62: 63:	
(P+2B)h (P+2C)h		Partition 1 (Erase Region 2) minimum block erase cycles x 1000 (bottom parameter device only)	2	64: 65:	
(P+2D)h		Partition 1 (Erase Region 2) bits per cell (bottom parameter device only) bits 0–3 = bits per cell in erase region bit 4 = reserved for "internal ECC used" (1=yes, 0=no) bits 5–7 = reserve for future use	1	66:	
(P+2E)h		Partition 1 (Erase Region 2) pagemode and synchronous mode capabilities defined in Table 10 (bottom parameter device only) bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no)	1	67:	

Partition Region 2 Information

P = 39h[1] Bottom	P = 39h[1] Top	Description (Optional flash features and commands)	See table below: Len	See table below: Address Bot	See table below: Address Top
(P+2F)h (P+30)h	(P+27)h (P+28)h	Number of identical partitions within the partition region	2	68: 69:	60: 61:
(P+31)h	(P+29)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Read mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6A:	62:
(P+32)h	(P+2A)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6B:	63:
(P+33)h	(P+2B)h	Simultaneous program and erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6C:	64:
(P+34)h	(P+2C)h	Partitions' erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in “bulk” x = number of erase block regions w/ contiguous same-size	1	6D:	65:
(P+35)h (P+36)h (P+37)h (P+38)h	(P+2D)h (P+2E)h (P+2F)h (P+30)h	Partition Region 2 Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	6E: 6F: 70: 71:	66: 67: 68: 69:
(P+39)h (P+3A)h	(P+31)h (P+32)h	Partition 2 (Erase Region 1) Minimum block erase cycles x 1000	2	72: 73:	6A: 6B:
(P+3B)h	(P+33)h	Partition 2 (Erase Region 1) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	74:	6C:
(P+3C)h	(P+34)h	Partition 2 (erase region 1) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no)	1	75:	6D:
	(P+35)h (P+36)h (P+37)h (P+38)h	Partition Region 2 Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes (top parameter device only)	4		6E: 6F: 70: 71:
	(P+39)h (P+3A)h	Partition 2 (Erase Region 2) minimum block erase cycles x 1000 (top parameter device only)	2		72: 73:
	(P+3B)h	Partition 2 (Erase Region 2) bits per cell (top parameter only) bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1		74:
	(P+3C)h	Partition 2 (Erase Region 2) pagemode and synchronous mode capabilities as defined in Table 10. (top parameter only) bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no)	1		75:
(P+3D)h	(P+3D)h	Features Space definitions (Reserved for future use)	TBD	76:	76:
(P+3E)h	(P+3E)h	Reserved for future use	Resv'd	77:	77:

Partition and Erase-block Region Information

Address	16 Mbit		32 Mbit		64Mbit		128Mbit	
	–B	–T	–B	–T	–B	–T	–B	–T
51:	--02	--02	--02	--02	--02	--02	--02	--02
52:	--01	--03	--01	--07	--01	--0F	--01	--1F
53:	--00	--00	--00	--00	--00	--00	--00	--00
54:	--01	--01	--01	--01	--01	--01	--01	--01
55:	--00	--00	--00	--00	--00	--00	--00	--00
56:	--00	--00	--00	--00	--00	--00	--00	--00
57:	--02	--03	--02	--07	--02	--F	--02	--1F
58:	--07	--07	--07	--07	--07	--07	--07	--07
59:	--00	--00	--00	--00	--00	--00	--00	--00
5A:	--20	--00	--20	--00	--20	--00	--20	--00
5B:	--00	--01	--00	--01	--00	--01	--00	--01
5C:	--64	--64	--64	--64	--64	--64	--64	--64
5D:	--00	--00	--00	--00	--00	--00	--00	--00
5E:	--01	--01	--01	--01	--01	--01	--01	--01
5F:	--02	--03	--02	--03	--02	--03	--02	--03
60:	--06	--01	--06	--01	--06	--01	--06	--01
61:	--00	--00	--00	--00	--00	--00	--00	--00
62:	--00	--01	--00	--01	--00	--01	--00	--01
63:	--01	--00	--01	--00	--01	--00	--01	--00
64:	--64	--00	--64	--00	--64	--00	--64	--00
65:	--00	--02	--00	--02	--00	--02	--00	--02
66:	--01	--06	--01	--06	--01	--06	--01	--06
67:	--03	--00	--03	--00	--03	--00	--03	--00
68:	--03	--00	--07	--00	--0F	--00	--1F	--00
69:	--00	--01	--00	--01	--00	--01	--00	--01
6A:	--01	--64	--01	--64	--01	--64	--01	--64
6B:	--00	--00	--00	--00	--00	--00	--00	--00
6C:	--00	--01	--00	--01	--00	--01	--00	--01
6D:	--03	--03	--07	--03	--F	--03	--1F	--03
6E:	--07	--07	--07	--07	--07	--07	--07	--07
6F:	--00	--00	--00	--00	--00	--00	--00	--00
70:	--00	--20	--00	--20	--00	--20	--00	--20
71:	--01	--00	--01	--00	--01	--00	--01	--00
72:	--64	--64	--64	--64	--64	--64	--64	--64
73:	--00	--00	--00	--00	--00	--00	--00	--00
74:	--01	--01	--01	--01	--01	--01	--01	--01
75:	--03	--02	--03	--02	--03	--02	--03	--02

NOTES:

1. The variable P is a pointer which is defined at CFI offset 15h.
2. For a 16Mb the 1.8 Volt Intel® Wireless Flash memory z1 = 0100h = 256 ⇒ 256 * 256 = 64K, y1 = 17h = 23d ⇒ y1+1 = 24 ⇒
   24 * 64K = 1½MB ⇒ Partition 2's offset is 0018 0000h bytes (000C 0000h words).
3. TPD - Top parameter device; BPD - Bottom parameter device.
4. Partition: Each partition is 4Mb in size. It can contain main blocks OR a combination of both main and parameter blocks.
5. Partition Region: Symmetrical partitions form a partition region. (there are two partition regions, A. contains all the partitions that are made up of main blocks only. B. contains the partition that is made up of the parameter and the main blocks.