CMOS 18-BIT TTL/GTLP UNIVERSAL BUS TRANSCEIVER

IDT74GTLP16612
PRELIMINARY

FEATURES:

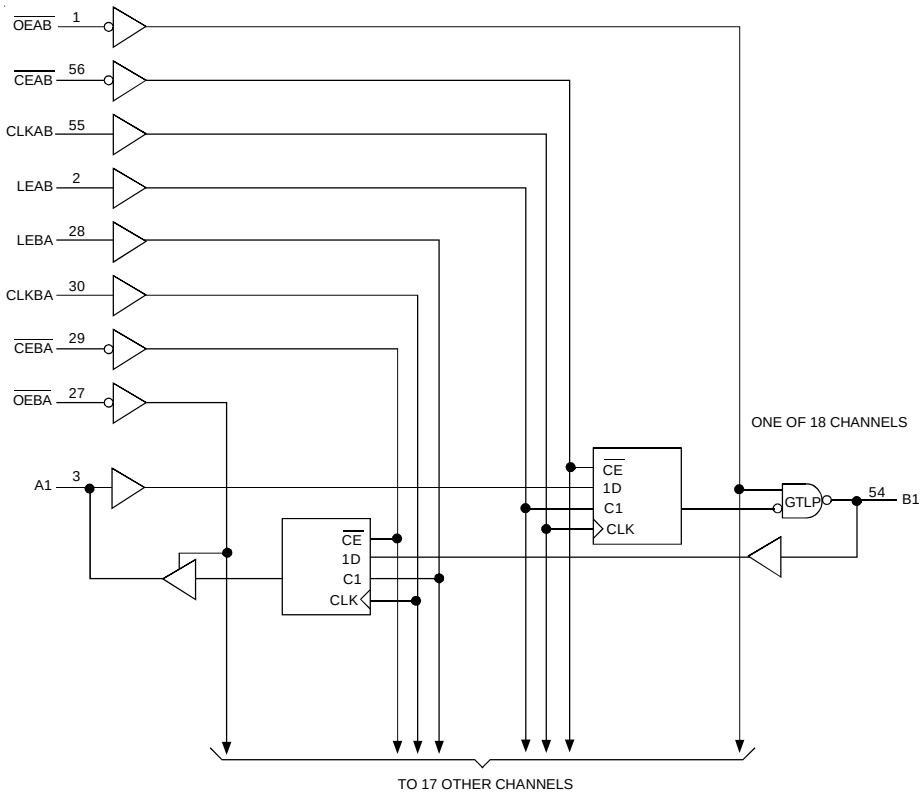
- **Bidirectional interface between GTLP and TTL logic levels**
- **Edge Rate Control Circuit reduces output noise**
- **VREF pin provides reference voltage for receiver threshold**
- **CMOS technology for low power dissipation**
- **Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage, and temperature**
- **5V tolerant inputs and outputs on A-Port**
- **Bus-Hold to eliminate the need for external pull-up resistors for unused inputs to A-Port**
- **Power up/down high-impedance**
- **TTL-compatible Driver and Control inputs**
- **High Output source/sink ±32mA on A-Port pins**
- **Flow-through architecture optimizes system layout**
- **D-type latch and flip-flop architecture for data flow in clocked, transparent, or latched mode**
- **Open drain on GTLP to support wired OR connection**
- **Available in SSOP and TSSOP packages**

DESCRIPTION:

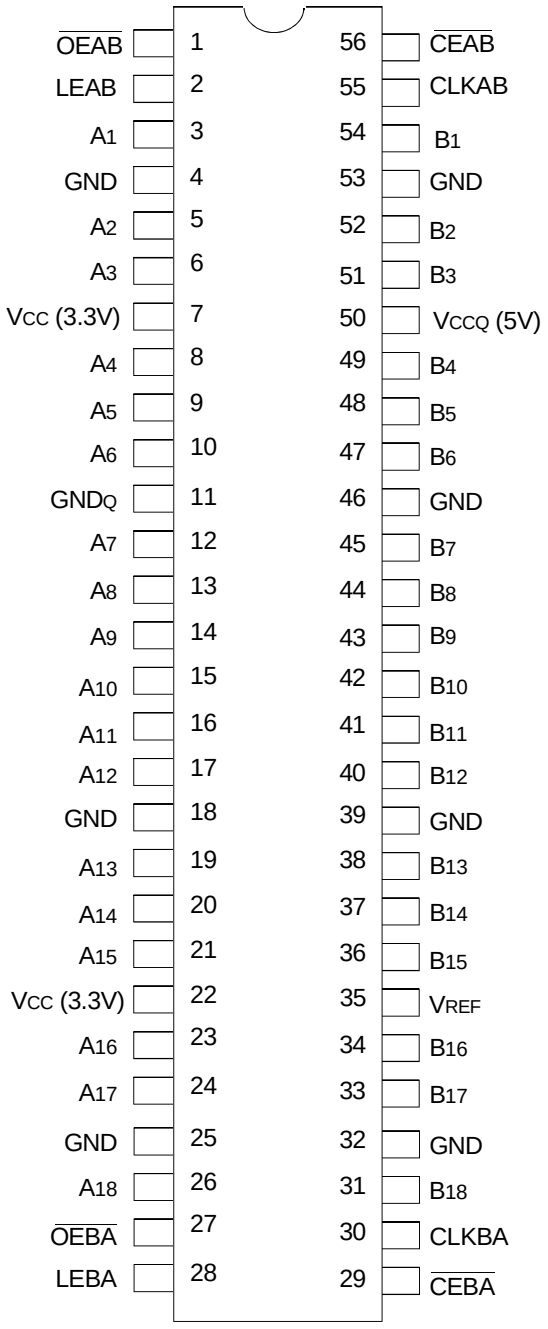
The GTLP16612 is an 18-bit universal bus transceiver. It provides signal level translation, from TTL to GTLP, for applications requiring a high-speed interface between cards operating at TTL logic levels and backplanes operating at GTLP logic levels. GTLP provides reduced output swing (<1V), reduced input threshold levels, and output edge-rate control to minimize signal setting times. The GTLP16612 is a derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD8-3 and incorporates internal edge-rate control, which is process, voltage, and temperature (PVT) compensated.

GTLP output low voltage is less than 0.5V. The output high is 1.5V, and the receiver threshold is 1V.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1,2)

Symbol	Rating	Max.	Unit
V_{CC}	Supply Voltage	–0.5 to +7	V
V_{CCQ}			
V_I	DC Input Voltage	–0.5 to +7	V
V_O	DC Output Voltage, 3-State	–0.5 to +7	V
V_O	DC Output Voltage, Active	–0.5 to V_{CC} + 0.5	V
I_{OL}	DC Output Sink Current into A-port	64	mA
I_{OH}	DC Output Source Current from A-port	–64	mA
I_{OL}	DC Output Sink Current into B-port (in the LOW state)	80	mA
I_{IK}	DC Input Diode Current V_I < 0V	–50	mA
I_{OK}	DC Output Diode Current V_O < 0V	–50	mA
I_{OK}	DC Output Diode Current V_O > V_{CC}	+50	mA
T_{STG}	Storage Temperature	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Unused inputs without Bus-Hold must be held HIGH or LOW.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.(2)	Max.	Unit
C_{IN}	Control Pins	V_I = V_{CCQ} or 0	8	—	pF
$C_{I/O}$	A-Port	V_I = V_{CCQ} or 0	9	—	pF
$C_{I/O}$	B-Port	V_I = V_{CCQ} or 0	6	—	pF

NOTES:
1. As applicable to the device type.
2. All typical values are at V_{CC} = 3.3V and V_{CCQ} = 5V.

PIN DESCRIPTION

Pin Names	Description(1)
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Transparent HIGH)
LEBA	B-to-A Latch Enable (Transparent HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{REF}	GTLP Input Reference Voltage
A_1 - A_{18}	A-to-B TTL Data Inputs or B-to-A 3-State Outputs
B_1 - B_{18}	B-to-A GTLP Data Inputs or A-to-B Open Drain Outputs

NOTE:
1. A-Port pins have Bus-Hold. All other pins are standard input, output, or I/O.

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Rating	Recommended	Unit
V_{CC}	Supply Voltage	3.15 to 3.45	V
V_{CCQ}		4.75 to 5.25	
V_{TT}	Bus Termination Voltage	1.35 to 1.65	V
V_I	Input Voltage on A-Port and Control Pins	0 to 5.5	V
I_{OH}	HIGH Level Output Current (A-Port)	-32	mA
I_{OL}	LOW Level Output Current (A-Port)	+32	mA
I_{OL}	LOW Level Output Current (B-Port)	+34	mA
T_A	Operating Temperature	–40 to +85	°C

NOTE:

1. Unused inputs without Bus-Hold must be held HIGH or LOW.

FUNCTIONAL DESCRIPTION:

The GTLP16612 combines a universal transceiver function with a TTL to GTLP translation. The A-Port and control pins operate at LVTTL or 5V TTL levels while the B-Port operates at GTLP levels. The transceiver logic includes D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clock mode.

FUNCTION TABLE(1,2)

Inputs					Outputs	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	Ax	Bx	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(3)	
L	L	L	L	X	B_0(4)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(4)	Clock Inhibit

NOTES:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{REF} = 1V, V_{CC} = 3.3V ± 5%, V_{CCQ} = 5V ± 5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	B-Port	—		V_{REF}+ 0.1	—	V_{TT}	V
	All Other ports	—		2	—	—	
V_{IL}	B-Port	—		0	—	V_{REF}– 0.1	V
	All Other ports	—		—	—	0.8	
V_{REF}	—	—		—	1	—	V
V_{IK}	—	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_I = –18mA	—	—	–1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max(2)	I_{OH} = –100µA	V_{CC}–0.2	—	—	V
		V_{CC} = 3.15V	I_{OH} = –8mA	2.4	—	—	
		V_{CCQ} = 4.75V	I_{OH} = –32mA	2	—	—	
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max(2)	I_{OL} = 100µA	—	—	0.2	V
		V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 32mA	—	—	0.5	
	B-Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 34mA	—	—	0.65	
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 5.5V or 0V	—	—	±10	µA
	A-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = 5.5V	—	—	20	
			V_I = V_{CC}	—	—	1	
			V_I = 0	—	—	–30	
	B-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = V_{CCQ}	—	—	5	
			V_I = 0	—	—	–5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V	—	—	100	µA
$I_{I(HOLD)}$	A-Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	V_I = 0.8V	75	—	—	µA
			V_I = 2V	–20	—	—	
I_{OZH}	A-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_O = 3.45 V	—	—	1	µA
	B-Port		V_O = 1.5V	—	—	5	
I_{OZL}	A-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_O = 0	—	—	–20	µA
	B-Port		V_O = 0.65V	—	—	–10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V V_{CCQ} = 5.25V I_O = 0 V_I = V_{CCQ} or GND	Outputs HIGH	—	30	40	mA
			Outputs LOW	—	30	40	
			Outputs Disabled	—	30	40	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V V_{CCQ} = 5.25V I_O = 0 V_I = V_{CCQ} or GND	Outputs HIGH	—	0	1	mA
			Outputs LOW	—	0	1	
			Outputs Disabled	—	0	1	
ΔI_{CC}(3)	A-Port and Control Pins	V_{CC} = 3.45V V_{CCQ} = 5.25V A or Control Inputs at V_{CC} or GND	One Input at 2.7V	—	0	1	mA

NOTES:

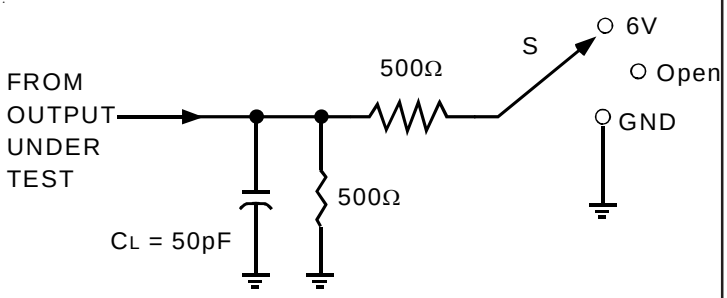
1. All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5V, and T_A = 25°C.
2. For conditions shown as Max. or Min., use appropriate value specified under Recommended Operating Conditions.
3. ΔI_{CC} is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (1,2)

		IDT74GTLP16612			
Symbol	**Parameter**	**Min.**	**Typ.(3)**	**Max.**	**Unit**
f_{CLOCK}	Max Clock Frequency	175	—	—	MHz
t_W	Pulse Duration, LEAB or LEBA HIGH	3	—	—	ns
t_W	Pulse Duration, CLKAB or CLKBA HIGH or LOW	3.2	—	—	
t_S	Setup Time, Ax before CLKAB ↑	0.5	—	—	ns
t_S	Setup Time, Bx before CLKBA ↑	3.1	—	—	
t_S	Setup Time, Ax before LEAB ↓	1.3	—	—	
t_S	Setup Time, Bx before LEBA ↓	3.7	—	—	
t_S	Setup Time, $\overline{CEAB}$ before CLKAB ↑	0.4	—	—	
t_S	Setup Time, $\overline{CEBA}$ beforeCLKBA ↑	1	—	—	
t_H	Hold Time, Ax after CLKAB ↑	1.5	—	—	ns
t_H	Hold Time, Bx after CLKBA ↑	0	—	—	
t_H	Hold Time, Ax after LEAB ↓	0.5	—	—	
t_H	Hold Time, Bx after LEBA ↓	0	—	—	
t_H	Hold Time, $\overline{CEAB}$ after CLKAB ↑	1.5	—	—	
t_H	Hold Time, $\overline{CEBA}$ afterCLKBA ↑	1.7	—	—	
t_{PLH}	Ax to Bx	1	4.3	6.5	ns
t_{PHL}		1	5	8.2	
t_{PLH}	LEAB to Bx	1.8	4.5	6.7	ns
t_{PHL}		1.5	5.3	8.6	
t_{PLH}	CLKAB to Bx	1.8	4.6	6.7	ns
t_{PHL}		1.5	5.4	8.7	
t_{PLH}	$\overline{OEAB}$ to Bx	1.6	4.4	6.2	ns
t_{PHL}		1.3	6.1	9.8	
t_{RISE} t_{FALL}	Transition Time, B outputs (20% to 80%)	—	2.6	—	ns
t_{PLH}	Bx to Ax	2	5.6	8.2	ns
t_{PHL}		1.4	5	7.2	
t_{PLH}	LEBA to Ax	2.1	4.2	6.3	ns
t_{PHL}		1.9	3.3	5	
t_{PLH}	CLKBA to Ax	2.3	4.4	6.8	ns
t_{PHL}		2.2	3.5	5.2	
t_{PZH} t_{PZL}	$\overline{OEBA}$ to Ax	1.5	5	6.2	
t_{PHZ} t_{PLZ}		1.9	3.9	7.9	ns

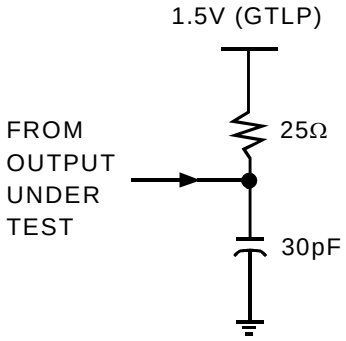
NOTES:
1. See Test Circuits and Waveforms. T_A = –40°C to +85°C.
2. Unless otherwise noted, V_{REF} = 1V, C_L = 30pF for B-Port, and C_L = 50pF for A-Port.
3. Typical values are at V_{CC} = 3.3V, V_{CCQ} = 5V, and T_A = 25°C.

TEST CIRCUITS AND WAVEFORMS



NOTE:
1. C_L includes probes and jig capacitance.

Test Circuit for A Outputs(1)

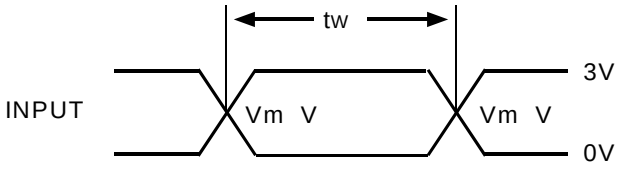


NOTE:
1. C_L includes probes and jig capacitance. For B-Port outputs, C_L = 30pF is used for worst case edge rate.

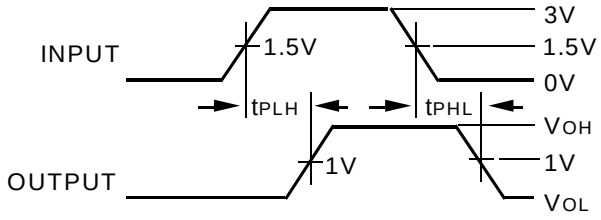
Test Circuit for B Outputs(1)

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open



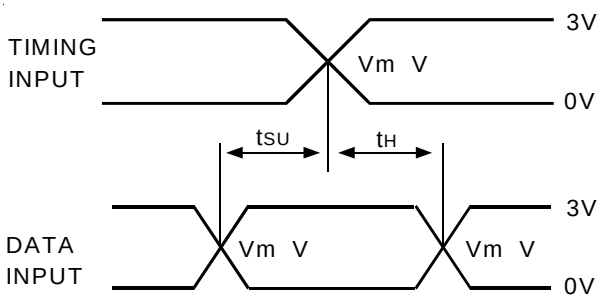
Voltage Waveforms Pulse Duration
(Vm = 1.5V for A-Port and 1V for B-Port)



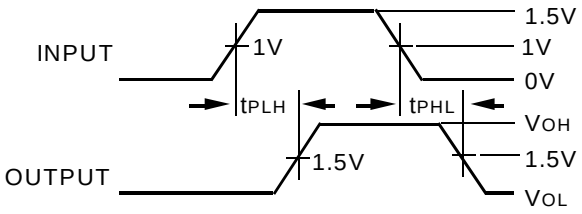
Voltage Waveforms Propagation Delay Times
(A-Port to B-Port)

NOTE:
All input pulses have the following characteristics: frequency = 10 MHz, $t_R = t_F$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

TEST CIRCUITS AND WAVEFORMS

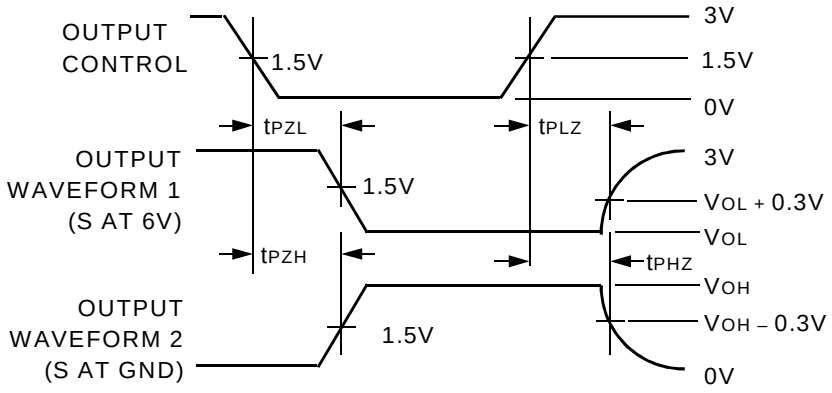


Voltage Waveforms Setup and Hold Times
(Vm = 1.5V for A-Port and 1V for B-Port)



Voltage Waveforms Propagation Delay Times
(B-Port to A-Port)

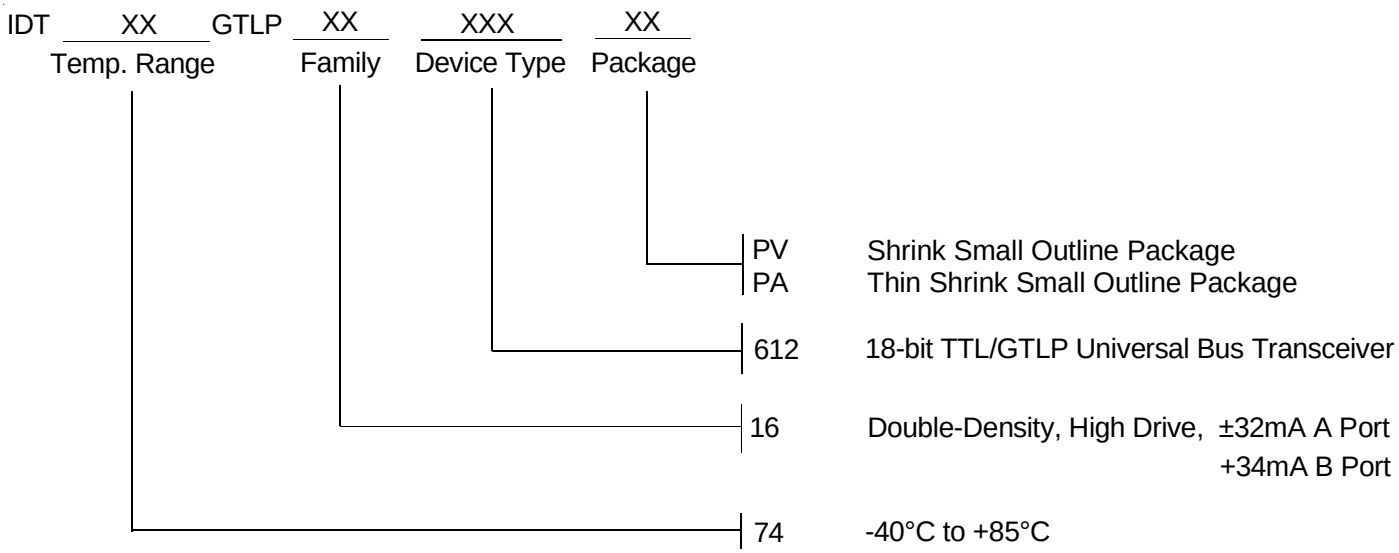
NOTE:
All input pulses have the following characteristics: frequency = 10 MHz, $t_R = t_F$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.



Voltage Waveforms Enable and Disable Times
(A-Port)

NOTE:
Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
All input pulses have the following characteristics: frequency = 10 MHz, $t_R = t_F$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

ORDERING INFORMATION



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