Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377T/AT/CT/DT

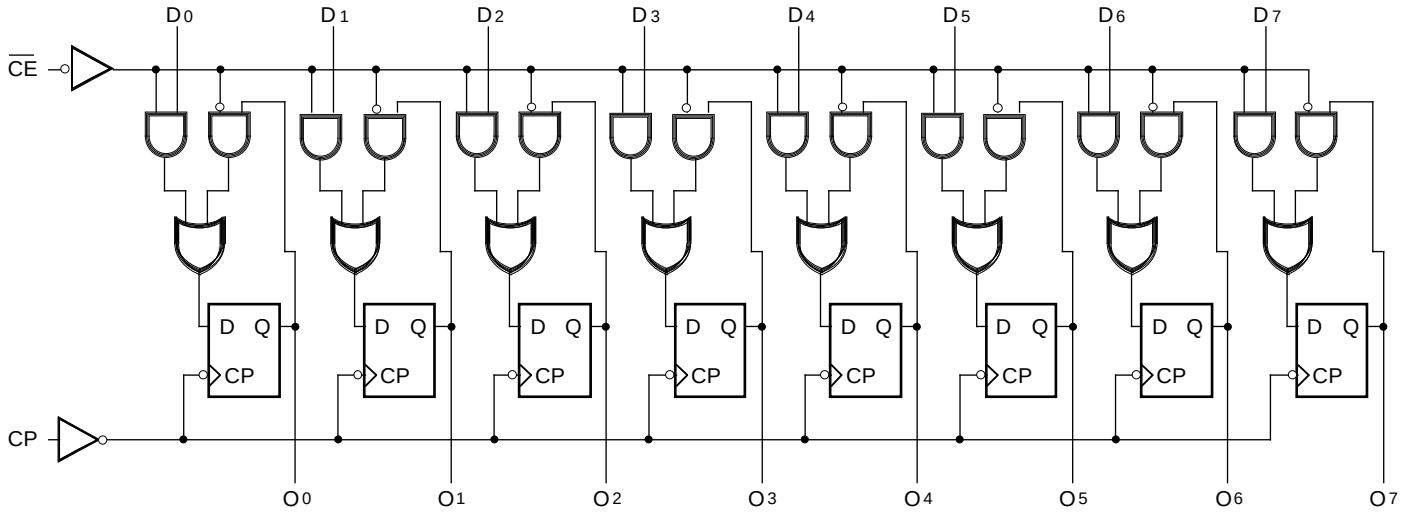
FEATURES:

- Std., A, C and D speed grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit “live insertion”
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

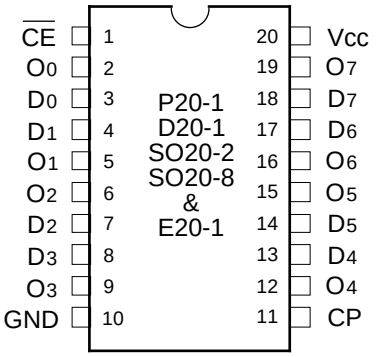
The IDT54/74FCT377T/AT/CT/DT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT377T/AT/CT/DT have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop’s O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

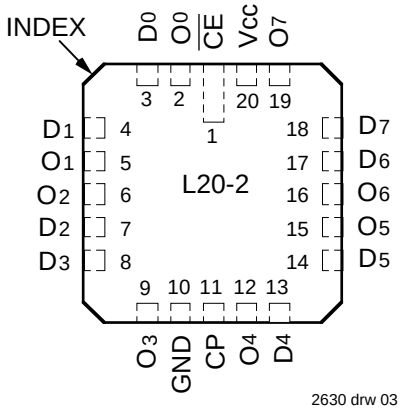


2630 drw 01

PIN CONFIGURATIONS



DIP/SOIC/QSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
$O_0 - O_7$	Data Outputs
CP	Clock Pulse Input

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1)

Operating Mode	Inputs CP	Inputs $\overline{CE}$	Inputs D	Outputs O
Load “1”	↑	l	h	H
Load “0”	↑	l	l	L
Hold	↑	h	X	No Change
	H	H	X	No Change

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NOTE:
1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranted but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{CE}$ = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{CE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT377T				FCT54/74FCT377AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	ns
t_{SU}	Set-Up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-Up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	ns

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			IDT54/74FCT377CT				FCT54/74FCT377DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	5.5	2.0	4.4	—	—	ns
t_{SU}	Set-Up Time HIGH or LOW Dn to CP		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Dn to CP		1.5	—	1.5	—	1.0	—	—	—	ns
t_{SU}	Set-Up Time HIGH or LOW $\overline{CE}$ to CP		3.5	—	3.5	—	3.0	—	—	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	0.0	—	—	—	ns
t_W	Clock Pulse Width, HIGH or LOW		6.0	—	7.0	—	3.0	—	—	—	ns

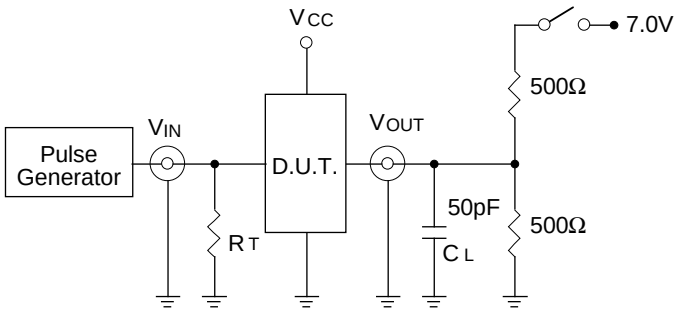
NOTES:

2630 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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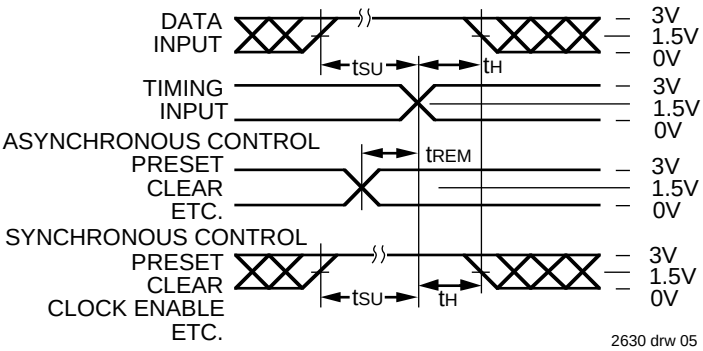
DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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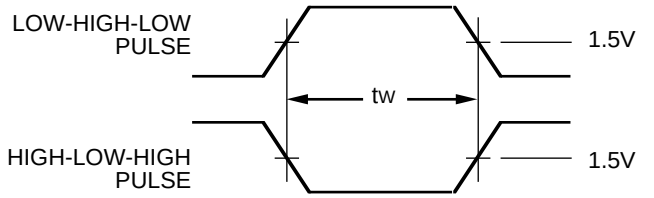
PULSE WIDTH



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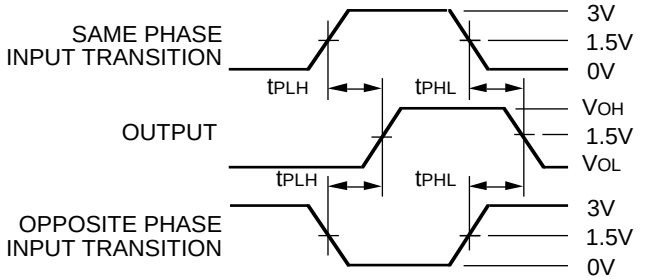
PROPAGATION DELAY



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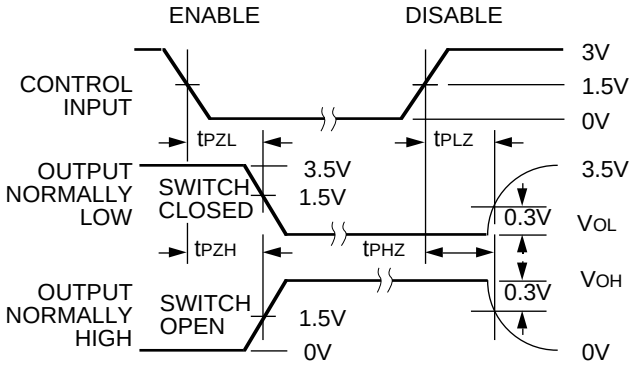
ENABLE AND DISABLE TIMES



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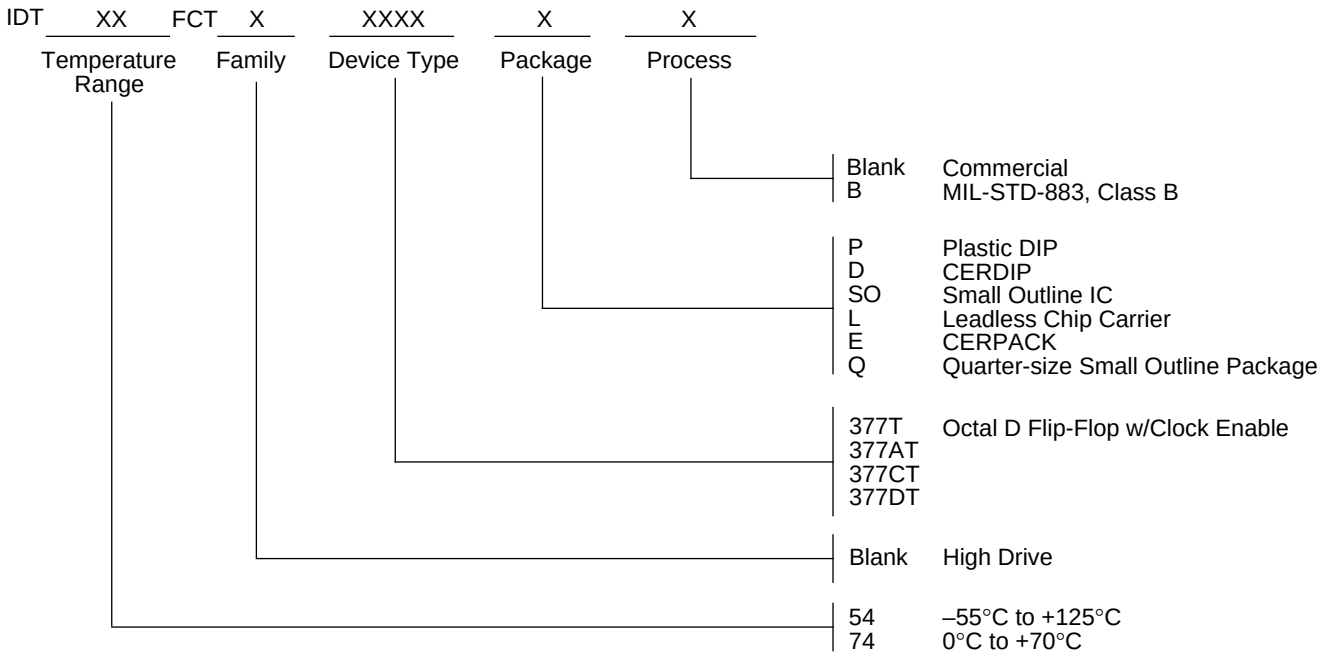
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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