



Description

The ICS650-27 is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 12.5 MHz or 25 MHz clock or fundamental mode crystal input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The ICS650-27 outputs all have zero ppm synthesis error.

The ICS650-27 is pin compatible and functionally equivalent to the ICS650-07. It is a performance upgrade and is recommended for all new 3.3V designs.

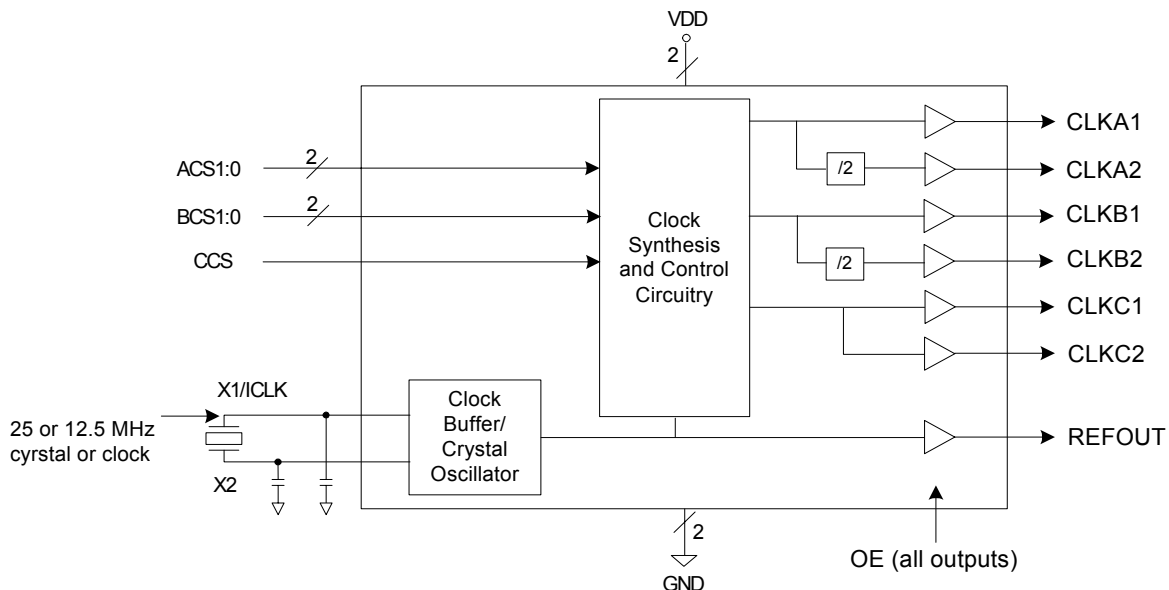
See the MK74CB214, ICS551, and ICS552-01 for non-PLL buffer devices which produce multiple low-skew copies of these output clocks.

See the ICS570, ICS9112-16/17/18 for zero delay buffers that can synchronize outputs and other needed clocks.

Features

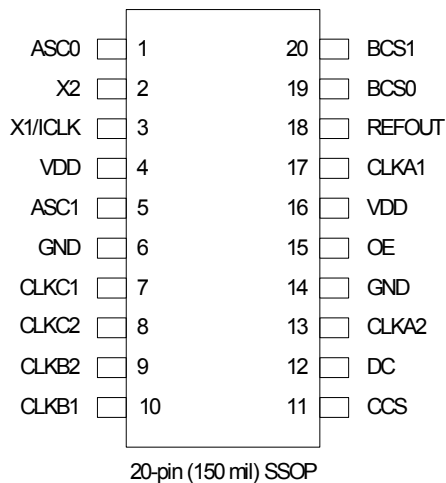
- Packaged in 20-pin (150 mil) SSOP (QSOP)
- Available in Pb (lead) free package
- 12.5 MHz or 25 MHz fundamental crystal or clock input
- Six output clocks with selectable frequencies
- SDRAM frequencies of 67, 83, 100, and 133 MHz
- Buffered crystal reference output
- Zero ppm synthesis error in all clocks
- Ideal for PMC-Sierra's ATM switch chips
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- Operating voltage of 3.3 V
- Industrial temperature only

Block Diagram





Pin Assignment



Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | ACS0 | Input | A clock select 0. Selects outputs on CLKA1 and CLKA2 per table on page 3. |
| 2 | X2 | Input | Crystal connection. Connect to a fundamental crystal or leave unconnected for a clock input. |
| 3 | X1/CLK | Input | Crystal connection. Connect to a fundamental crystal or clock input. |
| 4 | VDD | Power | Connect to +3.3 V or 5 V. Must be the same as pin 16. |
| 5 | ACS1 | Input | A clock select 1. Selects outputs on CLKA1 and CLKA2 per table on page 3. Internal pull-up. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLKC1 | Output | Output Clock C1. Depends on setting of CCS per table on page 3. |
| 8 | CLKC2 | Output | Output Clock C2. Depends on setting of CCS per table on page 3. Same as CLKC1. |
| 9 | CLKB2 | Output | Output Clock B2. Depends on setting of BCS1, 0 per table on page 3. |
| 10 | CLKB1 | Output | Output Clock B1. Depends on setting of BCS1, 0 per table on page 3. |
| 11 | CCS | Input | Clock C select pin. Selects outputs on CLKC1 and CLKC2 per table on page 3. |
| 12 | DC | - | Don't connect. Do not connect anything to this pin. |
| 13 | CLKA2 | Output | Output Clock A2. Depends on setting of ACS1, 0 per table on page 3. |
| 14 | GND | Power | Connect to ground. |
| 15 | OE | Input | Output enable. Tri-states all outputs when low. Internal pull-up. |
| 16 | VDD | Power | Connect to +3.3 V or 5 V. Must be the same as pin 4. |
| 17 | CLKA1 | Output | Output Clock A1. Depends on setting of ACS1, 0 per table on page 3. |
| 18 | REFOUT | Output | Buffered reference clock output. Same frequency as crystal or clock input. |
| 19 | BCS0 | Input | B clock select 0. Selects outputs on CLKB1 and CLKB2 per table on page 3. |
| 20 | BCS1 | Input | B clock select 1. Selects outputs on CLKB1 and CLKB2 per table on page 3. Internal pull-up. |



For a 25 MHz fundamental crystal or clock input, the following four tables apply:

A Clocks Select Table (outputs in MHz)

| ASC1 | ASC0 | CLKA1 | CLKA2 |
|------|------|---------|-----------|
| 0 | 0 | 100 | off (low) |
| 0 | M | Test | Test |
| 0 | 1 | 75 | off (low) |
| 1 | 0 | 33.3333 | 16.6667 |
| 1 | M | Test | Test |
| 1 | 1 | 66.6667 | 33.3333 |

B Clocks Select Table (outputs in MHz)

| BSC1 | BSC0 | CLKB1 | CLKB2 |
|------|------|----------|---------|
| 0 | 0 | Test | Test |
| 0 | M | 66.6667 | 33.3333 |
| 0 | 1 | 100 | 50 |
| 1 | 0 | 83.3333 | 41.6667 |
| 1 | M | Test | Test |
| 1 | 1 | 133.3333 | 66.6667 |

C Clocks Select Table (outputs in MHz)

| CCS | CLKC1 | CLKC2 |
|-----|-------|-------|
| 0 | 125 | 125 |
| M | Test | Test |
| 1 | 75 | 75 |

Reference Output Clock Frequency (in MHz)

| REFOUT |
|--------|
| 25 |

For a 12.5 MHz fundamental crystal or clock input, the following four tables apply:

A Clocks Select Table (outputs in MHz)

| ASC1 | ASC0 | CLKA1 | CLKA2 |
|------|------|---------|-----------|
| 0 | 0 | 50 | off (low) |
| 0 | M | Test | Test |
| 0 | 1 | 37.5 | off (low) |
| 1 | 0 | 16.6667 | 8.3333 |
| 1 | M | Test | Test |
| 1 | 1 | 33.3333 | 16.6667 |

B Clocks Select Table (outputs in MHz)

| BSC1 | BSC0 | CLKB1 | CLKB2 |
|------|------|---------|---------|
| 0 | 0 | Test | Test |
| 0 | M | 33.3333 | 16.6667 |
| 0 | 1 | 50 | 25 |
| 1 | 0 | 41.6667 | 20.8333 |
| 1 | M | Test | Test |
| 1 | 1 | 66.6667 | 33.3333 |

C Clocks Select Table (outputs in MHz)

| CCS | CLKC1 | CLKC2 |
|-----|-------|-------|
| 0 | 62.5 | 62.5 |
| M | Test | Test |
| 1 | 37.5 | 37.5 |

Reference Output Clock Frequency (in MHz)

| REFOUT |
|--------|
| 12.5 |

0 = connect directly to GND

M = leave unconnected (automatically self biases to VDD/2)

1 = connect directly to VDD



External Components

The ICS650-27 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01 μ F must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-27. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 175°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | +3.3 | +3.6 | V |



DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V \pm 10%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|------------------|---------------------------|---------|----------|---------|------------|
| Operating Voltage | VDD | | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | V _{IH} | X1 pin only, CLK input | VDD/2+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | X1 pin only, CLK input | | VDD/2 | VDD/2-1 | V |
| Input High Voltage | V _{IH} | all tri-level type inputs | VDD-0.5 | | | V |
| Input Low Voltage | V _{IL} | all tri-level type inputs | | | 0.5 | V |
| Input High Voltage | V _{IH} | all other inputs | 2 | | | V |
| Input Low Voltage | V _{IL} | all other inputs | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25mA | | | 0.8 | V |
| Output High Voltage, CMOS level | V _{OH} | I _{OH} = -8 mA | VDD-0.4 | | | V |
| Operating Supply Current | I _{DD} | No Load | | 50 | | mA |
| Short Circuit Current | I _{OS} | Each output | | \pm 50 | | mA |
| Internal pull-up resistor | R _{PU} | BCS1, OE pins | | 510 | | k Ω |
| | | ACSI pin | | 120 | | k Ω |
| Nominal output impedance | Z _{OUT} | | | 20 | | Ω |

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V \pm 10%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------|-----------------------------|------|------------|------|-------|
| Input Frequency | | | 10 | 12.5 or 25 | 27 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, Note 1 | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.8 V, Note 1 | | | 1.5 | ns |
| Output Clock Duty Cycle | | At VDD/2, Note 1 | 40 | 50 | 60 | % |
| Frequency Error | | All clocks | | | 0 | ppm |
| Absolute Jitter, short term | | Variation from mean, Note 1 | | \pm 150 | | ps |

Note 1: Measured with 15 pF load

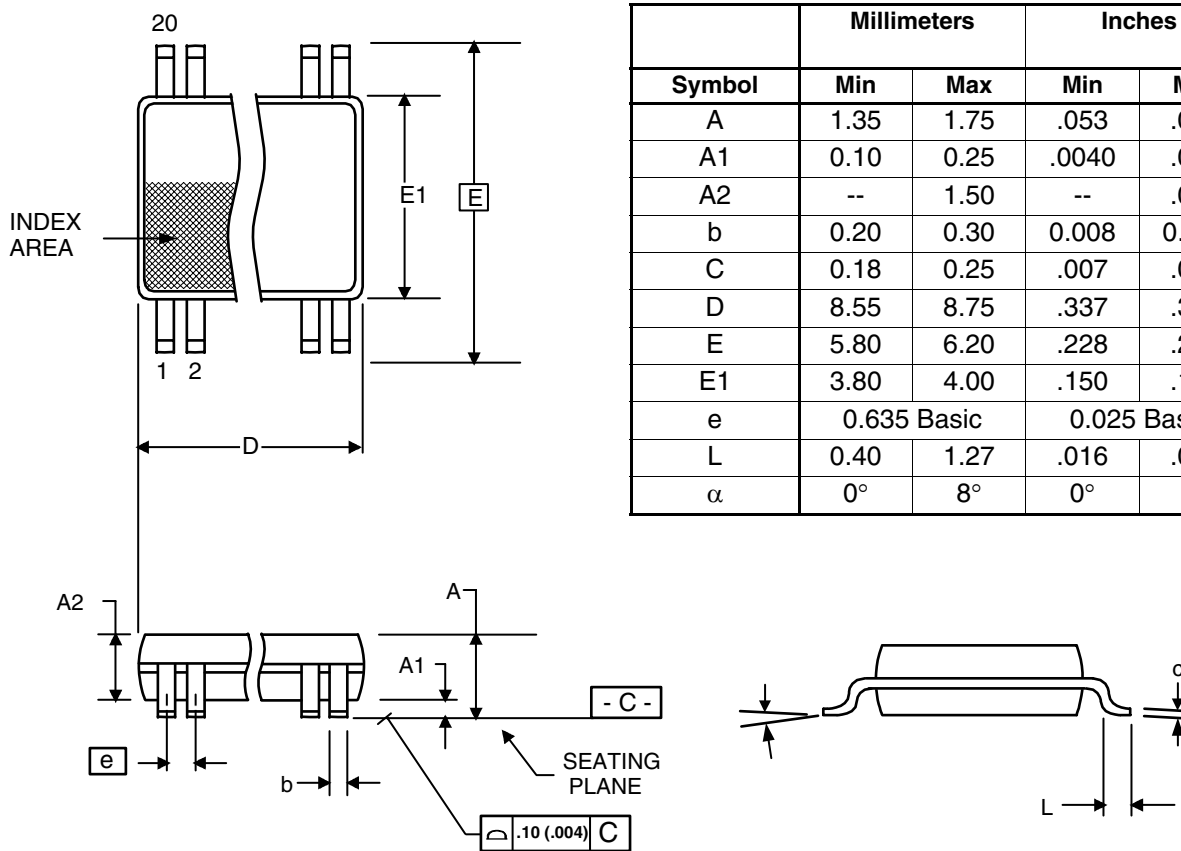
Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 135 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 93 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 60 | | °C/W |



Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|-------------|---------------|
| ICS650R-27I | ICS650R-27I | Tubes | 20-pin SSOP | -40 to +85° C |
| ICS650R-27IT | ICS650R-27I | Tape and Reel | 20-pin SSOP | -40 to +85° C |
| ICS650R-27ILF | 650R-27ILF | Tubes | 20-pin SSOP | -40 to +85° C |
| ICS650R-27ILFT | 650R-27ILF | Tape and Reel | 20-pin SSOP | -40 to +85° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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