8-BIT SINGLE-CHIP MICROCONTROLLERS

HMS77C1000A
HMS77C1001A

User's Manual (Ver. 2.0)

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hynix
Semiconductor

Version 1.1

Published by
MCU Application Team

Contents of Table

HMS77C1000A / HMS77C1001A

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

1. OVERVIEW

1.1 Description

The HMS77C1000A and HMS77C1001A are an advanced CMOS 8-bit microcontroller with 0.5K/1K words(12-bit) of EPROM. The Hynix Semiconductor HMS77C1000A and HMS77C1001A are a powerful microcontroller which provides a high flexibility and cost effective solution to many small applications. The HMS77C1000A and HMS77C1001A provide the following standard features: 0.5K/1K words of EPROM, 25 bytes of RAM, 8-bit timer/counter, power-on reset, on-chip oscillator and clock circuitry. In addition, the HMS77C1000A and HMS77C1001A supports power saving modes to reduce power consumption.

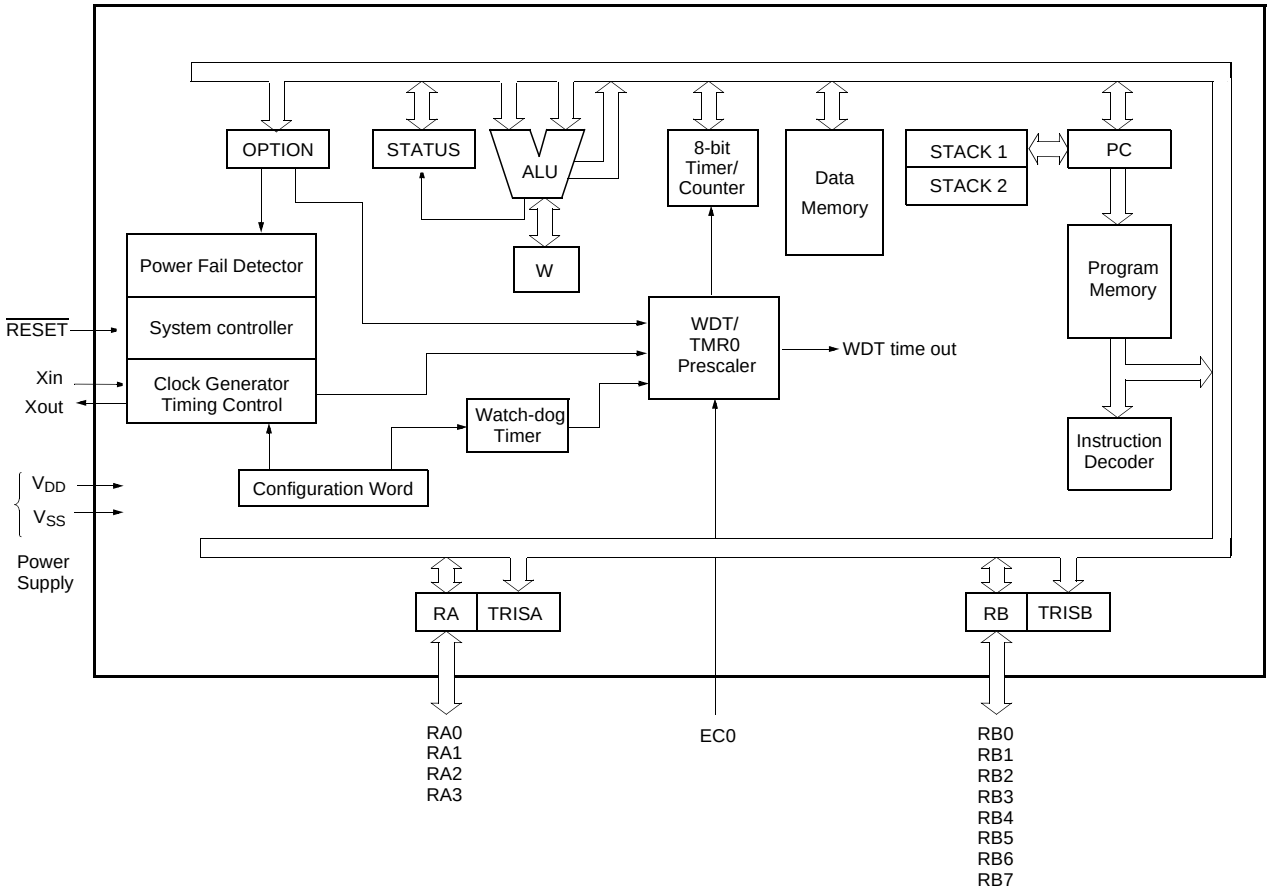
Device name	ROM Size	RAM Size	Package
HMS77C1000A	0.5K words(12-bit)	25 bytes	18 PDIP, SOP or 20 SSOP
HMS77C1001A	1K words(12-bit)	25 bytes	18 PDIP, SOP or 20 SSOP

1.2 Features

- **High-Performance RISC CPU:**
  - 12-bit wide instructions and 8-bit wide data path
  - 33 single word instructions
  - 0.5K/1K words on-chip program memory
  - 25 bytes on-chip data memory
  - Minimum instruction execution time 200ns @20MHz
  - Operating speed: DC - 20 MHz clock input
  - Seven special function hardware registers
  - Two-level hardware stack
- **Peripheral Features:**
  - Twelve programmable I/O lines
  - One 8-bit timer/counter with 8-bit programmable prescaler
  - Power-On Reset (POR)
  - Power Fail Detector : noise immunity circuit 2 level detect (2.7V, 1.8V)
  - Internal Reset Timer (IRT)
  - Watchdog Timer (WDT) with on-chip RC oscillator
  - Programmable code-protection
  - Power saving SLEEP mode
  - Selectable oscillator options: Configuration word

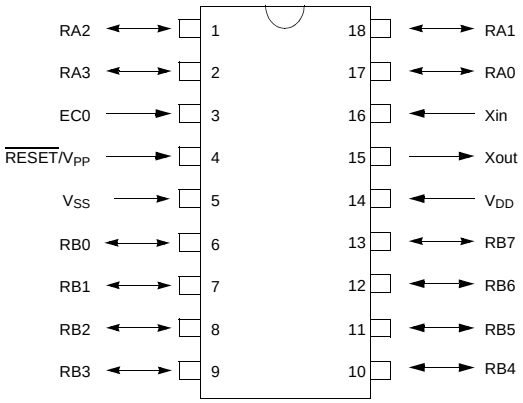
    RC: Low-cost RC oscillator (200KHz~4MHz)
    XT: Standard crystal/resonator (455KHz~4MHz)
    HF: High-speed crystal/resonator (4~20MHz)
    LF: Power saving, low-frequency crystal/resonator (32~200KHz)
- **CMOS Technology:**
  - Low-power, high-speed CMOS EPROM technology
  - Fully static design
  - Wide-operating range: 2.5V to 5.5V @ RC, XT, LF 4.5V to 5.5V @ HF

2. BLOCK DIAGRAM

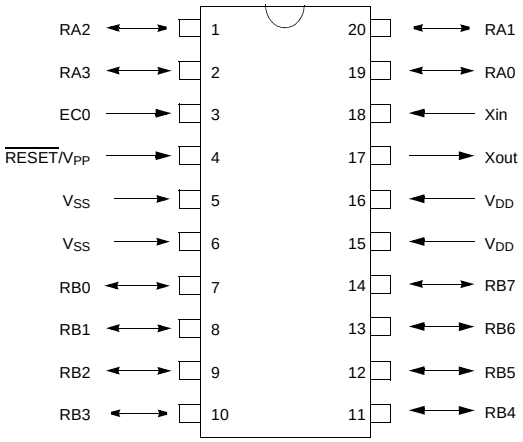


3. PIN ASSIGNMENT

18 PDIP or SOP



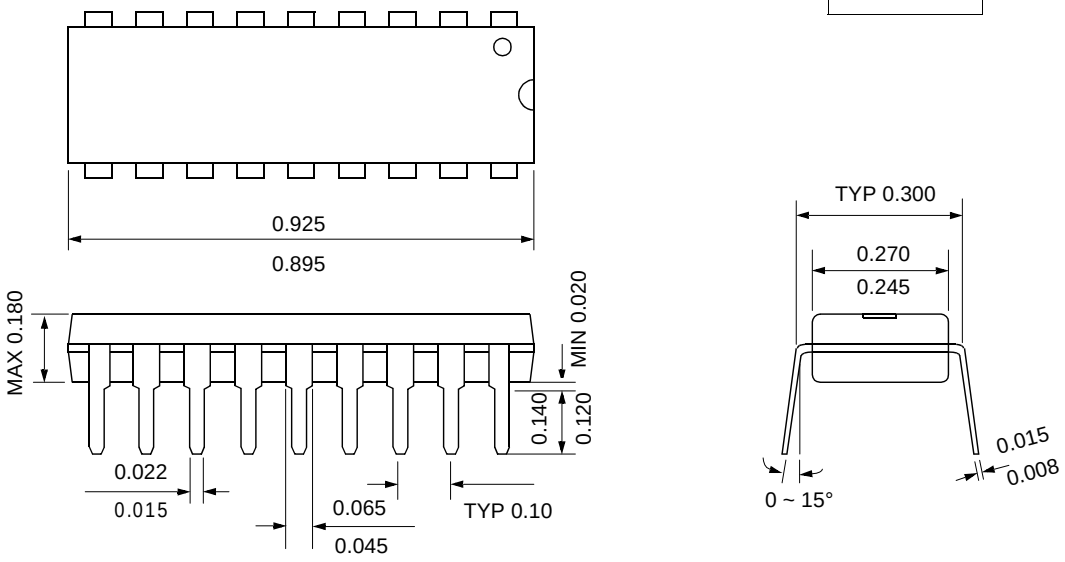
20 SSOP



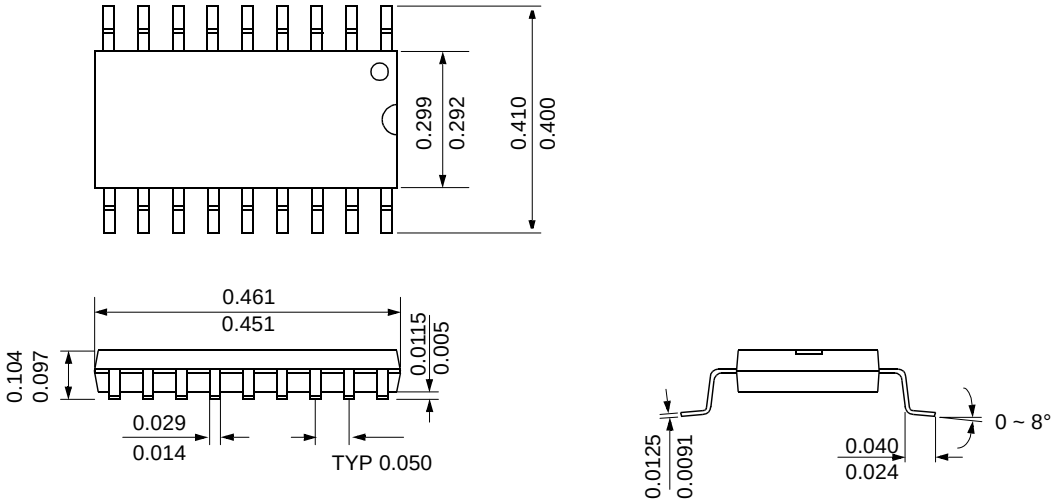
4. PACKAGE DIAGRAM

18 PDIP

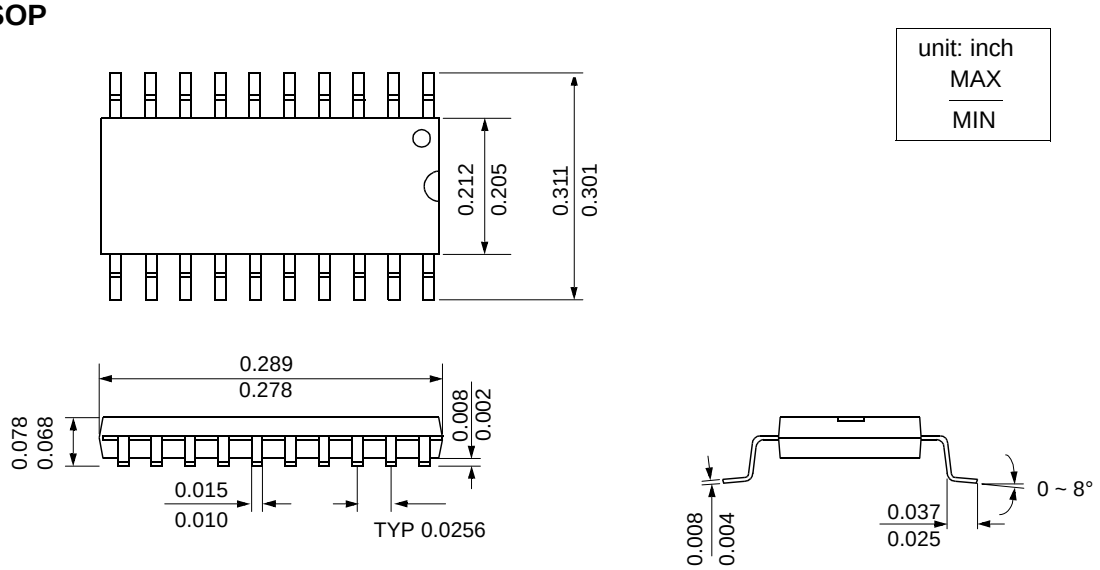
unit: inch
MAX
MIN



18 SOP



20 SSOP


unit: inch
MAX
MIN
0.212
0.205
0.311
0.301
0.289
0.278
0.078
0.068
0.008
0.002
0.015
0.010
TYP 0.0256
0.008
0.004
0.037
0.025
0 ~ 8°

5. PIN FUNCTION

V_{DD}: Supply voltage.

V_{SS}: Circuit ground.

$\overline{\text{RESET}}$: Reset the MCU.

X_{IN}: Input to the inverting oscillator amplifier and input to the internal main clock operating circuit.

X_{OUT}: Output from the inverting oscillator amplifier.

RA0~RA3: RA is an 4-bit, CMOS, bidirectional I/O port. RA pins can be used as outputs or inputs according to "0" or "1" written the their Port Direction Register(TRISA).

RB0~RB7: RB is a 8-bit, CMOS, bidirectional I/O port. RB pins can be used as outputs or inputs according to "0" or "1" written the their Port Direction Register(TRISB).

EC0: EC0 is an external clock input to Timer0. It should be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.

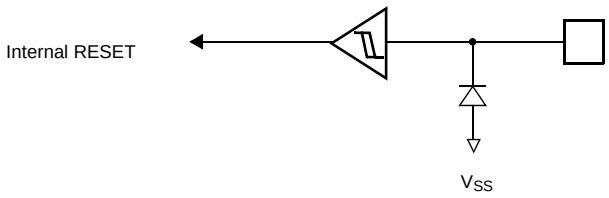
PIN NAME	DIP, SOP Pin No.	SSOP Pin No.	In/Out	Input Levels	Function
V_{DD}	14	15,16	P	-	Supply voltage
V_{SS}	5	5,6	P	-	Circuit ground
$\overline{\text{RESET}}$	4	4	I	ST	Reset signal input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{\text{RESET}}$ pin must not exceed V_{DD} to avoid unintended entering of programming mode.
X_{IN}	16	18	I	ST	Oscillator crystal input/external clock source input
X_{OUT}	15	17	O	-	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, X_{OUT} pin outputs CLKOUT which has 1/4 the frequency of X_{IN}, and denotes the instruction cycle rate.
RA0	17	19	I/O	TTL	4-bit bi-directional I/O ports
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	8-bit bi-directional I/O ports
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
EC0	3	3	I	ST	Clock input to Timer0. Must be tied to V_{DD} or V_{SS}, if not in use, to reduce current consumption.

TABLE 5-1 PINOUT DESCRIPTION

Legend : I =input, O = output, I/O = input/output, P = power, - = Not used, TTL = TTL input, ST = Schmitt Trigger input

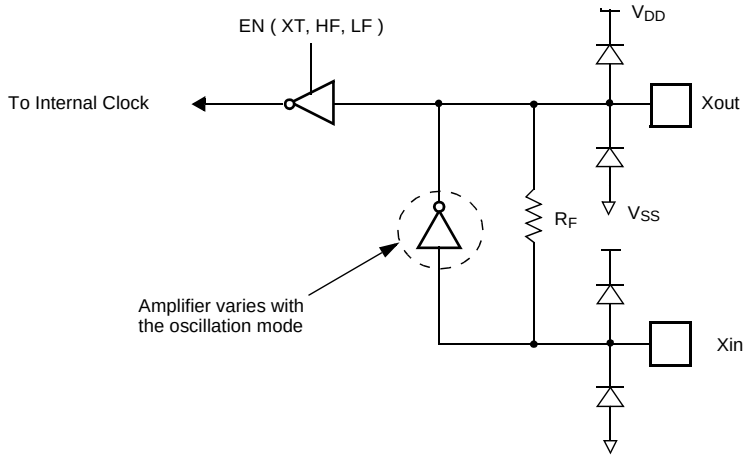
6. PORT STRUCTURES

• **$\overline{\text{RESET}}$**

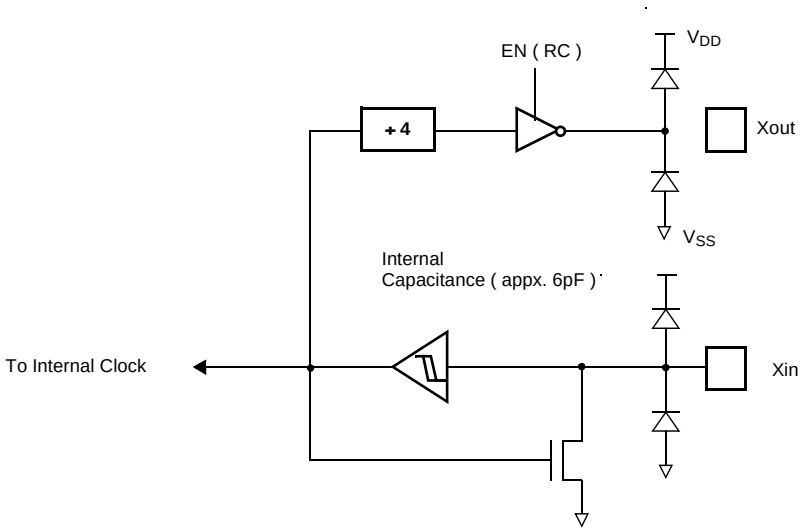


• **Xin, Xout**

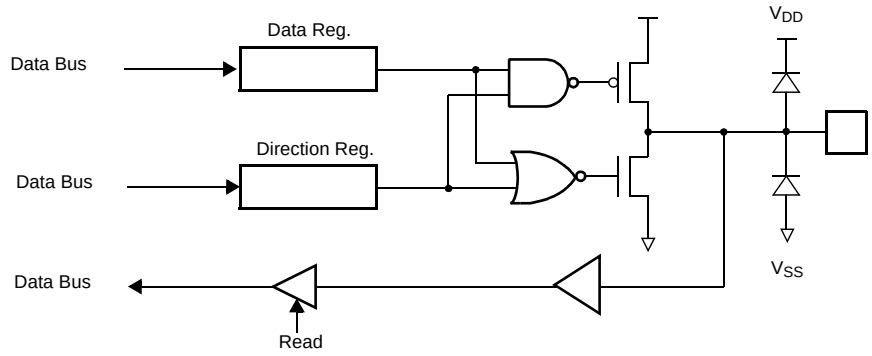
(XT, HF, LF Mode)



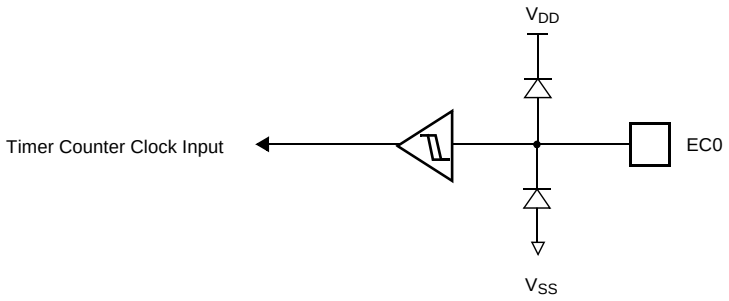
(RC Mode)



• **RA0~3/RB0~7**



• **EC0**



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Supply voltage ..... -0 to +7.5 V

Storage Temperature ..... -65 to +125 °C

Voltage on $\overline{\text{RESET}}$ with respect to V_{SS} ..... 0.3 to 13.5V

Voltage on any pin with respect to V_{SS}. -0.3 to V_{DD}+0.3

Maximum current out of V_{SS} pin ..... 150 mA

Maximum current into V_{DD} pin ..... 100 mA

Maximum output current sunk by (I_{OL} per I/O Pin) 25 mA

Maximum output current sourced by (I_{OH} per I/O Pin) ..... 20 mA

Maximum current (ΣI_{OL}) ..... 120 mA

Maximum current (ΣI_{OH}) ..... 80 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

7.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Specifications		Unit
			Min.	Max.	
Supply Voltage	V_{DD}	f_{XIN}=20MHz	4.5	5.5	V
		f_{XIN}=4MHz	2.5	5.5	
Operating Frequency	f_{XIN}	RC Mode	0.2	4	MHz
		XT Mode	0.455	4	
		HF Mode	4	20	
		LF Mode	32	200	KHz
Operating Temperature	T_{OPR}		-40	85	°C

7.3 DC Characteristics (1)

- **(T_A=-40°C~+85°C)**

Parameter	Symbol	Test Condition	Specification			Unit
			Min	Typ[1]	Max	
Supply Voltage						
XT, RC, LF	V_{DD}		2.5		5.5	V
HF			4.5		5.5	
V_{DD} start voltage to ensure Power-On Reset	V_{POR}		-	V_{SS}	-	V
VDD rise rate	S_{VDD}[2]		0.05	-	-	V/mS
RAM Data Retention Voltage	V_{DR}		-	1.5	-	V
Power Fail Detection						
Normal Level	V_{PFD}		-	2.7	-	V
Low Level			-	1.8	-	
Supply Current						
XT, RC[4]	I_{DD}[3]	X_{IN} = 4MHz, V_{DD} = 5V	-	1.8	3.3	mA
HF		X_{IN} = 20MHz, V_{DD} = 5V	-	9.0	20	mA
LF		X_{IN} = 32KHz, V_{DD} = 3V, WDT Disabled	-	17	40	uA
Power Down Current	I_{PD}[5]	V_{DD} = 3V, WDT Enabled	-	4	14	uA
		V_{DD} = 3V, WDT Disabled	-	0.4	5	

1. *Data in "Typ" column is at 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.*
2. *This parameter is characterized but not tested.*
3. *The test conditions for all I_{DD} measurements in NOP execution are:*
   X_{IN} = external square wave; all I/O pins tristated, pulled to V_{SS}, EC0 = V_{DD}, RESET = V_{DD}; WDT disabled/enabled as specified.
4. *Does not include current through $R_{ext.}$ The current through the resistor can be estimated by the formula; $I_R = V_{DD}/2R_{ext}$ (mA)*
5. *Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS} as like measurement conditions of supply current.*

7.4 DC Electrical Characteristics (2)

- **(T_A=-40°C~+85°C)**

Parameter	Symbol	Test Condition	Specification			Unit
			Min	Typ[1]	Max	
Input High Voltage						
I/O Ports (TTL)			$0.25V_{DD}$ +0.8			
$\overline{\text{RESET}}$, EC0, (ST)	V_{IH}		$0.85V_{DD}$		V_{DD}	V
X_{IN} (ST)		RC only	$0.85V_{DD}$			
X_{IN} (ST)		XT, HF, LF	$0.7V_{DD}$			
Input Low Voltage						
I/O Ports (TTL)					$0.15V_{DD}$	
$\overline{\text{RESET}}$, EC0, (ST)	V_{IL}		V_{SS}		$0.15V_{DD}$	V
X_{IN} (ST)		RC only			$0.15V_{DD}$	
X_{IN} (ST)		XT, HF, LF			$0.3V_{DD}$	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		$0.15V_{DD}$[2]			V
Input Leakage Current		$V_{IN} = V_{DD}$ or V_{SS}				
X_{IN} (ST)	I_L	XT, HF, LF	-3.0	0.5	3.0	uA
Other Pins			-1.0	0.2	1.0	
Output High Voltage						
I/O Ports	V_{OH}	I_{OH} = -5.0mA, V_{DD} = 4.5V	V_{DD} - 0.9		V_{DD}	V
X_{OUT}		I_{OH} = -0.5mA, V_{DD} = 4.5V, RC osc.				
Output Low Voltage						
I/O Ports	V_{OL}	I_{OL} = 8.0mA, V_{DD} = 4.5V	V_{SS}		0.8	V
X_{OUT}		I_{OL} = 0.6mA, V_{DD} = 4.5V, RC osc.				

1. *Data in "Typ" column is at 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.*
2. *This parameter are characterized but not tested.*

7.5 AC Electrical Characteristics (1)

- **(T_A=-40°C~+85°C)**

Parameter	Symbol	Test Condition	Specification			Unit
			Min	Typ	Max	
External Clock Input Frequency	F_{XIN}	XT osc mode	DC	-	4.0	MHz
		HF osc mode	DC	-	20	MHz
		LF osc mode	DC	-	200	KHz
Oscillator Frequency [1]	F_{XIN}	RC osc mode	DC	-	4.0	MHz
		XT osc mode	0.1	-	4.0	MHz
		HF osc mode	4.0	-	20	MHz
		LF osc mode	5.0	-	200	KHz
External Clock Input Period	T_{XIN}	XT osc mode	250	-	-	nS
		HF osc mode	50	-	-	nS
		LF osc mode	5	-	-	uS
Oscillator Period [1]	T_{XIN}	RC osc mode	250	-	-	nS
		XT osc mode	250	-	10,000	nS
		HF osc mode	50	-	250	nS
		LF osc mode	5	-	200	uS
Clock in X_{IN} Pin [1] **Low to High Time**	$T_{XIN}L$ $T_{XIN}H$	XT osc mode	85	-	-	nS
		HF osc mode	20	-	-	nS
		LF osc mode	2	-	-	uS
Clock in X_{IN} Pin [1] **Rise or Fall Time**	$T_{XIN}R$ $T_{XIN}F$	XT osc mode	-	-	25	nS
		HF osc mode	-	-	25	nS
		LF osc mode	-	-	50	nS

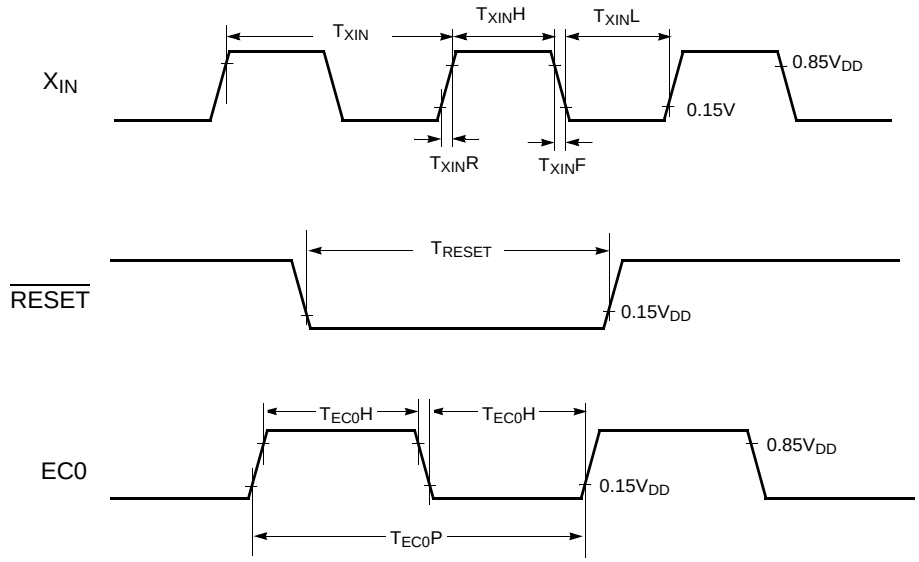
1. This parameter is characterized but not tested.

7.6 AC Electrical Characteristics (2)

- **(T_A=-40°C~+85°C)**

Parameter [1]	Symbol	Test Condition	Specification			Unit
			Min	Typ[2]	Max	
$\overline{\text{RESET}}$ Pulse Width (Low)	T_{RESET}	V_{DD} = 5V	100	-	-	nS
Watchdog Timer Time-Out Period (No-prescaler)	T_{WDT}	V_{DD} = 5V	9	18	30	mS
Internal Reset Timer Period	T_{IRT}	V_{DD} = 5V	9	18	30	mS
EC0 High or Low Pulse Width						
No Prescaler	$T_{EC0}H$ $T_{EC0}L$	T_{CY} = 4 X T_{XIN}	10	-	-	nS
With Prescaler			$0.5T_{CY}$ + 20	-	-	
EC0 Period						
No Prescaler	$T_{EC0}P$	N = Prescaler Value (1,2,4,.....256)	20	-	-	nS
With Prescaler			$(T_{CY}+40)$ / N	-	-	

1. These parameters are characterized but not tested.
2. Data in "Typ" column is at 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



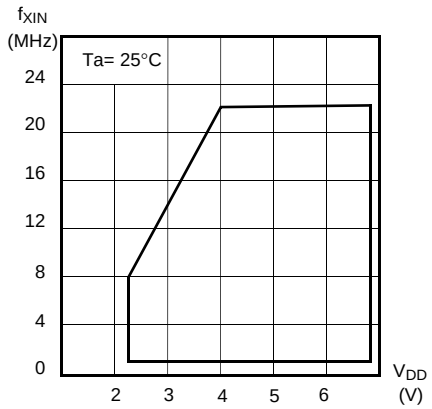
7.7 Typical Characteristics

These graphs and tables are for design guidance only and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (e.g. outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

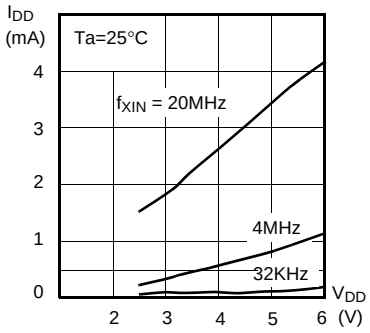
The data is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation

Operating Area

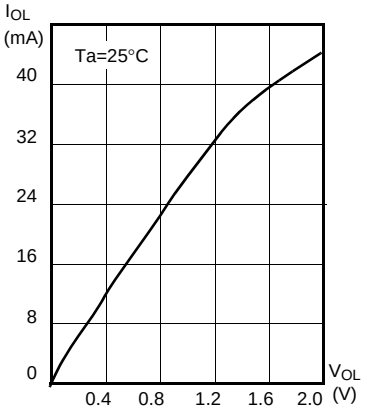


Normal Operation

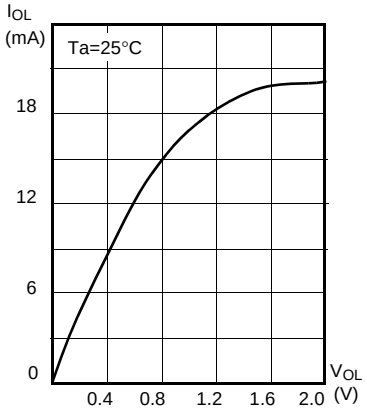
IDD–VDD



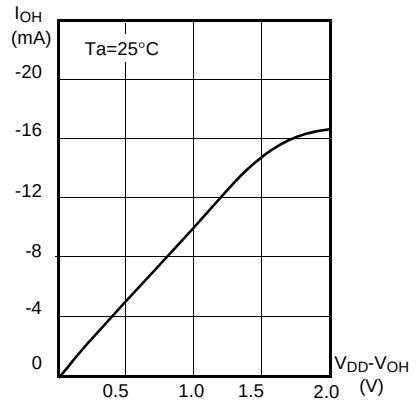
IOL–VOL, VDD=5V



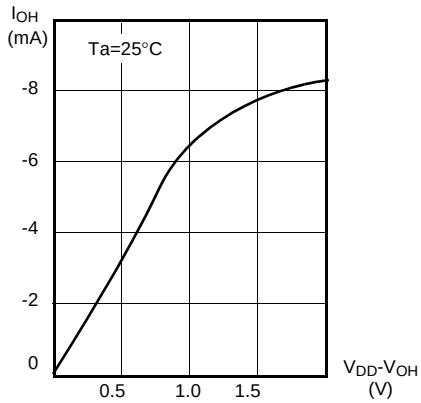
IOL–VOL, VDD=3V



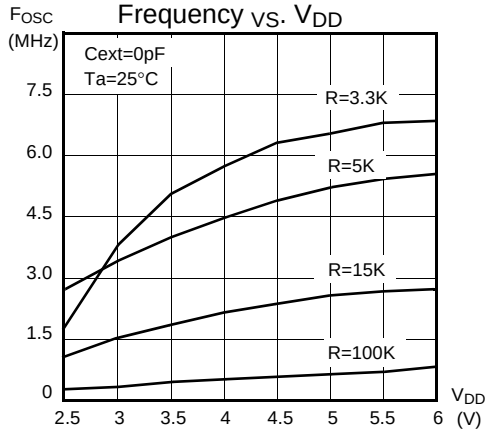
I_{OH}–V_{OH}, V_{DD}=5V



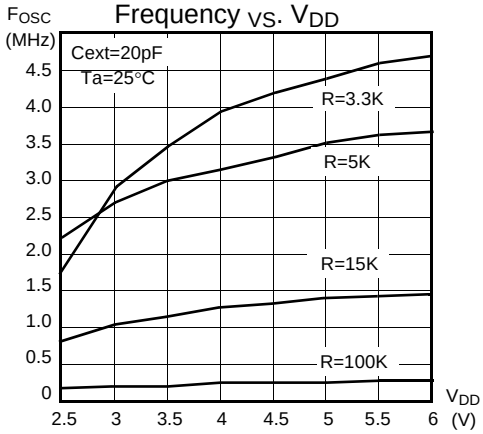
I_{OH}–V_{OH}, V_{DD}=3V



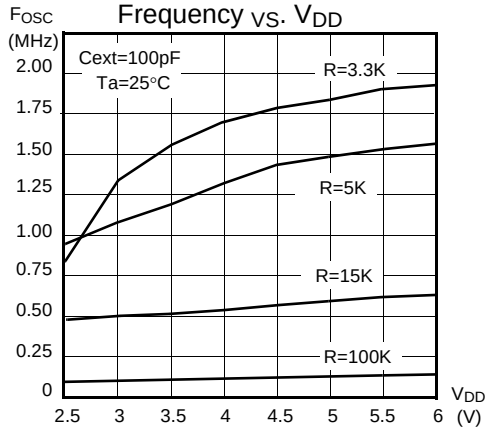
Typical RC Oscillator Frequency $_{VS.}$ V_{DD}



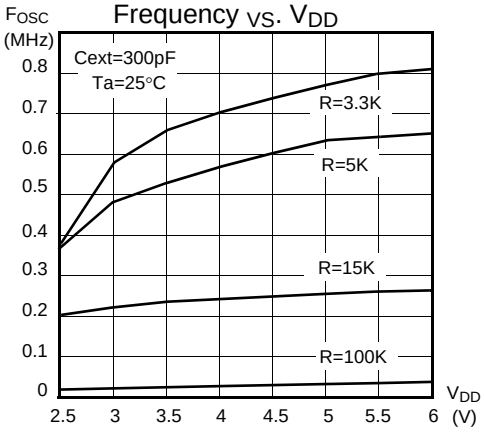
Typical RC Oscillator Frequency $_{VS.}$ V_{DD}



Typical RC Oscillator Frequency $_{VS.}$ V_{DD}



Typical RC Oscillator Frequency $_{VS.}$ V_{DD}



Cext	Rext	Average
		Fosc @ 5V,25°C
0pF	3.3K	6.5MHz
	5K	5.4MHz
	15K	2.3MHz
	100K	400KHz
20pF	3.3K	4.3MHz
	5K	3.5MHz
	15K	1.4MHz
	100K	240KHz
100pF	3.3K	1.8MHz
	5K	1.5MHz
	15K	610KHz
	100K	100KHz
300pF	3.3K	780KHz
	5K	630KHz
	15K	260KHz
	100K	42.5KHz

Table 7-1 RC Oscillator Frequencies

8. ARCHITECTURE

8.1 CPU Architecture

The HMS700 core is a RISC-based CPU and uses a modified Harvard architecture. This architecture uses two separate memories with separate address buses, one for the program memory and the other for the data memory. This architecture adapts 33 single word instructions that are 12-bit wide instruction and has an internal 2-stage pipeline (fetch and execute), which results in execution of one instruction per single cycle(200ns @ 20MHz) except for program branches.

The HMS77C100XA can address 1K x 12 Bits program memory and 25 Bytes data memory. And it can directly or indirectly address data memory.

The HMS700 core has three special function registers - PC, STATUS and FSR - in data memory map and has ATU (Address Translation Unit) to provide address for data memory and has an 8-bit general purpose ALU and working register(W) as an accumulator. The W register consists of 8-bit register and it can not be an addressed register.

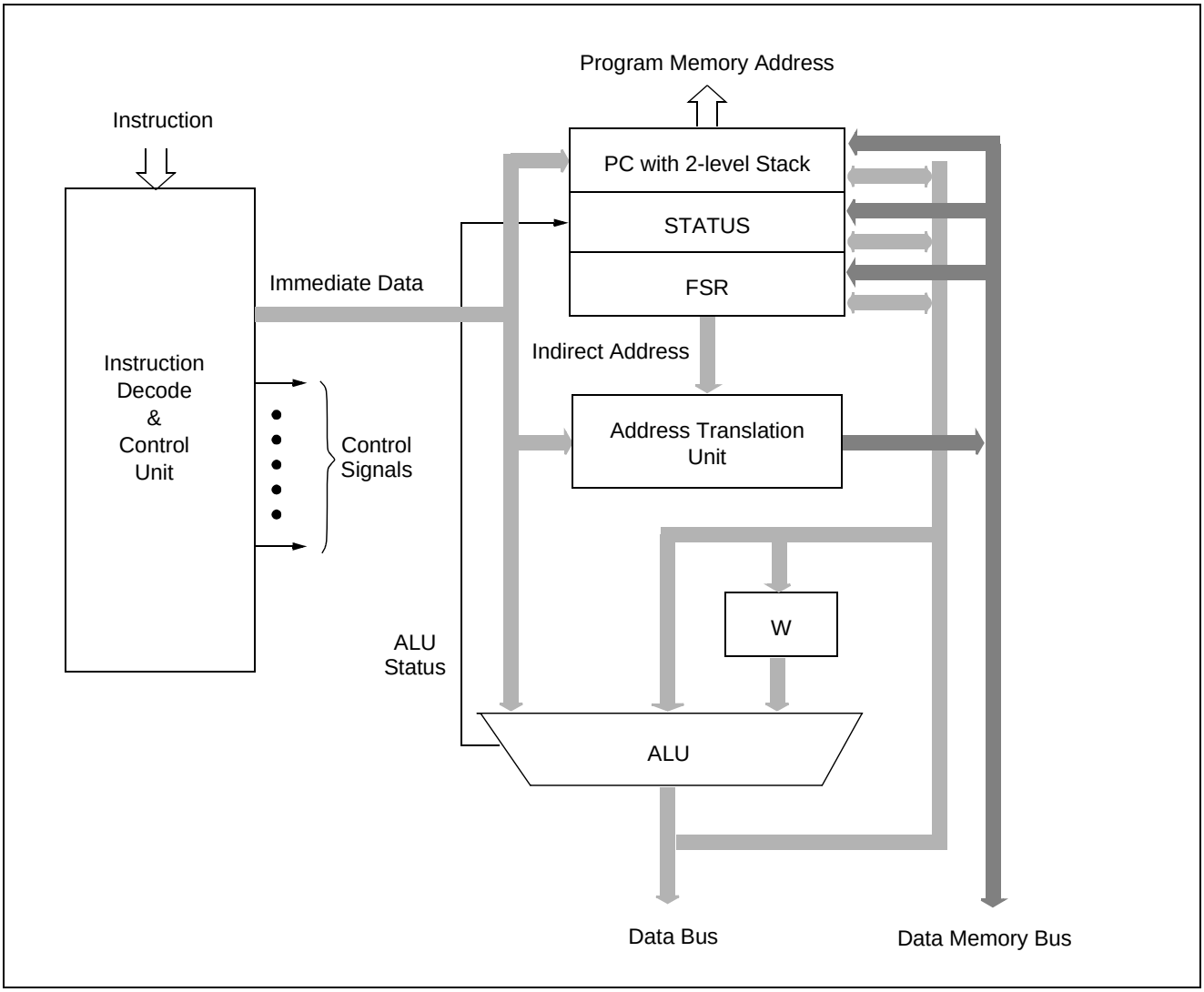


FIGURE 8-1 HMS700 CPU BLOCK DIAGRAM

9. MEMORY

The HMS77C100XA has separate memory maps for program memory and data memory. Program memory can only be read, not written to. It can be up to 1K words of program memory. Data memory can be read and written to 32 bytes including special function registers.

9.1 Program Memory

The program memory is organized as 0.5K, 12-bit wide words(HMS77C1000A) and 1K, 12-bit wide words(HMS77C1001A). The program memory words are addressed sequentially by a program counter. Incrementing at location $1FF_H$(HMS77C1000A) or $3FF_H$ (HMS77C1001A) will cause a wrap around to 000_H.

Figure 9-1 and Figure 9-2 show a map of program memory. After reset, CPU begins execution from reset vector which is stored in address($1FF_H$: HMS77C1000A, $3FF_H$: HMS77C1001A).

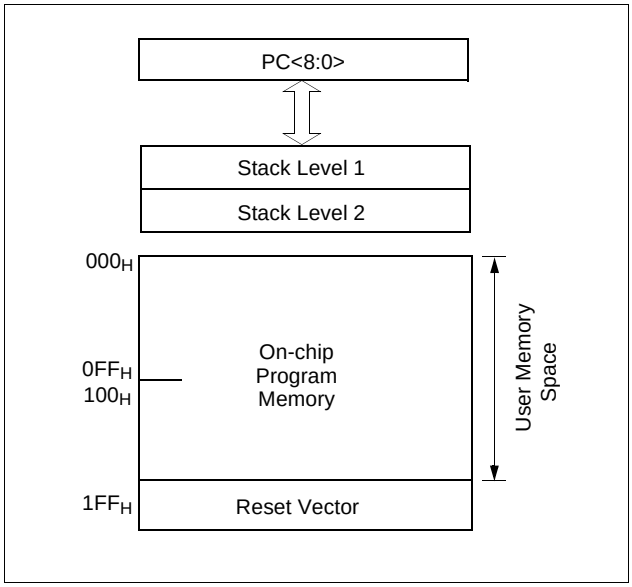


FIGURE 9-1 HMS77C1000A PROGRAM MEMORY MAP AND STACK

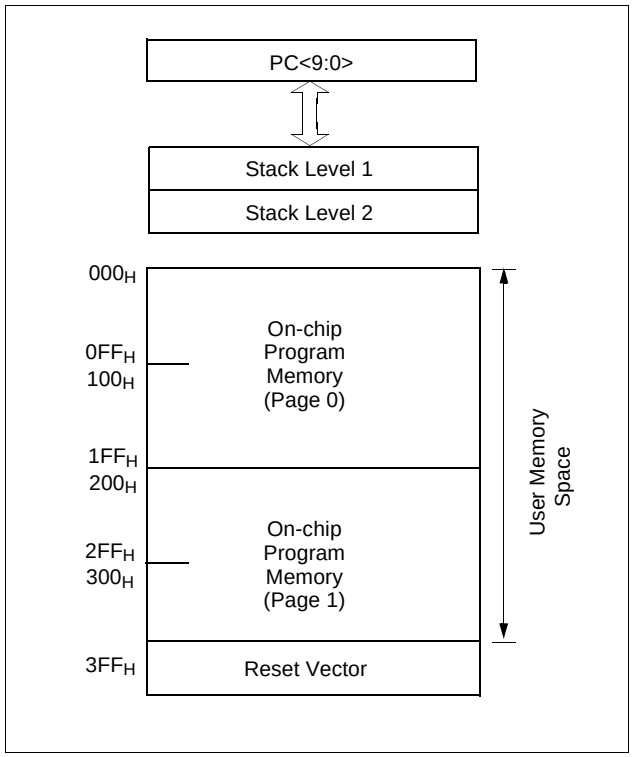


FIGURE 9-2 HMS77C1001A PROGRAM MEMORY MAP AND STACK

9.2 Data Memory

The data memory consists of 25 bytes of RAM and seven special function registers. The data memory locations are addressed directly or indirectly by using FSR.

Figure 9-3 shows a map of data memory. The special function registers are mapped into the data memory..

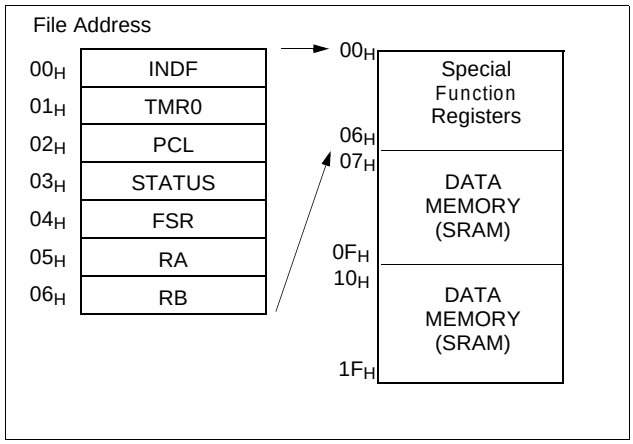


FIGURE 9-3 HMS77C100XA DATA MEMORY MAP

9.3 Special Function Registers

This devices has seven special function register that are the INDF register, the Program Counter(PC), the STATUS register, File Select Register(FSR), 8-bit Timer(TMR0), and I/O data register(RA, RB).

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 9-1).

TMR0, RA and RB are not in the G700 CPU. They are located in each peripheral function blocks. All special function register are placed on data memory map. The INDF register is not a physical register and this register is used for indirect addressing mode...

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset	$\overline{\text{RESET}}$ and WDT Reset
TRIS	N/A	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111
OPTION	N/A	Contains control bits to configure Timer0, Timer0/WDT prescaler and PFD								0011 1111	0011 1111
INDF	00_H	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
TMR0	01_H	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
PCL	02_H	Low order 8bits of PC								1111 1111	1111 1111
STATUS	03_H	-	-	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
FSR	04_H	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
RA	05_H	-	-	-	-	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
RB	06_H	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu

TABLE 9-1 SPECIAL FUNCTION REGISTER SUMMARY

Legend : Shaded boxes = unimplemented or unused, - = unimplemented, read as '0'
x = unknown, u = unchanged, q = see the tables in Section 17 for possible values.

9.3.1 INDF Register

The INDF register is not physically implemented register, used for indirect addressing mode. If the INDF register are accessed, CPU goes to indirect addressing mode. Then CPU accesses the Data memory which address is the contents of FSR.

If the INDF register are accessed in indirect addressing mode(I.e., FSR=00H), 00H will be loaded into data bus. This time, note the arithmetic status bits of STATUS register may be affected.

The FSR<4:0> bits are used to select data memory addresses 00_H to $1F_H$.

HMS77C1000A and HMS77C1001A do not use banking. FSR<7:5> are unimplemented and read as '1's.

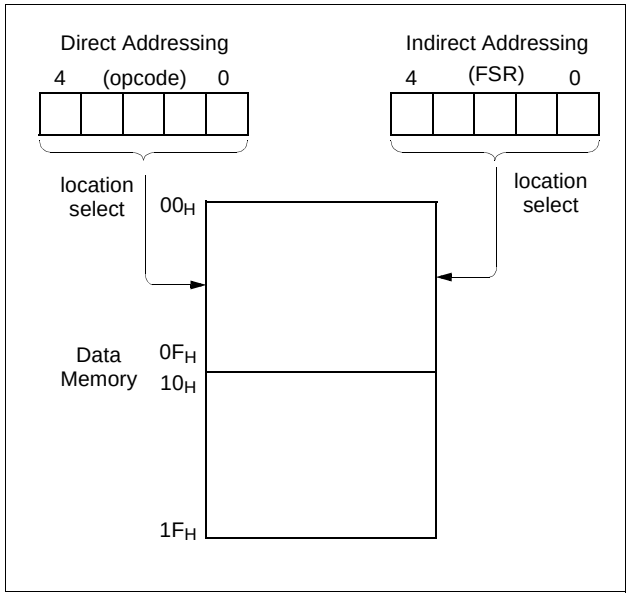


FIGURE 9-4 DIRECT/INDIRECT ADDRESSING

9.3.2 TMR0 Register

The TMR0 register is a data register for 8-bit timer/ counter. In reset state, the TMR0 register is initialized with "00_H".

9.3.3 Program Counter (PC)

The program counter contains the 10-bit address of the instruction to be executed(9-bit address for HMS77C1000A).

The lower 8 bits of the program counter are contained in the PCL register which can be provided by the instruction word for a call instruction, or any instruction where the PCL is the destination while the ninth bit of the program counter comes from the page address bit - PA0 of the STATUS register(HMS77C1001A only).

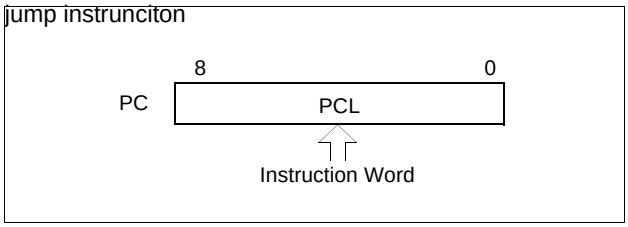
This is necessary to cause program branches across program memory page boundaries.

Prior to the execution of a branch operation, the user must initialize the PA0 bit of STATUS register.

The eighth bit of the program counter can come from the instruction word by execution of goto instruction, or can be cleared by execution of call or any instruction where the PCL is the destination.

In reset state, the program counter is initialized with "$1FF_H$"(HMS77C1000A) or "$3FF_H$"(HMS77C1001A).

Note: *Because PC<8> is cleared in the subroutine call instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).*



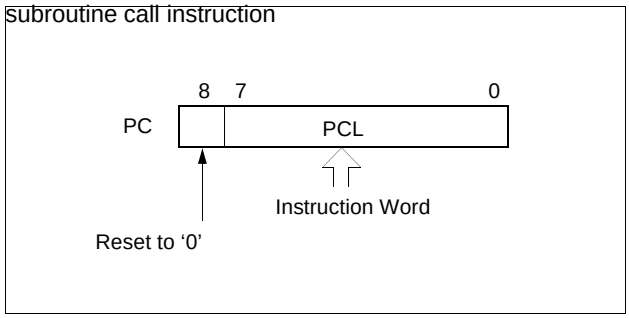


FIGURE 9-5 LOADING OF BRANCH INSTRUCTION - HMS77C1000A

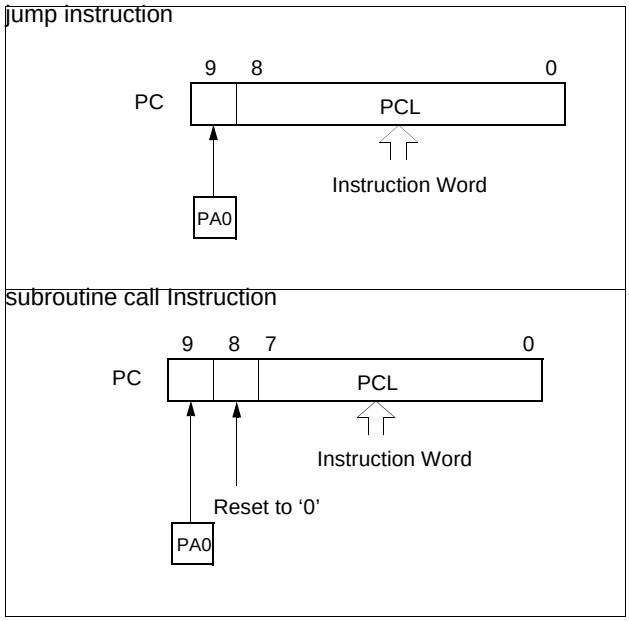


FIGURE 9-6 LOADING OF BRANCH INSTRUCTION - HMS77C1001A

9.3.4 Stack Operation

The HMS77C100XA have a 2-level hardware stack. The stack register consists of two 9-bit save registers(HMS77C1000A), 10-bit save registers(HMS77C1001A). A physical transfer of register contents from the program counter to the stack or vice versa, and within the stack, occurs on call and return instructions. If more than two sequential call instructions are executed, only the most recent two return address are stored. If more than two sequential return instructions are executed, the stack will be filled with the address previously stored in level 2. The stack cannot be read or written by

program.

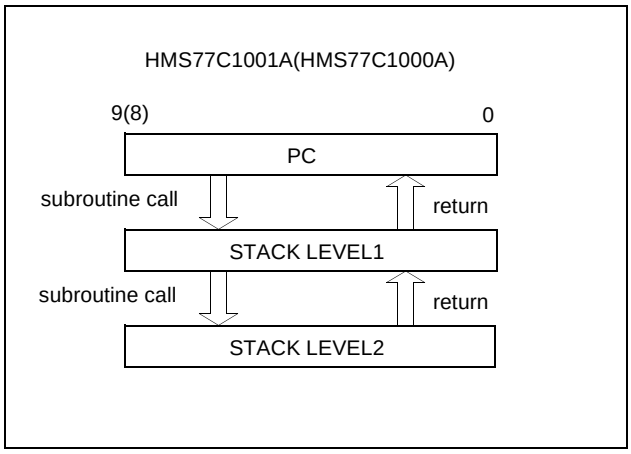


FIGURE 9-7 OPERATION OF 2-LEVEL STACK

9.3.5 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page select bit for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

It is recommended that only instructions that do not affect status of CPU be used on STATUS register. Care should be exercised when writing to the STATUS register as the ALU status bits are updated upon completion of the write operation, possibly leaving the STATUS register with a result that is different than intended. In reset state, the STATUS register is initialized with "$00011XXX_B$".

		R/W	R	R	R/W	R/W	R/W
-	-	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

ADDRESS ; 03_H
RESET VALUE : 0001_1XXX

R = Readable bit
W = Writable bit

PA0: Program memory page select bits
0 = page 0 (000h - 1FFh) - HMS77C1000A/ 1001A
1 = page 1 (200h - 3FFh) - HMS77C1001A

$\overline{TO}$: Time-overflow bit
1 = After power-up, watchdog clear instruction, or entering power-down mode
0 = A watchdog timer time-overflow occurred

$\overline{PD}$: Power-down bit
1 = After power-up or by the watchdog clear instruction
0 = By execution of power-down mode

Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

DC: Digit carry/$\overline{borrow}$ bit
(for addition and subtraction)
addition
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
subtraction
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

C: Carry/$\overline{borrow}$ bit
(for additon,subtraction and rotation)
addition
1 = A carry occurred
0 = A carry did not occur
subtraction
1 = A borrow did not occur
0 = A borrow occurred
rotation
Load bit with LSB or MSB, respectively

FIGURE 9-8 STATUS REGISTER

9.3.6 FSR Register

The FSR register is an 8-bit register. The lower 5 bits are used to store indirect address for data memory. The upper 3 bits are unimplemented and read as "0". Figure 9-9 shows how the FSR register can be used in indirect addressing mode.

In reset state, the FSR register is initialized with "$1XXX\_XXXX_B$".

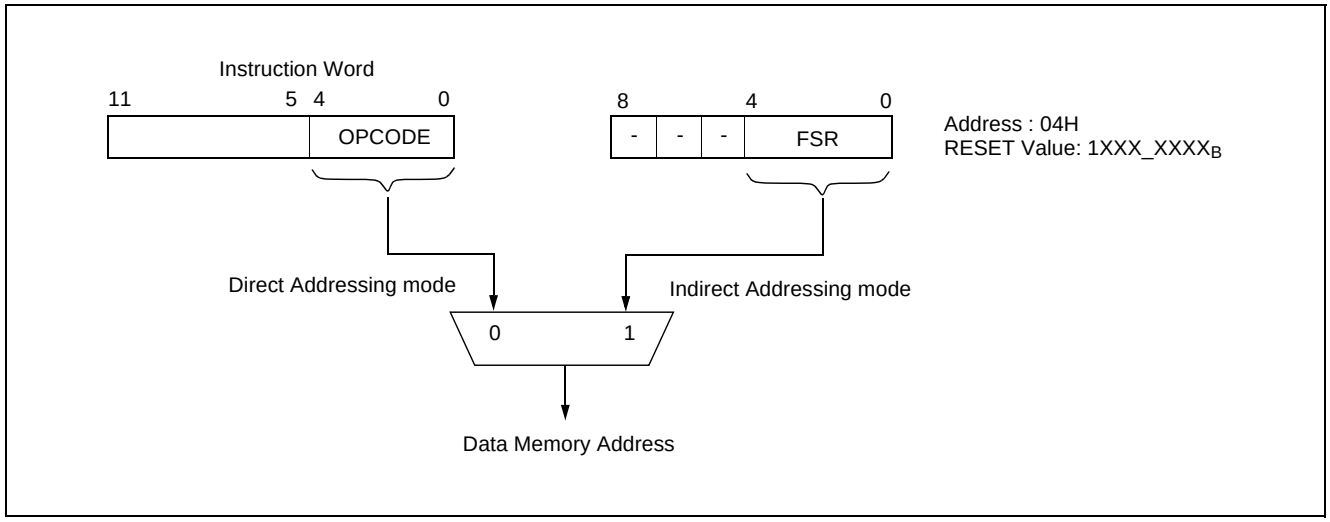


FIGURE 9-9 FSR REGISTER AND DIRECT/INDIRECT ADDRESSING MODE

9.3.7 OPTION Register

The OPTION register consists of 8-bit write-only register and can not addressed. This register is able to control the status of PFD, TMR0/WDT prescaler and TMR0.

To modify the OPTION register, the content of W register are transferred to the OPTION register by executing the OPTION instruction.

In reset state, the OPTION register is initialized with "00111111_B" .

W	W	W	W	W	W	W	W
LOWOPT	PFDEN	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

ADDRESS ; N/A
RESET VALUE : 0011_1111

W = Writable bit
-n = Value at POR reset

LOWOPT: Power-fail detection level select bit.
1 = Lowered detection level (1.8V @ 5V)
0 = Normal detection level (2.7V @ 5V)

PFDEN: Power-fail detection enable bit
1 = Enable power-fail detection
0 = Disable power-fail detection

T0CS: Timer 0 clock source select bit
1 = Transition on EC0 pin
0 = Internal instruction cycle clock

T0SE: Timer 0 source edge select bit
1 = Increment on high-to-low transition on EC0
0 = Increment on low-to-high transition on EC0

PSA: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to the Timer 0

PS2-PS0: Prescaler rate select bits)

Bit Value	Timer 0 rate	WDT rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

FIGURE 9-10 OPTION REGISTER

10. I/O PORTS

The HMS77C100XA has a 4-bit I/O port(RA) and a 8-bit I/O port(RB).

All pin have data(RA,RB) and direction(TRISA,TRISB) registers which can assign these ports as output or input.

A “0” in the port direction registers configure the corresponding port pin as output. Conversely, write “1” to the corresponding bit to specify it as input pin (Hi-Z state).

For example, to use the even numbered bit of RB as output ports and the odd numbered bits as input ports, write “55_H” to TRISB register during initial setting as shown in Figure 10-1.

All the port direction registers in the HMS77C100XA have “1” written to them by reset function. This causes all port as input.

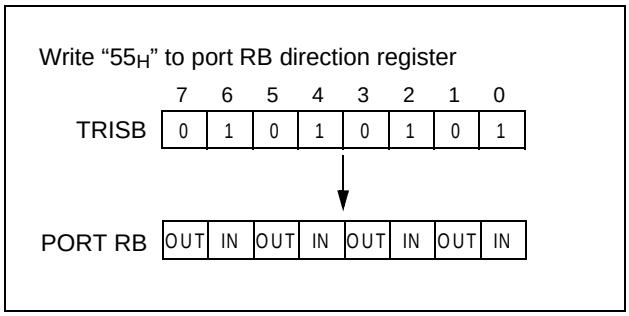


FIGURE 10-1 EXAMPLE OF PORT I/O ASSIGNMENT

10.1 Port RA

RA is a 4-bit I/O register. Each I/O pin can independently used as an input or an output through the port direction register, TRISA. A “0” in the TRISA register configure the corresponding port pin as output. Conversely, write “1”to the corresponding bit to specify it as input pin.

Bits 7-4 are unimplemented and read as '0's.

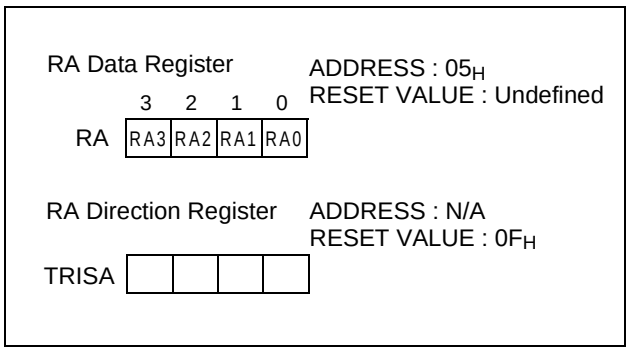


FIGURE 10-2 RA PORT REGISTERS

10.2 Port RB

RB is an 8-bit I/O register. Each I/O pin can independently used as an input or an output through the port direction register, TRISB. A “0” in the TRISB register configure the corresponding port pin as output. Conversely, write “1”to the corresponding bit to specify it as input pin.

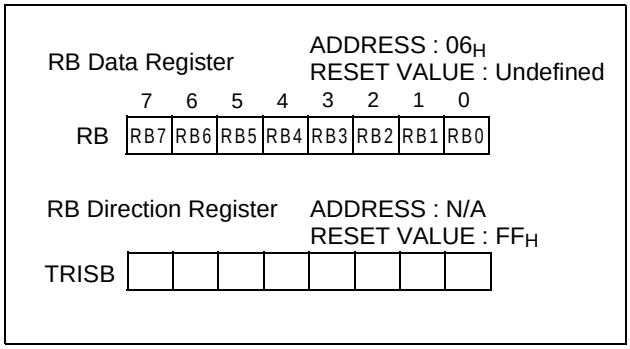


FIGURE 10-3 RB PORT REGISTERS

Note: *A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.*

10.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 10-4. All ports may be used for both input and output operation.

For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output..

10.4 I/O Successive Operations

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 10-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port.

The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed.

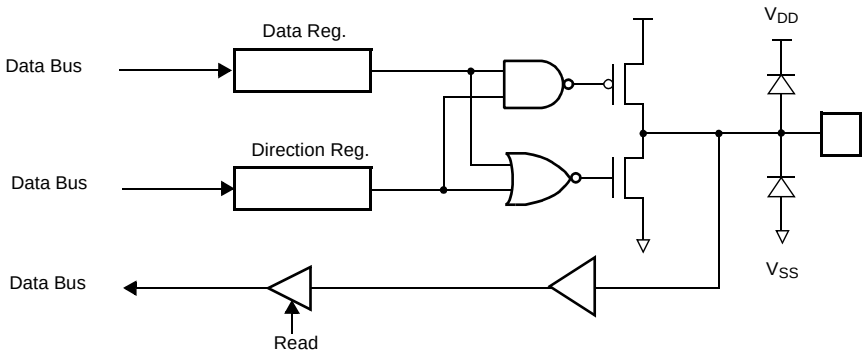


FIGURE 10-4 EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset	$\overline{\text{RESET}}$ and WDT Reset
TRIS	N/A	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111
RA	05_H	-	-	-	-	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
RB	06_H	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu

TABLE 10-1 SUMMARY OF PORT REGISTERS

Legend: Shaded boxes = unimplemented or unused, - = unimplemented, read as '0', x = unknown, u = unchanged.

Otherwise, the previous state of that pin may be read into the CPU rather than the new state.

When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

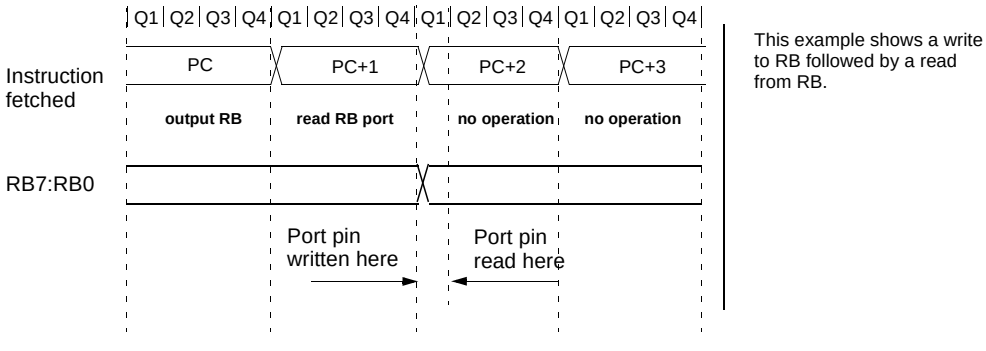


FIGURE 10-5 SUCCESSIVE I/O OPERATION

11. TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- 8-bit software programmable prescaler
- Internal or external clock select
- Edge select for external clock

Figure 11-1 is a simplified block diagram of the Timer0 module, while Figure 11-2 shows the electrical structure of the Timer0 input.

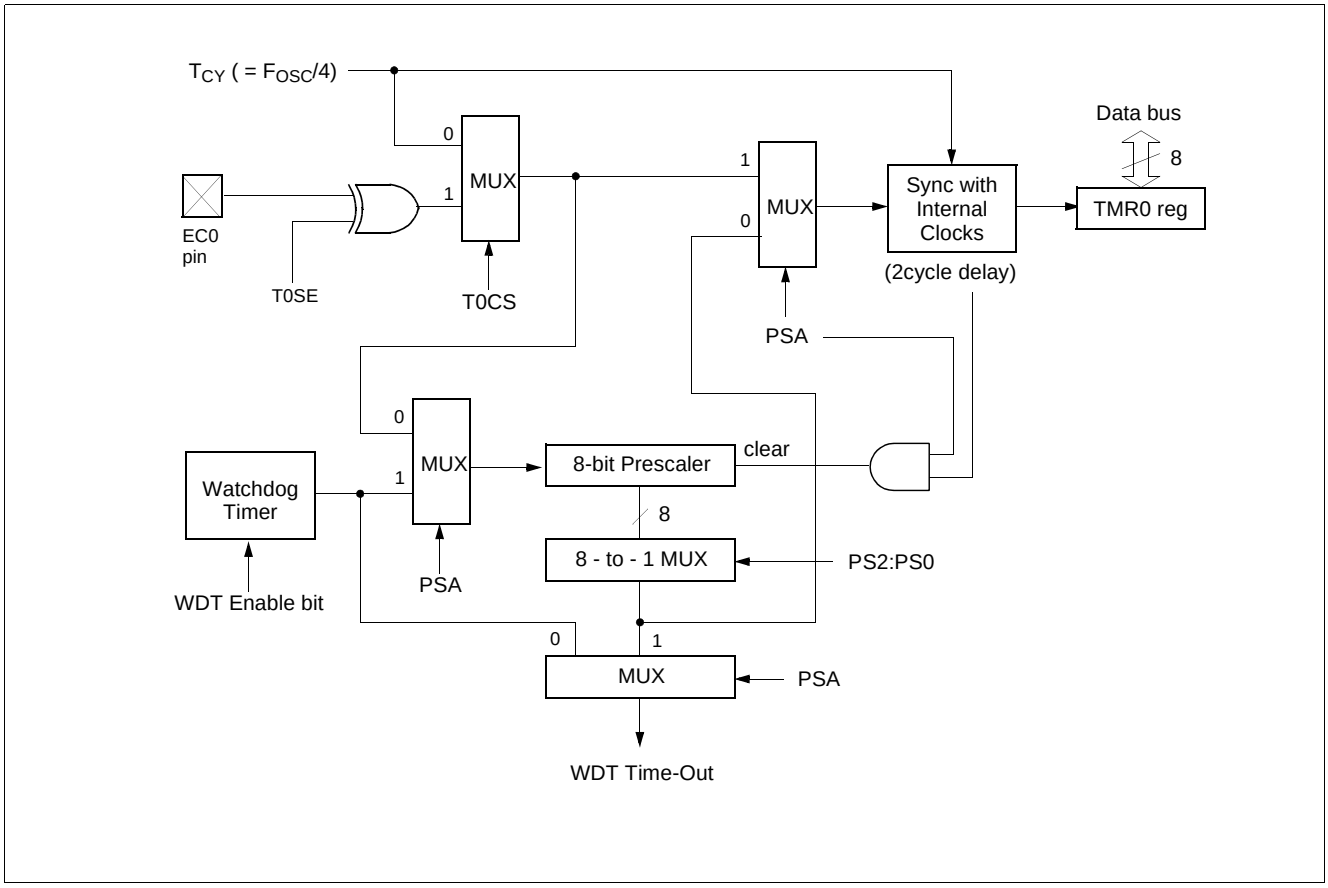


FIGURE 11-1 BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

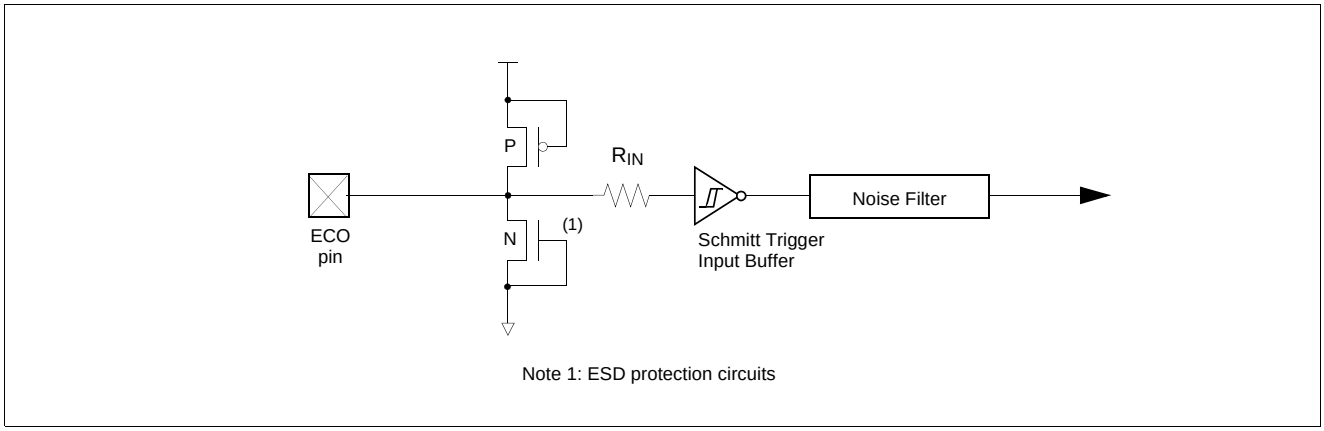


FIGURE 11-2 ELECTRICAL STRUCTURE OF EC0 PIN

11.1 Timer Mode

If the OPTION register bit5(T0CS) is cleared, the timer mode is selected and is operated with internal system clock (T_{CY}). The Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Figure 11-3 and Figure 11-4 show the timing diagram of Timer.

- No Prescaler (PSA=0)
  Timer will increment every instruction cycle(Q4).

- With Prescaler (PSA=1)
  Timer will increment with prescaler division ratio.
  @ PS2~PS0 = (1:2) ~ (1:256)Counter Mode

11.2 Counter Mode

If the OPTION register bit5(T0CS) is set, the counter mode is selected and operates with event clock input.

In this mode, Timer0 will increment either on every rising or falling edge of pin EC0. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge.

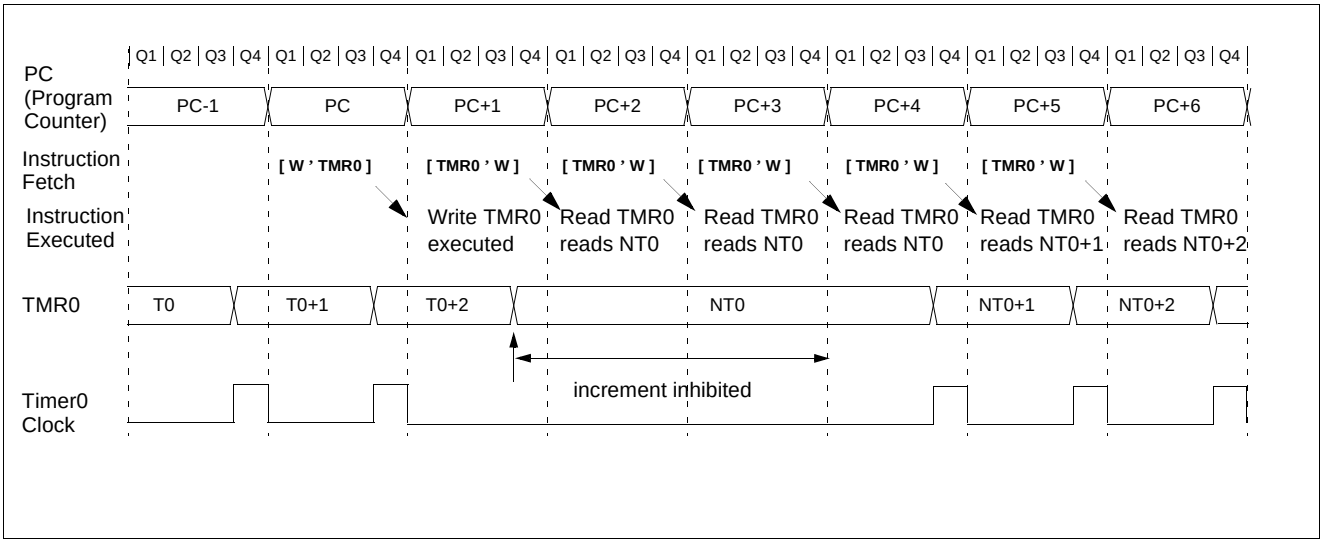


FIGURE 11-3 TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

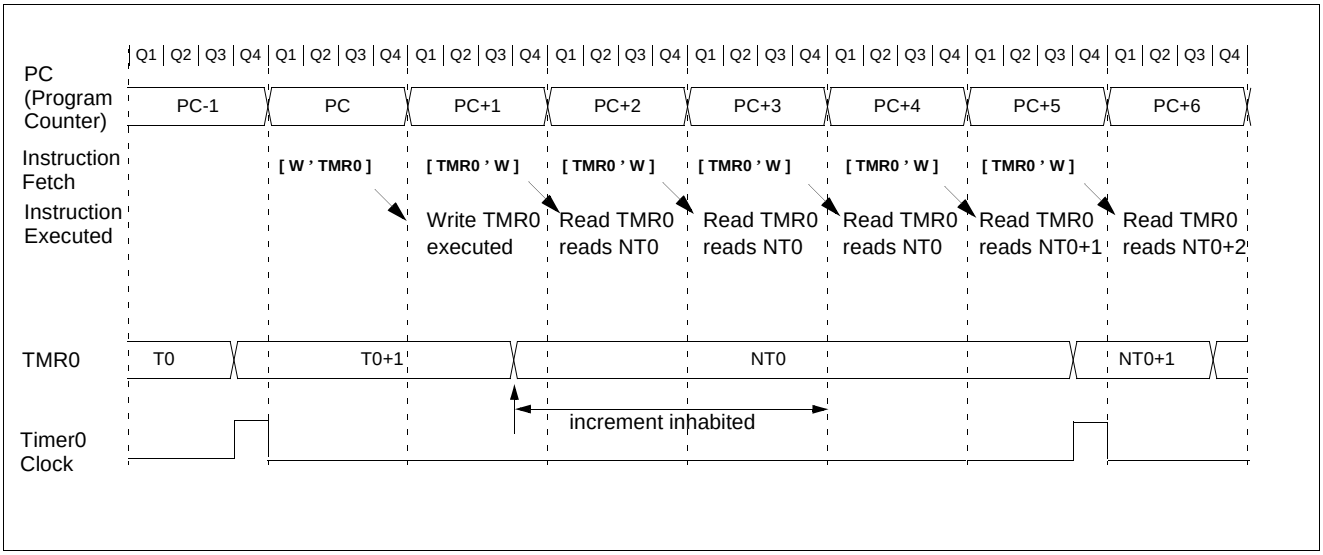


FIGURE 11-4 TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset	$\overline{\text{RESET}}$ and WDT Reset
TMR0	01_H	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
OPTION	N/A	LOWOPT	PFDEN	T0CS	T0SE	PSA	PS2	PS1	PS0	0011 1111	0011 1111

TABLE 11-1 REGISTERS ASSOCIATED WITH TIMER0

Legend: x = unknown, u = unchanged.

11.3 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (T_{OSC}) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

11.3.1 External Clock Synchronization

The synchronization of EC0 input with the internal phase clocks is accomplished by sampling EC0 clock or the prescaler output on the Q2 and Q4 falling of the internal phase clocks.

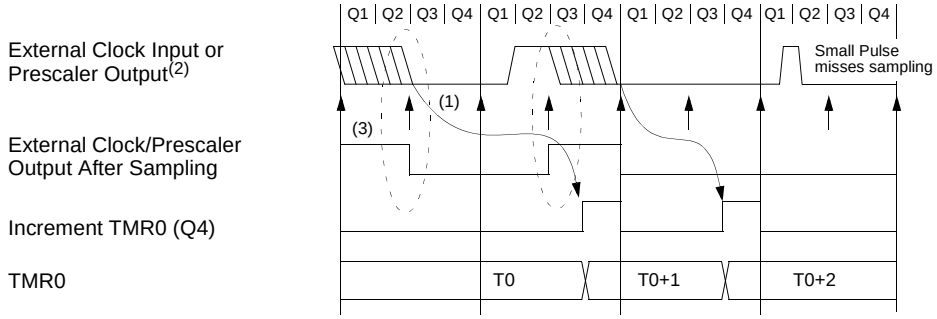
After the synchronization, counter increments on the next instruction cycle (Q4). There is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incrementing. Figure 11-5 shows the synchronization and the increment of the counter mode.

- EC0 clock specification
  - No Prescaler (PSA = 0)
    High or low time(min) ≥ $2T_{XIN}$ + 20ns
  - With Prescaler (PSA = 1)
    High or low time(min) ≥ $4T_{XIN}$ + 40ns

But, there is a noise filter on the EC0 pin, the minimum low or high time(10ns) should be required.

11.3.2 Timer0 Increment Delay

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incrementing. Figure 11-5 shows the delay from the external clock edge to the timer incrementing.



Note 1: Delay from clock input change to TMR0 increment is $3T_{XIN}$ to $7T_{XIN}$. (Duration of Q = T_{XIN}).
Therefore, the error in measuring the interval between two edges on TMR0 input = $\pm 4T_{XIN}$ max.

2: External clock if no prescaler selected, prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

FIGURE 11-5 TIMER0 TIMING WITH EXTERNAL CLOCK

11.4 Prescaler

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is neither readable nor writable.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio. When the prescaler is assigned to the Timer0 module, prescale values of 1:2,

1:4,..., 1:256 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

On a RESET, the prescaler contains all '0's.

12. CONFIGURATION AREA

The device configuration area can be programmed or left unprogrammed to select device configurations such as oscillator type, security bit or watchdog timer enable bit.

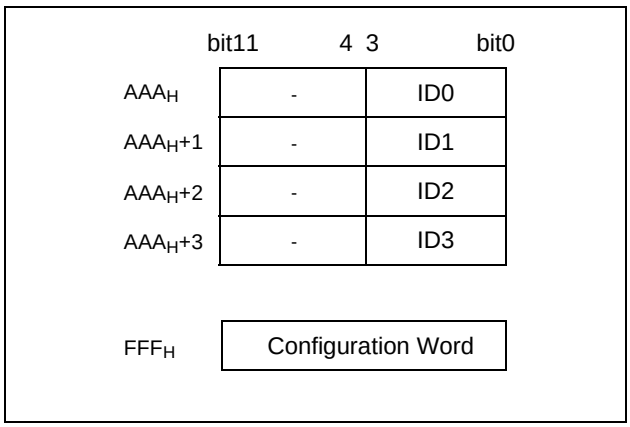


FIGURE 12-1 DEVICE CONFIGURATION AREA

Four memory locations [AAAH ~ $(AAA+3)_H$] are designated as customer ID recording locations where the user can store check-sum or other customer identification numbers. These area are not accessible during normal execution but are readable and writable during program/verify mode. It is recommended that only the 4 least significant bits of ID recording locations are used.

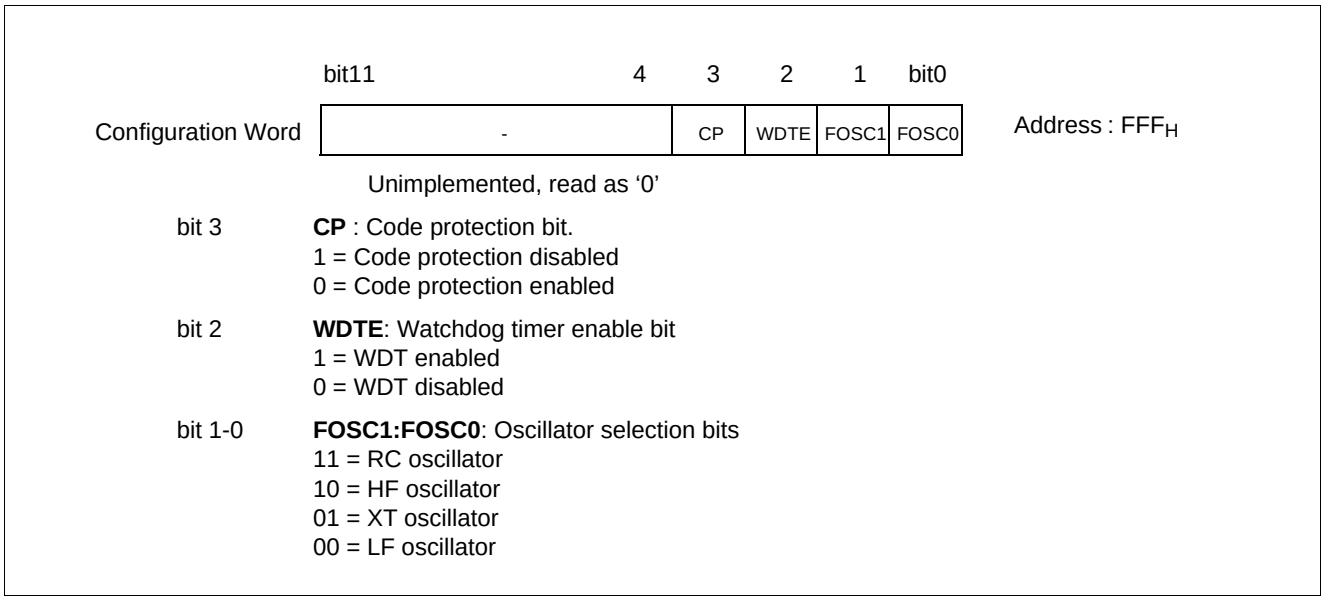


FIGURE 12-2 CONFIGURATION WORD FOR HMS77C100XA

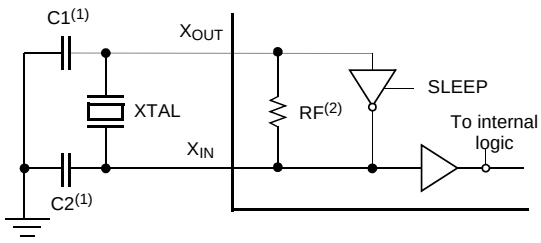
13. OSCILLATOR CIRCUITS

HMS77C100XA supports four user-selectable oscillator modes. The oscillator modes are selected by programming the appropriate values into the configuration word.

- XT : Crystal/Resonator
- HF : High Speed Crystal/Resonator
- LF : Low Speed and Low Power Crystal
- RC : External Resistor/Capacitor

13.1 XT, HF or LF Mode

In XT, LF or HF modes, a crystal or ceramic resonator is connected to the X_{IN} and X_{OUT} pins to establish oscillation (Figure 13-1). The HMS77C100XA oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. Bits 0 and 1 of the configuration register (FOSC1:FOSC2) are used to configure the different external resonator/crystal oscillator modes. These bits allow the selection of the appropriate gain setting for the internal driver to match the desired operating frequency. When in XT, LF or HF modes, the device can have an external clock source drive the X_{IN} pin (Figure 13-2). In this case, the X_{OUT} pin should be left open.



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.

2: RF varies with the crystal chosen (approx. value = 9 MΩ).

FIGURE 13-1 CRYSTAL OR CERAMIC RESONATOR (HF, XT OR LF OSC CONFIGURATION)

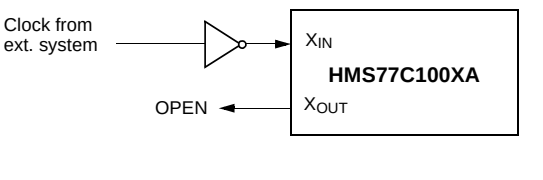


FIGURE 13-2 EXTERNAL CLOCK INPUT OPERATION (HF, XT OR LF OSC CONFIGURATION)

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
XT	455 kHz 2.0 MHz 4.0 MHz	22-100 pF 15-68 pF 15-68 pF	22-100 pF 15-68 pF 15-68 pF
HF	4.0 MHz 8.0 MHz 16.0 MHz	15-68 pF 10-68 pF 10-22 pF	15-68 pF 10-68 pF 10-22 pF

TABLE 13-1 CAPACITOR SELECTION FOR CERAMIC RESONATORS

Note: *These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.*

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LF	32 kHz[1] 100 kHz 200 kHZ	15 pF 15-30 pF 15-30 pF	15 pF 30-47 pF 15-82 pF
XT	100 kHz 200 kHz 455 kHz 1 MHz 2 MHz 4 MHz	15-30 pF 15-30 pF 15-30 pF 15-30 pF 15-30 pF 15-47 pF	200-300 pF 100-200 pF 15-100 pF 15-30 pF 15-30 pF 15-47 pF
HF	4 MHz 8 MHz 20 MHz	15-30 pF 15-30 pF 15-30 pF	15-30 pF 15-30 pF 15-30 pF

TABLE 13-2 CAPACITOR SELECTION FOR CRYSTAL

1. *For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.*

Note: *These values are for design guidance only. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.*
If you change from this device to another device, please verify oscillator characteristics in your application.

13.2 RC Oscillation Mode

The external RC oscillator mode provides a cost-effective approach for applications that do not require a precise operating frequency. In this mode, the RC oscillator frequen-

cy is a function of the supply voltage, the resistor(R) and capacitor(C) values, and the operating temperature.

In addition, the oscillator frequency will vary from unit to unit due to normal manufacturing process variations. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low C values. The external R and C component tolerances contribute to oscillator frequency variation as well.

The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 13-3 shows how the R is connected to the HMS77C100XA. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ. Table 13-3 shows recommended value of Rext and Cext.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), it is recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

Cext	Rext	Average F_{XIN} @ 5V, 25°C
0pF	3.3K 5K 15K 100K	6.5MHz 5.4MHz 2.3MHz 400KHz
20pF	3.3K 5K 15K 100K	4.3MHz 3.5MHz 1.4MHz 240KHz
100pF	3.3K 5K 15K 100K	1.8MHz 1.5MHz 610KHz 100KHz
300pF	3.3K 5K 15K 100K	780KHz 630KHz 260KHz 42.5KHz

TABLE 13-3 RC OSCILLATION FREQUENCIES

The Electrical Specifications sections show R frequency variation from part to part due to normal process variation.

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the X_{OUT} pin, and can be used for test purposes or to synchronize other logic.

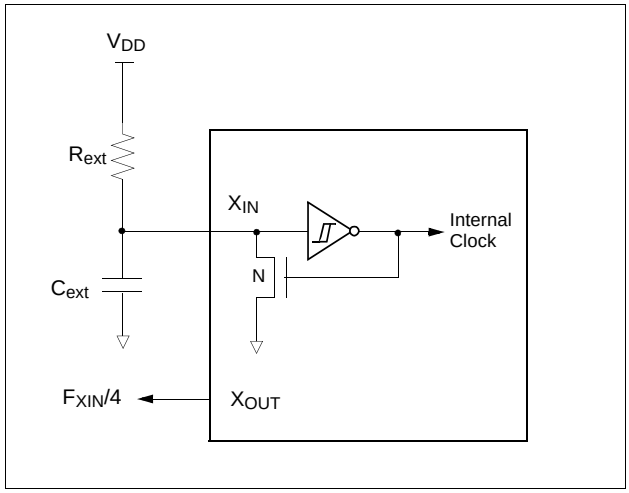


FIGURE 13-3 RC OSCILLATION MODE

14. RESET

HMS77C100XA devices may be reset in one of the following ways:

- Power-On Reset (POR)
- Power-Fail detect reset (PFDR)
- $\overline{\text{RESET}}$ (normal operation)
- $\overline{\text{RESET}}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

Each one of these reset conditions causes the program counter to branch to reset vector address. (HMS77C1000A is $1FF_H$ and HMS77C1001A is $3FF_H$).

Table 14-1 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-On Reset (POR), PFDR, $\overline{\text{RESET}}$ or WDT reset. A $\overline{\text{RESET}}$ or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions. These bits may be used to determine the nature of the reset.

Table 14-2 lists a full description of reset states of all registers. Figure 14-1 shows a simplified block diagram of the on-chip reset circuit.

Condition	PCL Addr: 02_H	STATUS Addr: 03_H
Power-On Reset	1111 1111	0001 1xxx
$\overline{\text{RESET}}$ reset or PFD reset (normal operation)	1111 1111	000u uuuu[1]
$\overline{\text{RESET}}$ wake-up or PFD reset (from SLEEP)	1111 1111	0001 0uuu
WDT reset (normal operation)	1111 1111	0000 uuuu[2]
WDT wake-up (from SLEEP)	1111 1111	0000 0uuu

TABLE 14-1 RESET CONDITIONS FOR SPECIAL REGISTERS

1. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits retain their last value until one of the other reset conditions occur.
2. The CLRWDT instruction will set the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits.

Legend : x = unknown, u = unchanged.

Register	Address	Power-On Reset	Wake-up Reset	$\overline{\text{RESET}}$, PFDR, WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111	1111 1111
OPTION	N/A	0011 1111	0011 1111	0011 1111
INDF	00_H	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0	01_H	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL[1]	02_H	1111 1111	1111 1111	1111 1111
STATUS[1]	03_H	0001 1xxx	100q quuu	000q quuu
FSR	04_H	1xxx xxxx	1uuu uuuu	1uuu uuuu
PORTA	05_H	---- xxxx	---- uuuu	---- uuuu
PORTB	06_H	xxxx xxxx	uuuu uuuu	uuuu uuuu
General Purpose Register Files	$07\text{-}1F_H$	xxxx xxxx	uuuu uuuu	uuuu uuuu

TABLE 14-2 RESET CONDITIONS FOR ALL REGISTERS

1. See Table 14-1 for reset value for specific conditions.

Legend : - = unimplemented, read as '0', x = unknown, u = unchanged.
q = see the tables in Section 17 for possible values.

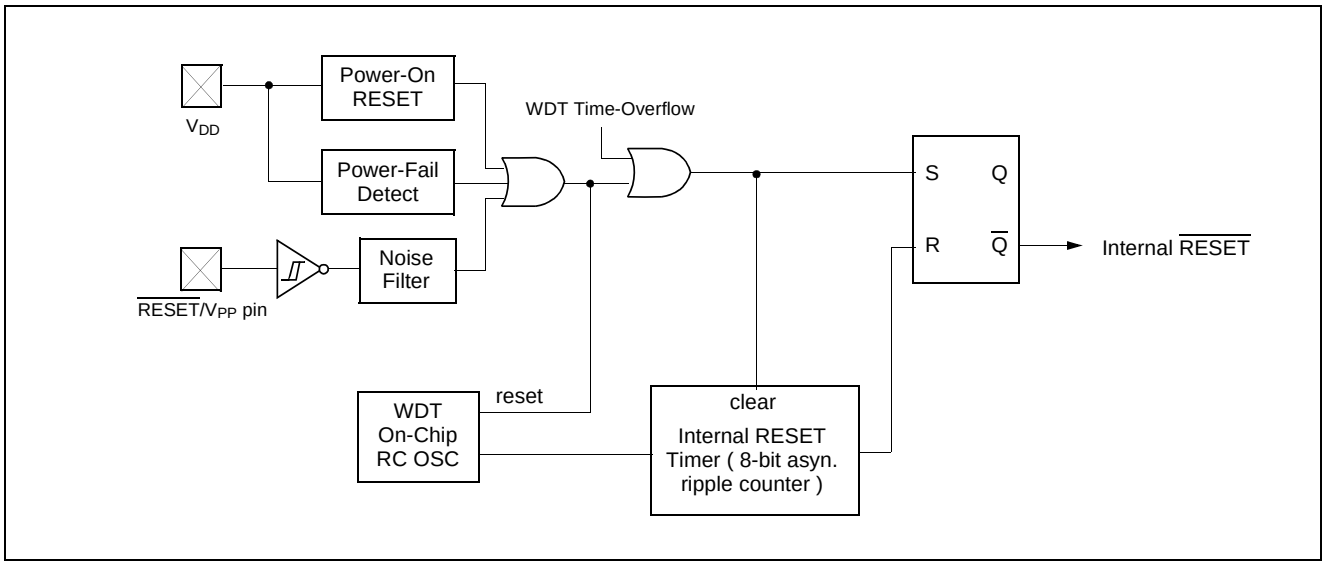


FIGURE 14-1 SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

14.1 Power-On Reset (POR)

The HMS77C100XA family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations. To use this feature, the user merely ties the $\overline{RESET}/V_{PP}$ pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 14-1.

The Power-On Reset circuit and the Internal Reset Timer circuit are closely related. On power-up, the reset latch is set and the IRT is reset. The IRT timer begins counting once it detects $\overline{RESET}$ to be high. After the time-out period, which is typically 7 ms (oscillation stabilization time), it will reset the reset latch and thus end the on-chip reset signal.

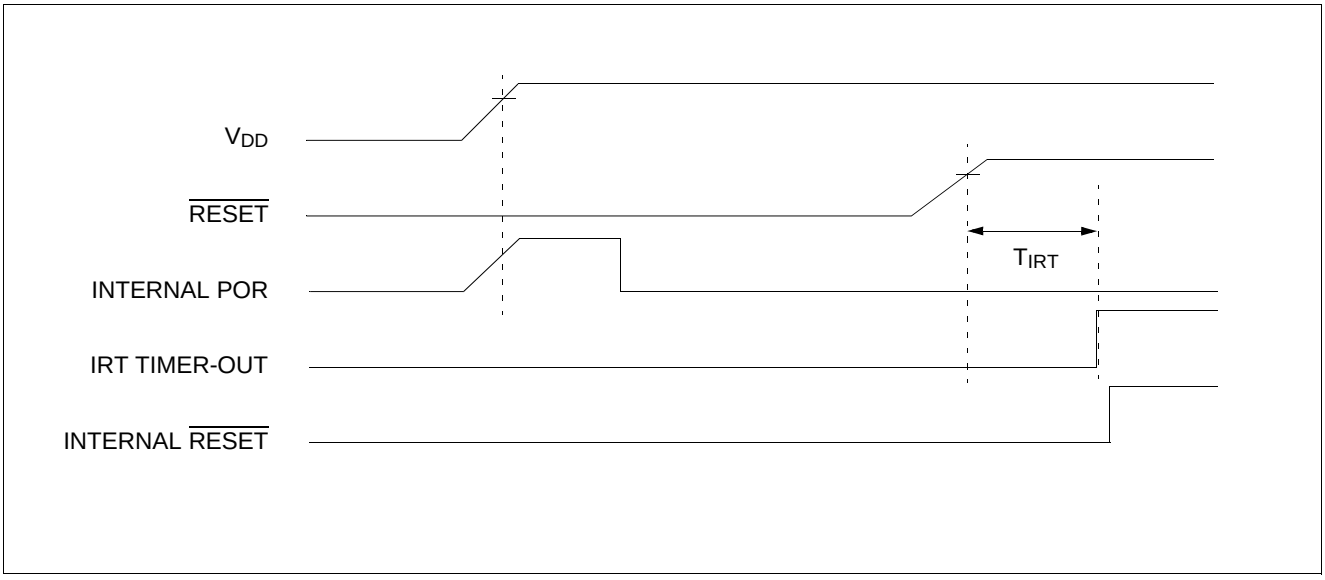


FIGURE 14-2 TIME-OUT SEQUENCE ON POWER-UP ($\overline{RESET}$ NOT TIED TO V_{DD})

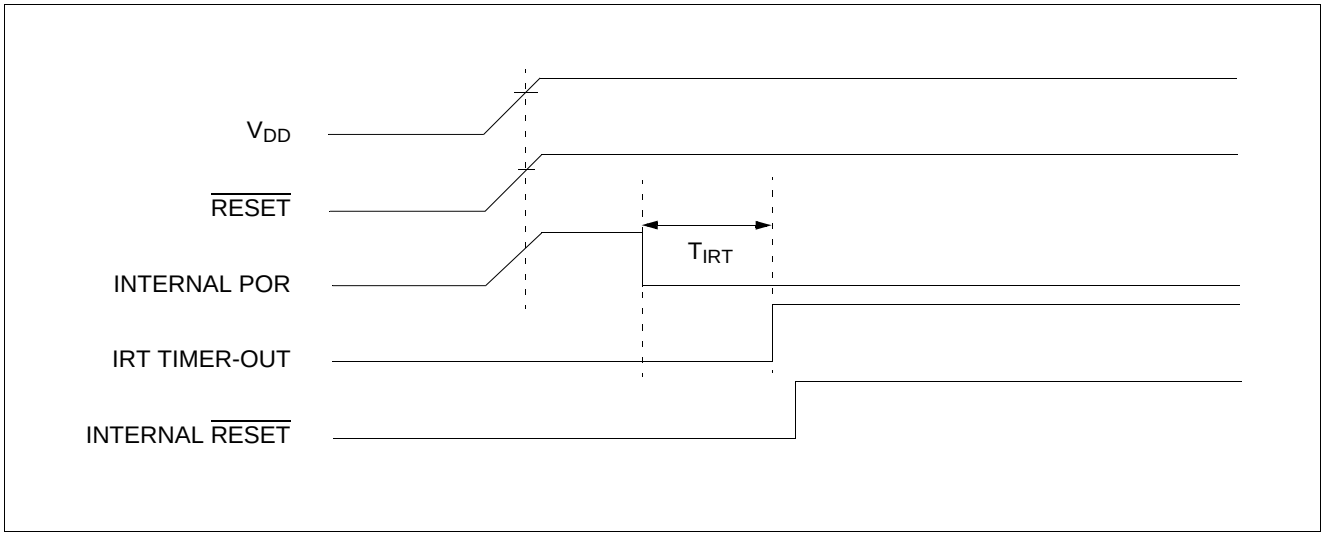


FIGURE 14-3 TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{RESET}}$ TIOED TO V_{DD}): FAST V_{DD} RISE TIME

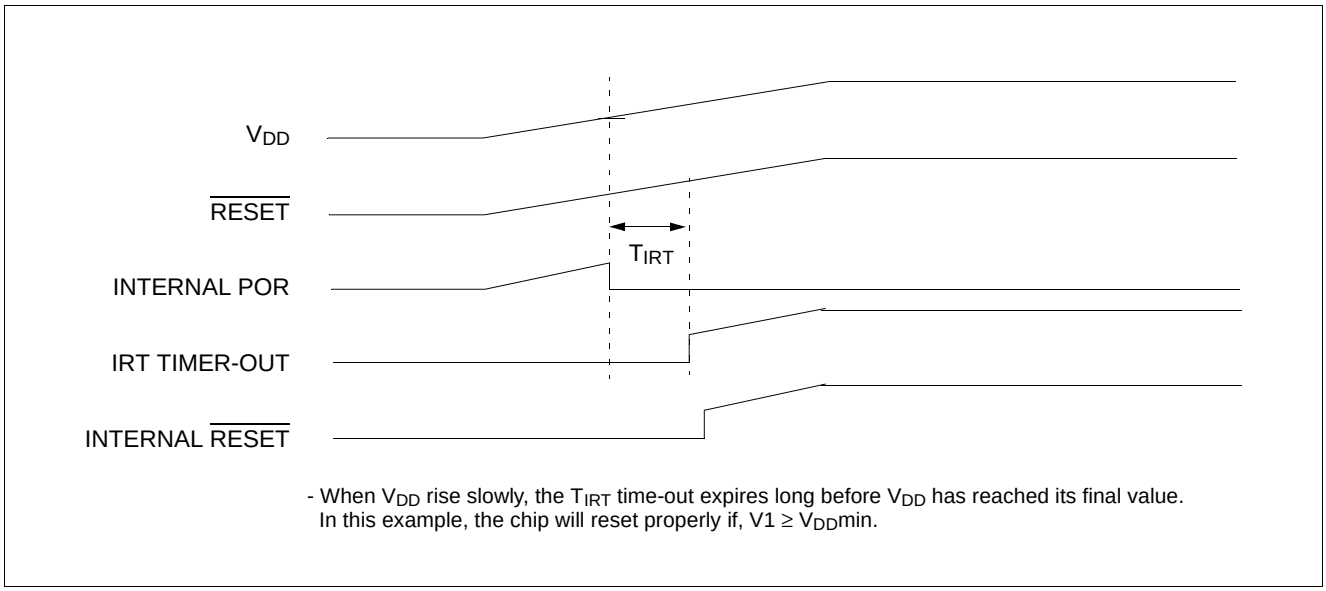


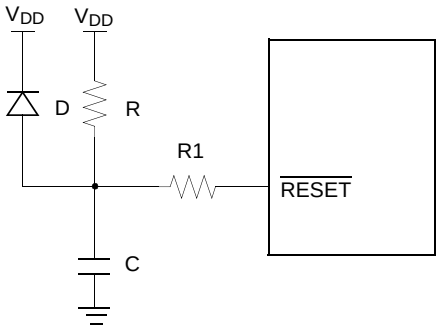
FIGURE 14-4 TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{RESET}}$ TIOED TO V_{DD}): SLOW V_{DD} RISE TIME

A power-up example where $\overline{\text{RESET}}$ is not tied to VDD is shown in Figure 14-2. VDD is allowed to rise and stabilize before bringing $\overline{\text{RESET}}$ high. The chip will actually come out of reset TIRT after $\overline{\text{RESET}}$ goes high and POR, PFDR is released.

In Figure 14-3, the on-chip Power-On Reset feature is being used ($\overline{\text{RESET}}$ and VDD are tied together). The VDD is stable before the internal reset timer times out and there is no problem in getting a proper reset. However, Figure 14-4 depicts a problem situation where VDD rises too slowly. The time between when the IRT senses a high on the $\overline{\text{RESET}}$/V_{PP} pin, and when the $\overline{\text{RESET}}$/V_{PP} pin (and VDD) actually reach their full value, is too long. In this situation, when the internal reset timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external R circuits be used to achieve longer POR delay times (Figure 14-5).

Note: *When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.*

The POR circuit does not produce an internal reset when V_{DD} declines.



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100W to 1 kW will limit any current flowing into RESET from external capacitor C in the event of RESET pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 14-5 EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER- UP)

14.2 Internal Reset Timer (IRT)

The Internal Reset Timer (IRT) provides a fixed 7 ms nominal time-out on reset. The IRT operates on an internal RC oscillator. The processor is kept in RESET as long as the IRT is active. The IRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip IRT keeps the device in a RESET condition for approximately 7 ms after the voltage on the $\overline{RESET}/V_{PP}$ pin has reached a logic high (V_{IH}) level and POR released. Thus, external RC networks connected to the $\overline{RESET}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications. The Device Reset time delay will vary from chip to chip due to V_{DD}, temperature, and process variation.

The IRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the HMS77C100XA from SLEEP mode automatically.

15. WATCHDOG TIMER (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the X_{IN} pin. That means that the WDT will run even if the clock on the X_{IN} and X_{OUT} pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Figure 12-2). Refer to the HMS77C100XA Programming Specifications to determine how to access the configuration word.

15.1 WDT Period

The WDT has a nominal time-out period of 14 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:256 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 3.5 seconds can be realized. These periods vary with temperature, V_{DD} and part-to-part process variations (see DC specs).

Under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

15.2 WDT Programming Considerations

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

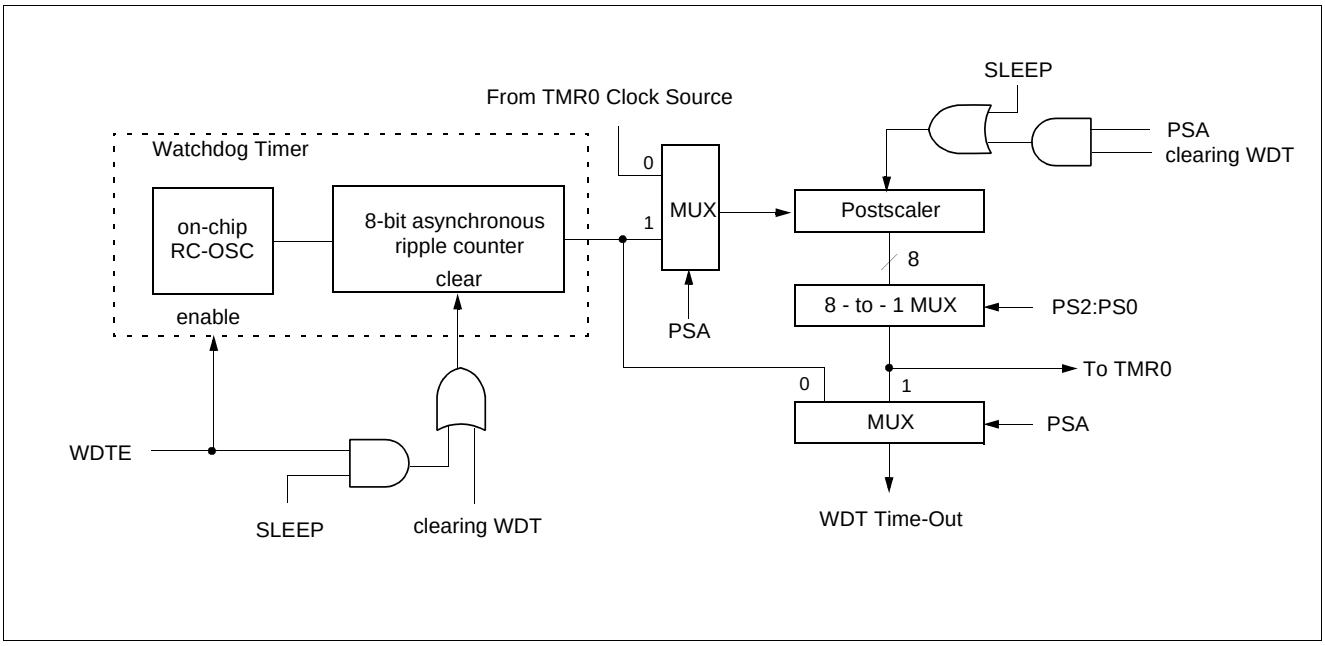


FIGURE 15-1 WATCHDOG TIMER BLOCK DIAGRAM

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Power-On Reset	$\overline{RESET}$ and WDT Reset
OPTION	N/A	LOWOPT	PFDEN	T0CS	T0SE	PSA	PS2	PS1	PS0	0011 1111	0011 1111

TABLE 15-1 SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

16. Power-Down Mode (SLEEP)

For applications where power consumption is a critical factor, device provides power down mode with Watchdog operation. Executing of SLEEP Instruction is entrance to SLEEP mode. In the SLEEP mode, oscillator is turn off and system clock is disable and all functions is stop, but all registers and RAM data is held. The wake-up sources from SLEEP mode are external $\overline{\text{RESET}}$ pin reset and watchdog time-overflow reset.

16.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction. If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{\text{TO}}$ bit (STATUS<4>) is set, the $\overline{\text{PD}}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{\text{RESET}}$ pin low.

For lowest current consumption while powered down, the EC0 input should be at V_{DD} or V_{SS} and the $\overline{\text{RESET}}$ pin must be at a logic high level .

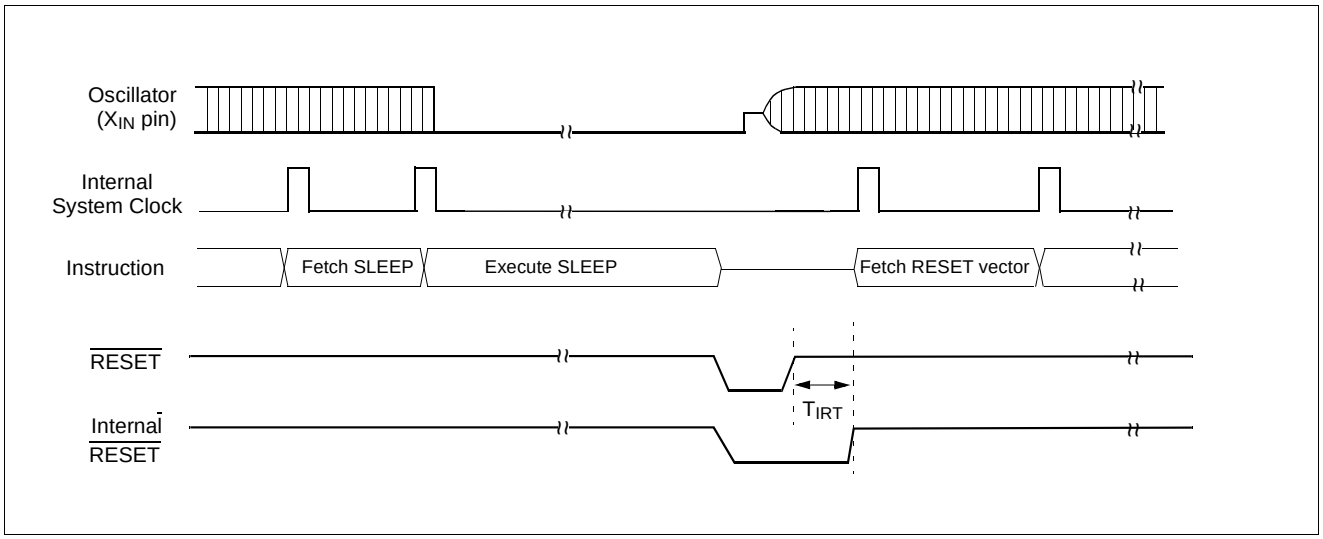


FIGURE 16-1 TIMING DIAGRAM OF WAKE-UP FROM SLEEP MODE DUE TO EXTERNAL $\overline{\text{RESET}}$ PIN RESET

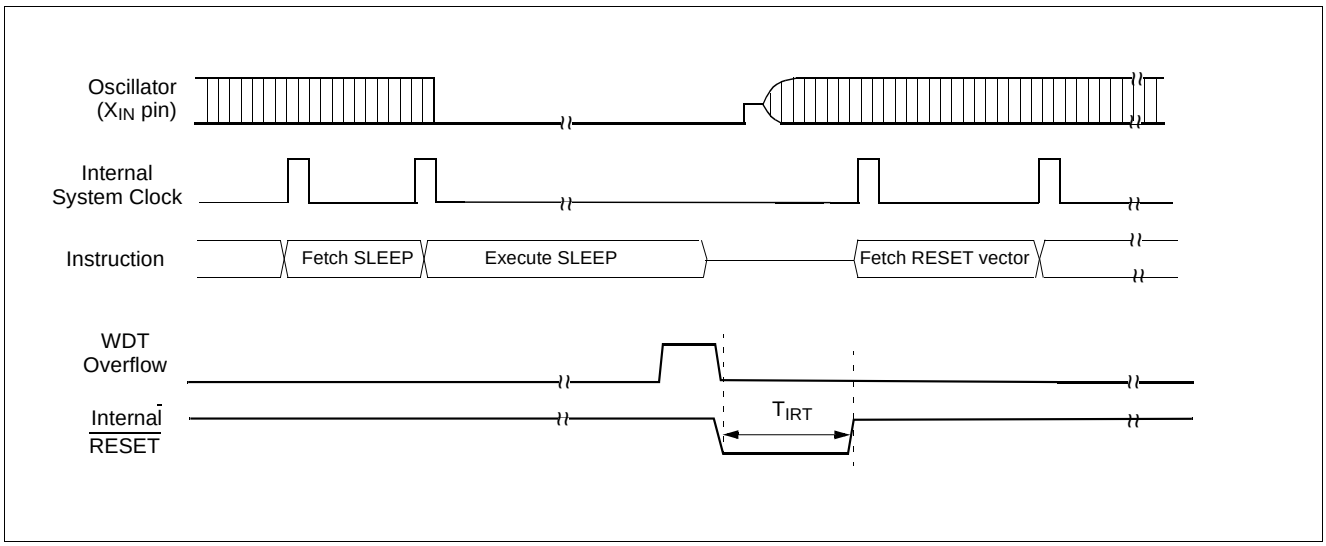


FIGURE 16-2 TIMING DIAGRAM OF WAKE-UP FROM SLEEP MODE DUE TO WATCHDOG TIME-OVERFLOW RESET

16.2 Wake-up From SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external reset input on $\overline{\text{RESET}}$ pin.
2. A Watchdog Timer time-out reset (if WDT was enabled).
3. PFD reset

Both of these events cause a device reset. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits can be used to determine the cause of device reset. The $\overline{\text{TO}}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

16.3 Minimizing Current Consumption

The SLEEP mode is designed to reduce power consumption. To minimize current drawn during SLEEP mode, the user should turn-off output drivers that are sourcing or sinking current, if it is practical.

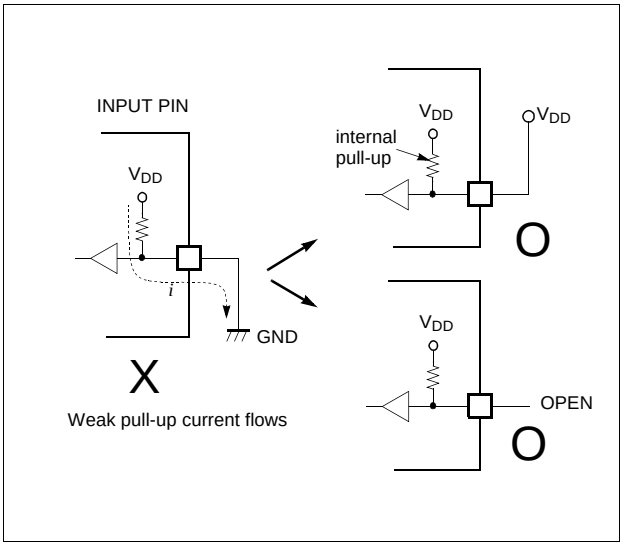
It should be set properly that current flow through port doesn't exist.

First conseider the setting to input mode. Be sure that there is no current flow after considering its relationship with external circuit. In input mode, the pin impedance viewing from external MCU is very high that the current doesn't flow.

But input voltage level should be V_{SS} or V_{DD}. Be careful that if unspecified voltage, i.e. if uncertain voltage level (not V_{SS}or V_{DD}) is applied to input pin, there can be little current (max. 1mA at around 2V) flow.

Note: *In the* SLEEP *operation, the power dissipation associated with the oscillator and the internal hardware is lowered; however, the power dissipation associated with the pin interface (depending on the external circuitry and program) is not directly determined by the hardware operation of the* SLEEP *feature. This point should be little current flows when the input level is stable at the power voltage level (V_{DD}/V_{SS}); however, when the input level becomes higher than the power voltage level (by approximately 0.3V), a current begins to flow. Therefore, if cutting off the output transistor at an I/O port puts the pin signal into the high-impedance state, a current flow across the ports input transistor, requiring it to fix the level by pull-up or other means.*

If it is not appropriate to set as an input mode, then set to output mode considering there is no current flow. Setting to High or Low is decided considering its relationship with external circuit. For example, if there is external pull-up resistor then it is set to output mode, i.e. to high, and if there is external pull-down register, it is set to low.



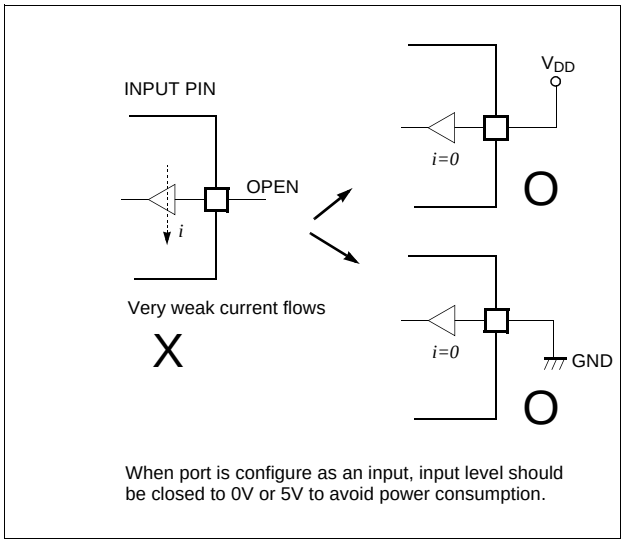
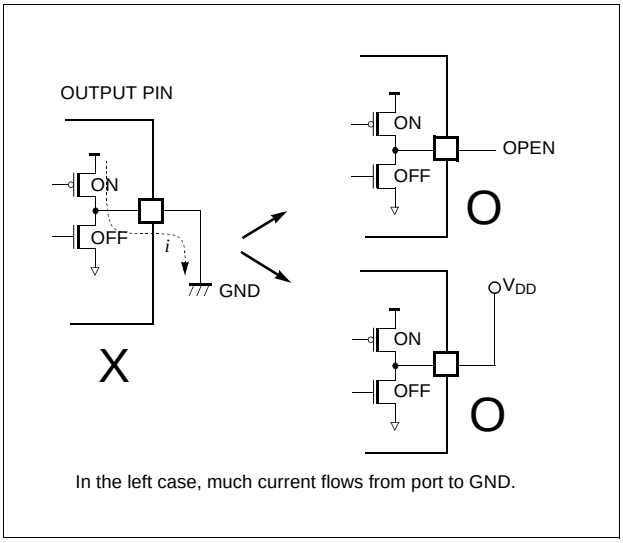


FIGURE 16-3 APPLICATION EXAMPLE OF UNUSED INPUT PORT



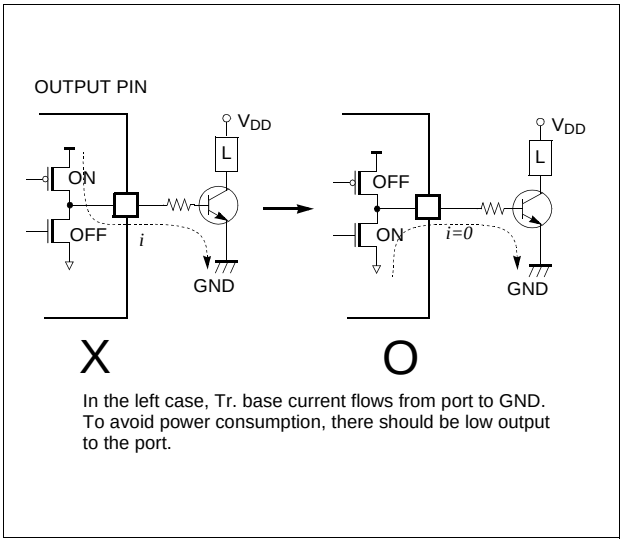


FIGURE 16-4 APPLICATION EXAMPLE OF UNUSED OUTPUT PORT

17. TIME-OUT SEQUENCE AND POWER DOWN STATUS BITS ($\overline{TO}$/$\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{RESET}$ or Watchdog Timer (WDT) reset, or a $\overline{RESET}$ or WDT wake-up reset.

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up(POR)
u	u	$\overline{RESET}$ or PFD reset (normal operation)[1]
1	0	$\overline{RESET}$ Wake-up or PFD reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

TABLE 17-1 $\overline{TO}$/$\overline{PD}$ STATUS AFTER RESET

1. The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{RESET}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

These STATUS bits are only affected by events listed in Table 17-2.

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

TABLE 17-2 EVENTS AFFECTING $\overline{TO}$/$\overline{PD}$ STATUS BITS

Note: *A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit.*

Table 14-1 lists the reset conditions for the special function registers, while Table 14-2 lists the reset conditions for all the registers.

18. POWER FAIL DETECTION PROCESSOR

HMS77C100XA has an on-chip power fail detection circuitry to immunize against power noise.

If V_{DD} falls below a level for longer 100ns, the power fail detection processor may reset MCU and preserve the device from the malfunction due to Power Noise.

OPTION Register

LOWOPT	PFDEN	T0CS	$\overline{\text{T0SE}}$	$\overline{\text{PSA}}$	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

bit 7 **LOWOPT**: Power-fail detection level select bit.
1 = Lowered detection level (typ. 1.8V @ 5V)
0 = Normal detection level (typ. 2.7V @ 5V)

bit 6 **PFDEN**: Power-fail detection enable bit
1 = Enable power-fail detection
0 = Disable power-fail detection

FIGURE 18-1 POWER FAIL DETECTION PROCESSOR

The bit6(PFDEN) of OPTION register activates the PFD Circuit, and bit7(LOWopt) lowers the detection level of the Power Noise. The normal detection level is typically 2.7V and the lowered detection level is typically 1.8V. Figure 18-2 shows a Power Fail Detection Situations where the detection level is selected by LOWOPT Bit.

Note: *The PFD circuit is not implemented on the in circuit emulator, user can not experiment with it. There fore, after final development user program, this function may be experimented on OTP*

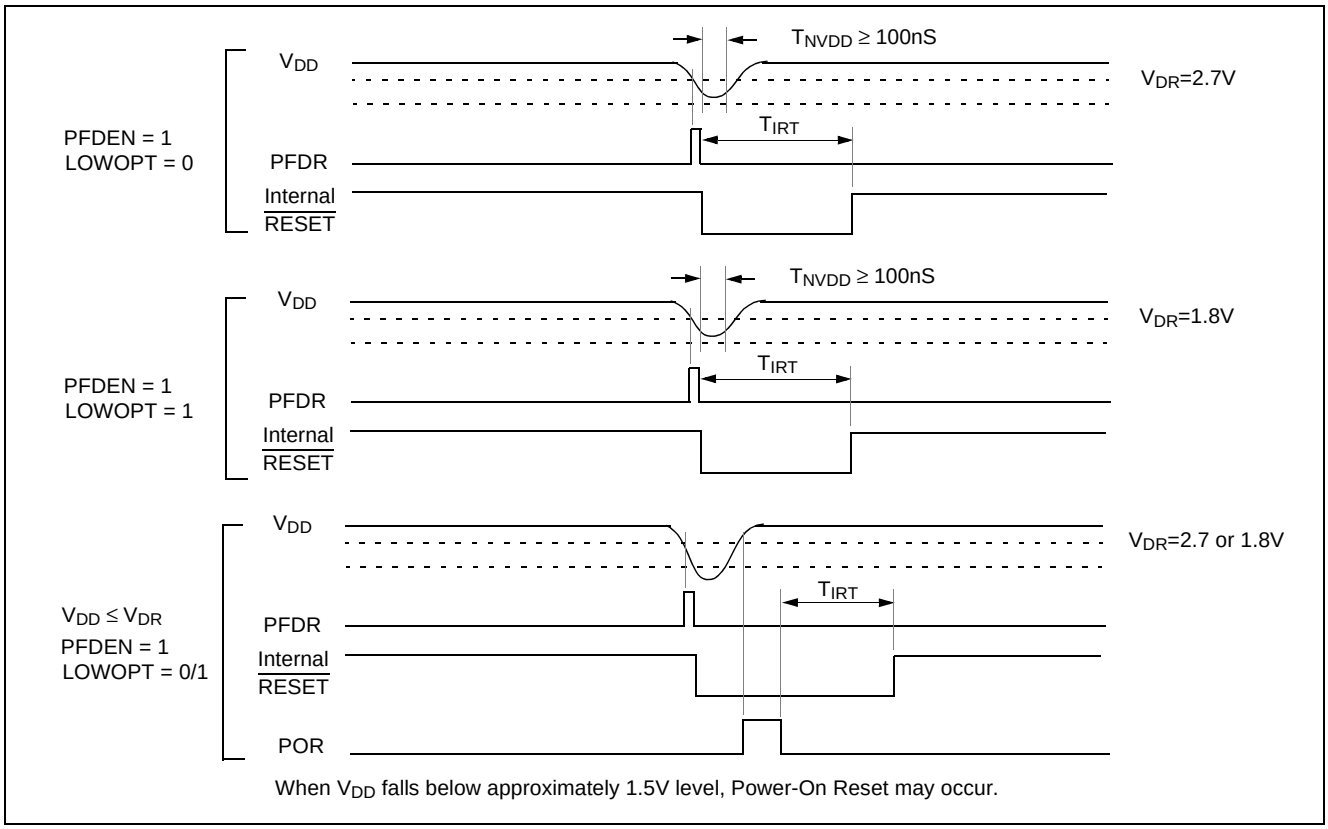


FIGURE 18-2 POWER FAIL DETECTION SITUATIONS