HD74HCT563/HD74HCT573

Octal Transparent Latches (with 3-state outputs)

HITACHI

Description

When the latch enable (LE) input is high, the Q outputs of HD74HCT563 will follow the inversion of the D inputs and the Q outputs of HD74HCT573 will follow the D inputs.

When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enabled returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (D to Q, $\overline{Q}$) = 13 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 4.5 to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

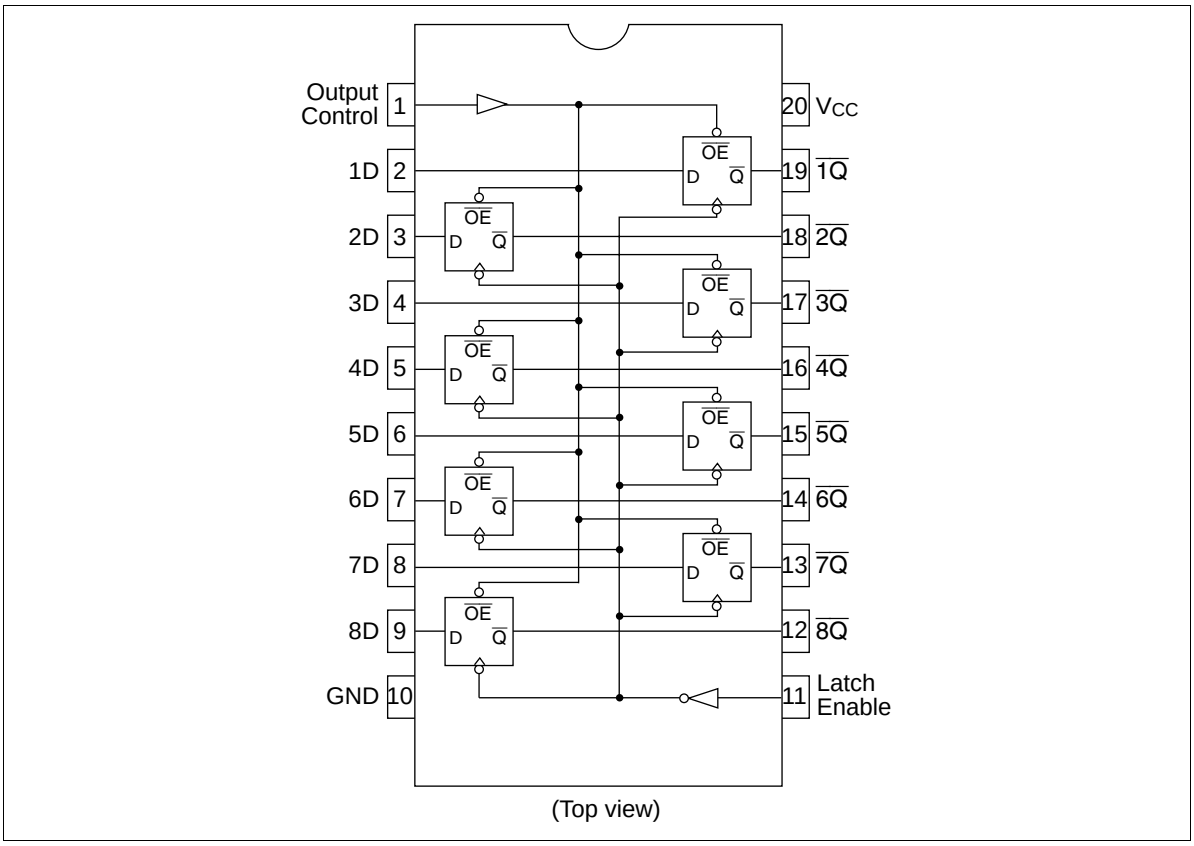
Function Table

			Outputs	
Output Control	**Latch Enable**	**Data**	**HD74HCT563**	**HD74HCT573**
L	H	H	L	H
L	H	L	H	L
L	L	X	$\overline{Q}_0$	Q_0
H	X	X	Z	Z

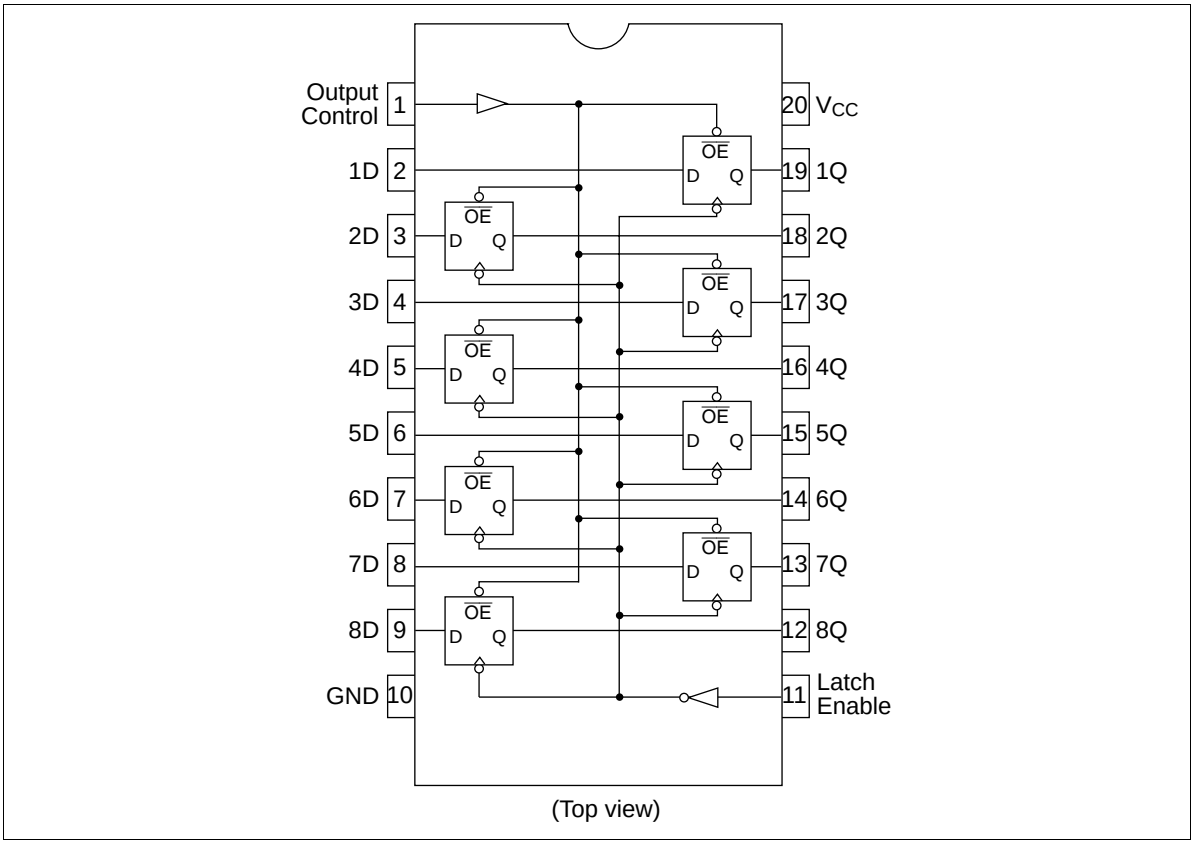
Hitachi semiconductor

Pin Arrangement

HD74HCT563

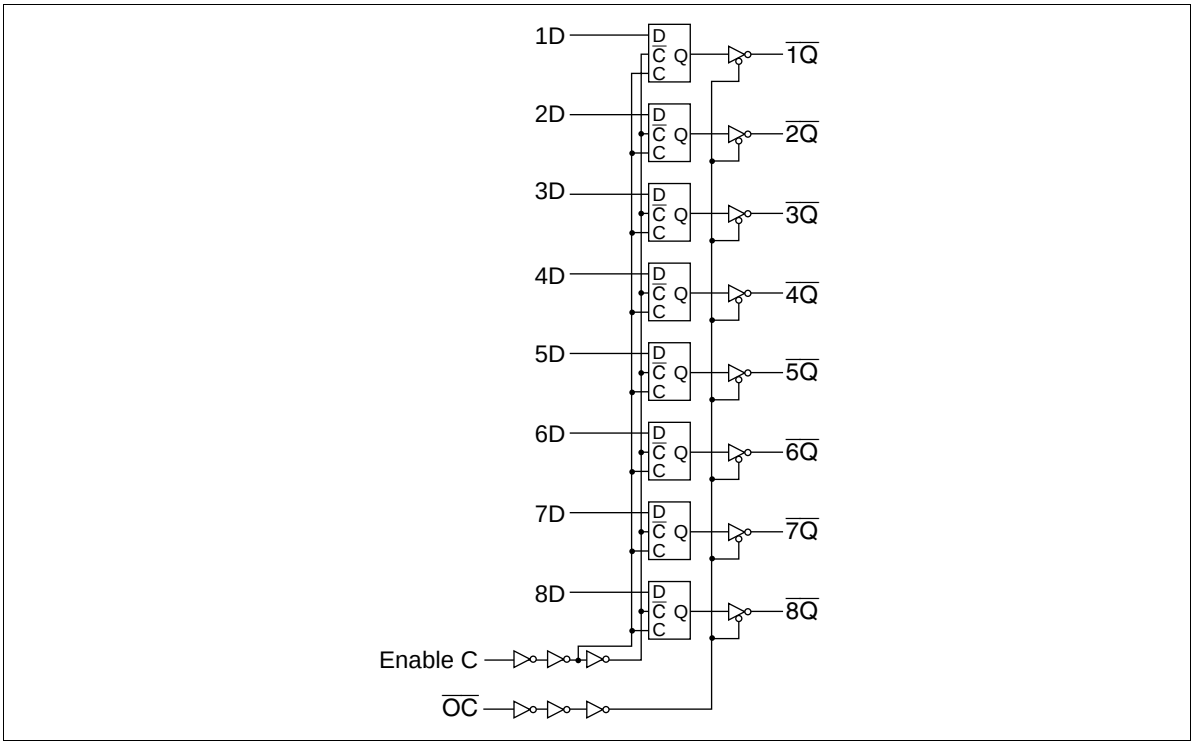


HD74HCT573

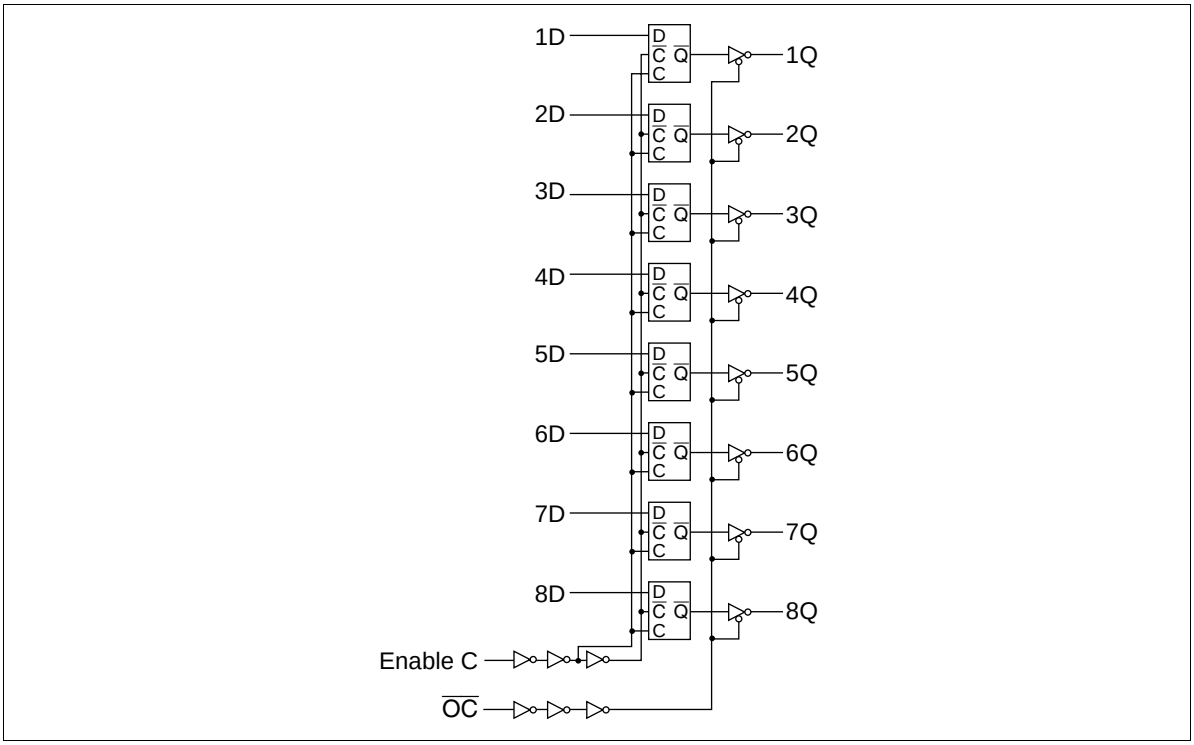

Output Control
1
1D
2
2D
3
3D
4
4D
5
5D
6
6D
7
7D
8
8D
9
GND
10
20
V_{CC}
19
1Q
18
2Q
17
3Q
16
4Q
15
5Q
14
6Q
13
7Q
12
8Q
11
Latch Enable
OE
D
Q
(Top view)

Block Diagram

HD74HCT563



HD74HCT573



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V
DC current drain per pin	I_{OUT}	±35	mA
DC current drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

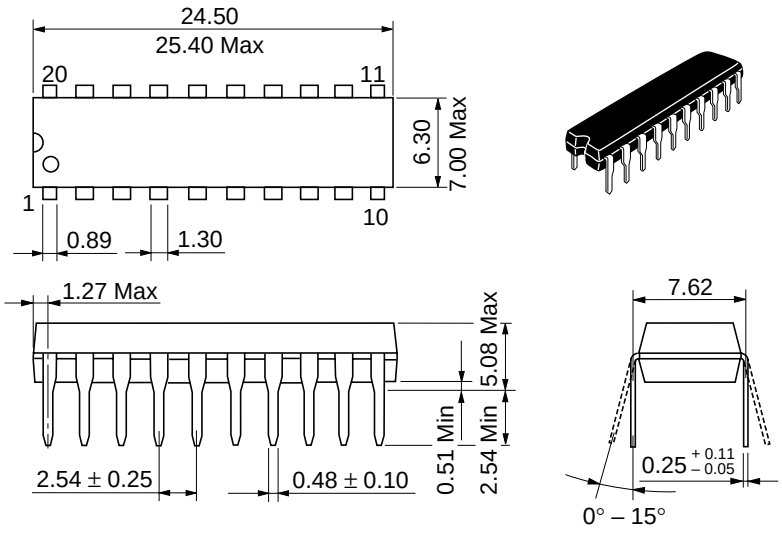
DC Characteristics

Item	Symbol	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max		V_{cc} (V)	
Input voltage	V_{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5	
	V_{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5	
Output voltage	V_{OH}	4.4	—	—	4.4	—	V	4.5	Vin = V_{IH} or V_{IL}, I_{OH} = –20 µA
		4.18	—	—	4.13	—		4.5	I_{OH} = –6 mA
	V_{OL}	—	—	0.1	—	0.1	V	4.5	Vin = V_{IH} or V_{IL}, I_{OL} = 20 µA
		—	—	0.26	—	0.33		4.5	I_{OL} = 6 mA
Off-state output current	I_{OZ}	—	—	±0.5	—	±5.0	µA	5.5	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND
Input current	Iin	—	—	±0.1	—	±1.0	µA	5.5	Vin = V_{CC} or GND
Quiescent current	I_{CC}	—	—	4.0	—	40	µA	5.5	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

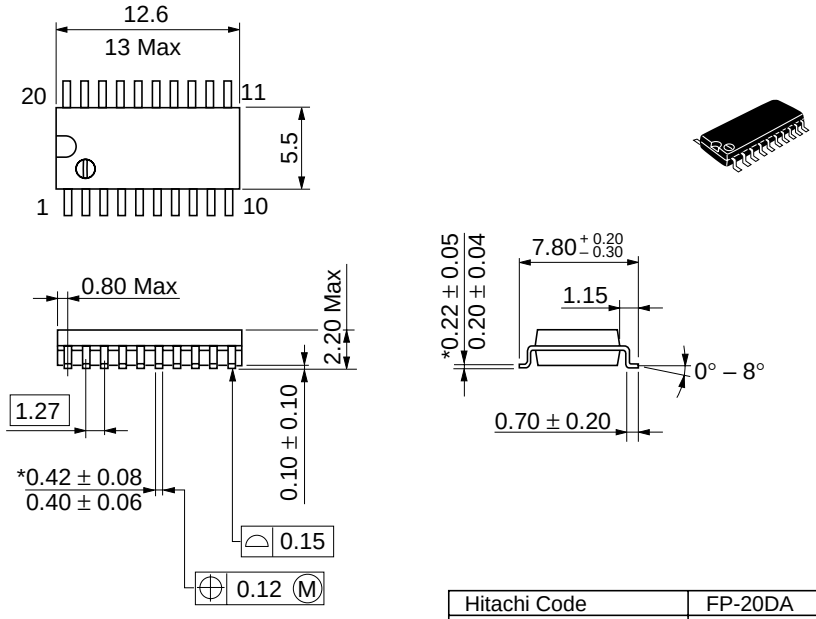
Item	Symbol	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max		V_{cc} (V)	
Propagation delay time	t_{PLH}	—	13	22	—	28	ns	4.5	Data to Q, $\overline{Q}$
	t_{PHL}	—	13	22	—	28		4.5	
	t_{PLH}	—	14	23	—	29	ns	4.5	Enable G to Q, $\overline{Q}$
	t_{PHL}	—	14	23	—	29		4.5	
Output enable time	t_{ZL}	—	14	30	—	38	ns	4.5	
	t_{ZH}	—	15	30	—	38		4.5	
Output disable time	t_{LZ}	—	16	30	—	38	ns	4.5	
	t_{HZ}	—	17	30	—	38		4.5	
Setup time	t_{su}	12	3	—	15	—	ns	4.5	
Hold time	t_h	5	–1	—	5	—	ns	4.5	
Pulse width	t_w	16	4	—	20	—	ns	4.5	
Output rise/fall time	t_{TLH}	—	4	12	—	15	ns	4.5	
	t_{THL}	—	4	12	—	15		4.5	
Input capacitance	Cin	—	5	10	—	10	pF	—	

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

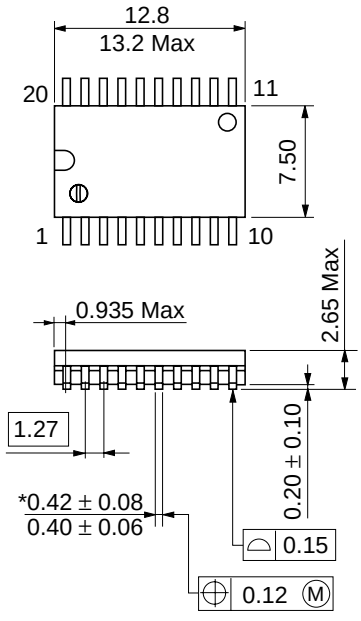
Unit: mm

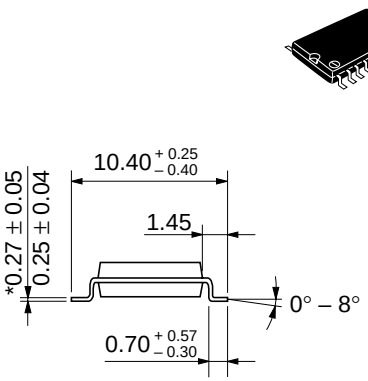


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

Unit: mm

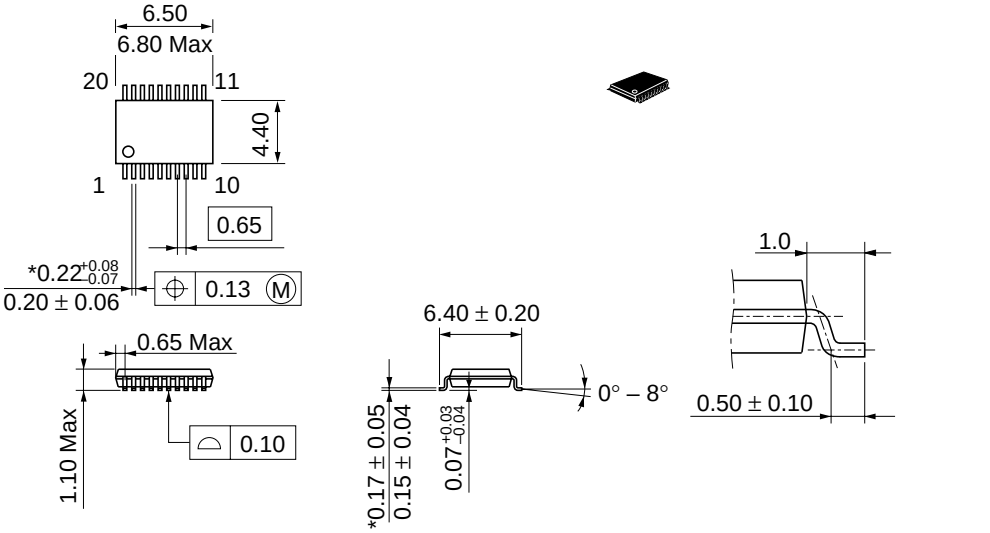




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

Unit: mm



Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

*Dimension including the plating thickness
Base material dimension

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX