

POB4UV6414C-(75/102)T-S

32MByte (4M x 64) CMOS, PC/100

Synchronous DRAM Module

General Description

The POB4UV6414C-(75/102)T-S is a high performance, 32-megabyte synchronous, dynamic RAM module organized as 4M words by 64 bits, in a 144-pin, small outline dual-in-line memory module (SODIMM) package.

The module utilizes four Fujitsu MB81F641642D-(75/102)FN CMOS 4Mx16 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

Features

- High Density 32MByte
- Cycle Time (CL=3) : 7.5ns (-75), 10ns (-102)
- Cycle Time (CL=2) : 11.5ns (-75), 10ns (-102)
- Low Power: Active 3.0W (-75), 2.6W (-102)
- LVTTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.000 inch

ABSOLUTE MAXIMUM RATINGS

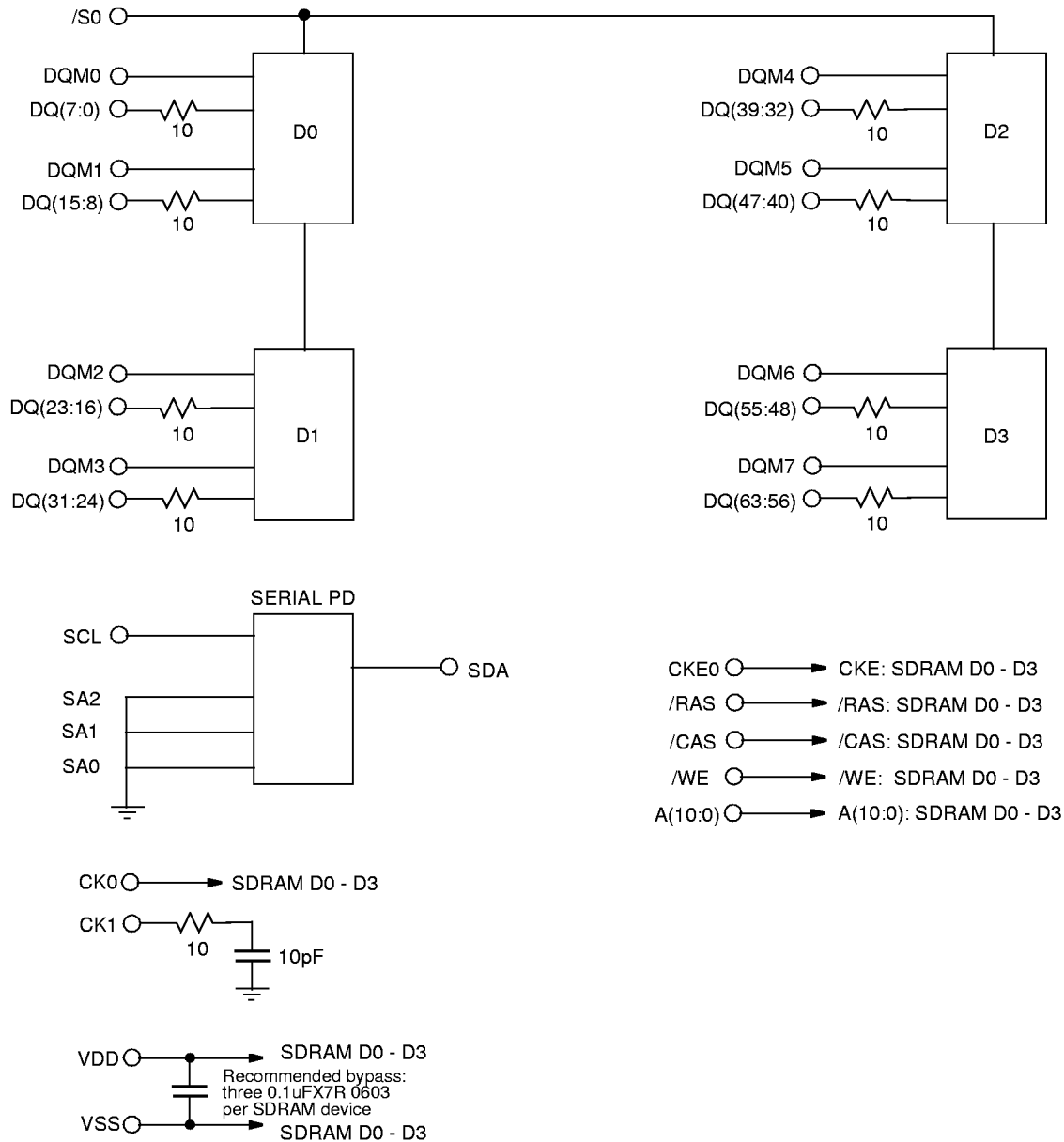
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{SS}	V _T	-0.5 to +4.6	V
Power Dissipation	P _T	4.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Short Circuit Output Current	I _{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High voltage	2.0	-	V _{CC} +0.5	V
V _{IL}	Input Low voltage	-0.5	-	0.8	V

Funktional Diagram



Note: To obtain most advantageous board layout, byte lanes may be swapped. Bits within a byte may also be swapped, however, bits between bytes may not be swapped

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Pin Name

A0~A11	Row Addresses	DQMB0-DQMB7	DQ Mask Enables
A0~A7	Column Addresses	CS0*	Chip Select
BA0, BA1	Bank Select Address	WE*	Write Enable
DQ0~DQ63	Data Inputs/Outputs	SCL	Serial Clock
CLK0, CLK1	Clock Inputs	SDA	Serial Data Input/Output
RAS*	Row Address Strokes	V _{CC}	Power Supply
CAS*	Column Address Strokes	V _{SS}	Ground
CKE0	Clock Enables	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V _{SS}	2	V _{SS}	73	NC	74	CLK1
3	DQ0	4	DQ32	75	V _{SS}	76	V _{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V _{CC}	82	V _{CC}
11	V _{CC}	12	V _{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V _{SS}	92	V _{SS}
21	V _{SS}	22	V _{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V _{CC}	28	V _{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V _{CC}	102	V _{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0 (Note)
35	V _{SS}	36	V _{SS}	107	V _{SS}	108	V _{SS}
37	DQ8	38	DQ40	109	A9	110	BA1 (Note)
39	DQ9	40	DQ41	111	A10/AP (Note)	112	A11
41	DQ10	42	DQ42	113	V _{CC}	114	V _{CC}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V _{CC}	46	V _{CC}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V _{SS}	120	V _{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V _{SS}	56	V _{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V _{CC}	130	V _{CC}
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	V _{CC}	64	V _{CC}	135	DQ30	136	DQ62
65	RAS*	66	CAS*	137	DQ31	138	DQ63
67	WE*	68	NC	139	V _{SS}	140	V _{SS}
69	CS0*	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	V _{CC}	144	V _{CC}

Notes : 1. Address A10 : Initiates Auto-Precharge
2. Address BA0,BA1 : Bank select within the SDRAM devices.

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SERIAL PD INFORMATION

Byte#	Function Described	Function Supported		Hex Value	
		-75	-102	-75	-102
0	# Bytes Written into serial memory at module mfr	128 bytes		80h	
1	Total # bytes of SPD memory device	256 bytes		08h	
2	Fundamental memory type	SDRAM		04h	
3	# Row Address on this assembly	12		0Ch	
4	# Column Addresses on this assembly	8		08h	
5	# Module Banks on this assembly	1		01h	
6	Data Width of this assembly	64 bits		40h	
7	Data Width of this assembly (continued)			00h	
8	Voltage interface standard of this assembly	LVTTTL		01h	
9	SDRAM cycle time at CL=3 (tCLK)	7.5ns	10ns	75h	A0h
10	SDRAM Access from Clock at CL=3 (tAC)	6ns		60h	
11	DIMM configuration type	Non-Parity		00h	
12	Refresh Rate/Type	S/R, Normal 15.6 ms		80h	
13	SDRAM Width Primary DRAM	x16		10h	
14	ECC SDRAM Data Width	N/A		00h	
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK		01h	
16	Burst Length Supported	1, 2, 4, 8 & Full		8Fh	
17	# Banks on each SDRAM device	4		04h	
18	CAS# Latency	2, 3		06h	
19	CS# Latency	0		01h	
20	Write Latency	0		01h	
21	SDRAM Module Attribute	Non-Buffered/Registered		00h	
22	SDRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P		0Eh	
23	Min Clock cycle Time at CL=2 (tCLK)	11.5ns	10ns	B5h	A0h
24	Max. Data Access Time from clock at CL=2 (tAC)	7.0ns	6.0ns	70h	60h
25	Min Clock cycle Time at CL=1 (tCLK)	N/A		00h	
26	Max. Data Access Time from clock at CL=1 (tAC)	N/A		00h	
27	Min. Row Precharge Time (tRP)	22.5ns	20ns	17h	14h
28	Min. Row Active Delay (tRRD)	15ns	20ns	0Fh	14h
29	Min. RAS to CAS Delay (tRCD)	22.5ns	20ns	17h	14h
30	Min. RAS Pulse Width (tRAS)	45ns	50ns	2Dh	32h
31	Module Bank Density	32MB		08h	
32	Address and Command Input Setup Time (tSI)	2ns		20h	
33	Address and Command Input Hold Time (tHI)	1ns		10h	
34	Data Input Setup Time (tSI)	2ns		20h	
35	Data Input Hold Time (tHI)	1ns		10h	
36-61	Superset Information			00h	
62	SPD Revision	Rev. 1.2		12h	
63	Checksum for bytes 0-62	JEDEC Calculation		JEDEC Calculation	

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SERIAL PD INFORMATION (CONTINUED)

Byte#	Function Described	Function Supported		Hex Value	
		-75	-102	-75	-102
64	Manufacturers JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Manufacturers JEDEC ID code per JEP-106E	SMART's ID		94h	
66-71	Manufacturers JEDEC ID code per JEP-106E	None		FFh	
72	Manufacturing location	Mfr Specific Data			
73	Manufacturer's Part Number	P		50h	
74	Manufacturer's Part Number	O		4Fh	
75	Manufacturer's Part Number	B		42h	
76	Manufacturer's Part Number	4		34h	
77	Manufacturer's Part Number	U		55h	
78	Manufacturer's Part Number	V		56h	
79	Manufacturer's Part Number	6		36h	
80	Manufacturer's Part Number	4		34h	
81	Manufacturer's Part Number	1		31h	
82	Manufacturer's Part Number	4		34h	
83	Manufacturer's Part Number	C		43h	
84	Manufacturer's Part Number	7	1	37h	31h
85	Manufacturer's Part Number	5	0	35h	30h
86	Manufacturer's Part Number	T	2	54h	32h
87	Manufacturer's Part Number	S	T	53h	54h
88	Manufacturer's Part Number	None	S	FFh	53h
89	Manufacturer's Part Number	None		FFh	
90	Manufacturer's Part Number	None		FFh	
91	Revision Code	Mfr Specific Data		Mfr Specific Data	
92	Revision Code	None		FFh	
93	Manufacturing Date				
94	Manufacturing Date	DATE		DATE	
95-98	Assembly Serial Number	Serial Number		S.No.	
99	Manufacturer Specific Data	S		53h	
100	Manufacturer Specific Data	M		4Dh	
101	Manufacturer Specific Data	A		41h	
102	Manufacturer Specific Data	R		52h	
103	Manufacturer Specific Data	T		54h	
104	Manufacturer Specific Data	M		4Dh	
105	Manufacturer Specific Data	o		6Fh	
106	Manufacturer Specific Data	d		64h	
107	Manufacturer Specific Data	u		75h	
108	Manufacturer Specific Data	l		6Ch	
109	Manufacturer Specific Data	a		61h	
110	Manufacturer Specific Data	r		72h	
111	Manufacturer Specific	T		54h	
112	Manufacturer Specific Data	e		65h	
113	Manufacturer Specific Data	c		63h	
114	Manufacturer Specific Data	h		68h	
115	Manufacturer Specific Data	n		6Eh	
116	Manufacturer Specific Data	o		6Fh	
117	Manufacturer Specific Data	l		6Ch	
118	Manufacturer Specific Data	o		6Eh	
119	Manufacturer Specific Data	g		67h	
120	Manufacturer Specific Data	i		69h	
121	Manufacturer Specific Data	e		65h	
122	Manufacturer Specific Data	s		73h	
123	Manufacturer Specific Data	None		FFh	
124	Manufacturer Specific Data	None		FFh	
125	Manufacturer Specific Data	None		FFh	
126	Intel Spec. Frequency	100Mhz		64h	
127	Intel Spec. Detail for 100Mhz	1000-1101	1000-1111	8Dh	8Fh
128-255	Open for CPQ Use for Read & Write	None		FFh	

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 1,2

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Output High Voltage		$V_{OH(DC)}$	$I_{OH} = -2mA$	2.4	-	V
Output Low Voltage		$V_{OL(DC)}$	$I_{OL} = 2mA$	-	0.4	V
Input Leakage Current (Any Input)		I_{LI}	$0V \leq V_{IN} \leq V_{CC}$; All other pins not under test = 0V	-40	40	μA
Output Leakage Current		I_{LO}	$0V \leq V_{IN} \leq V_{CC}$ $D_{out} = \text{Disable}$	-10	10	μA
Operating Current (Average Power Supply Current)	-75	I_{CC1S}	Burst: Length=4, $t_{RC} = \text{min}$ for BL=4, $t_{CK} = \text{min}$. One bank- active, Outputs open, Addresses changed up to 3-times during t_{RC} (min), $0V \leq V_{in} \leq V_{CC}$	-	480	mA
	-102			-	440	
	-75	I_{CC1D}	Burst: Length=4 (each bank), $t_{RC} = \text{min}$ for BL=4 (each bank), $t_{CK} = \text{min}$. 2 banks active, Output open, Addresses changed up to 3-times during t_{RC} (min), $0V \leq V_{in} \leq V_{CC}$	-	840	mA
	-102			-	720	
Precharge Standby Current (Power Supply Current)		I_{CC2P}	CKE= V_{IL} , All banks idle, $t_{CK} = \text{min}$, Power down mode, $0V \leq V_{in} \leq V_{CC}$	-	4	mA
		I_{CC2PS}	CKE= V_{IL} , All banks idle, CLK=H or L, Power down mode, $0V \leq V_{in} \leq V_{CC}$	-	4	
Precharge Standby Current (Power Supply Current)	-75	I_{CC2N}	CKE= V_{IH} , All banks idle, $t_{CK} = \text{min}$, NOP commands only, Input signals (except to CMD) are changed one time during 3 clock cycles, $0V \leq V_{in} \leq V_{CC}$	-	100	mA
	-102			-	80	
Precharge Standby Current (Power Supply Current)		I_{CC2NS}	CKE= V_{IH} , All banks idle, CLK=H or L, Input signals are stable, $0V \leq V_{in} \leq V_{CC}$	-	20	

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(Continued)

Parameter		Symbol	Test Condition	Value		Unit
				Min.	Max.	
Active Standby Current (Power Supply Current)		I_{CC3P}	CKE= V_{IL} , Any bank active, $t_{CK}=\text{min}$, $0V \leq V_{in} \leq V_{CC}$	-	8	mA
		I_{CC3PS}	CKE= V_{IL} , Any bank active, CLK = H or L, $0V \leq V_{in} \leq V_{CC}$	-	8	mA
	-75	I_{CC3N}	CKE= V_{IH} , Any bank active, $t_{CK}=\text{min}$, NOP commands only, Input signals (except to CMD) are changed one time during 3 clock cycles, $0V \leq V_{in} \leq V_{CC}$	-	120	mA
	-102			-	100	
		I_{CC3NS}	CKE= V_{IH} , Any bank active, CLK = H or L, $0V \leq V_{in} \leq V_{CC}$	-	40	mA
Burst mode Current (Average Power supply current)	-75	I_{CC4}	$t_{CK}=\text{min}$, Burst length=4, Outputs open, Multiple-banks active, Gapless data, $0V \leq V_{in} \leq V_{CC}$	-	680	mA
	-102			-	560	
Refresh Current #1 (Average Power Supply Current)	-75	I_{CC5}	Auto-refresh; $t_{CK}=\text{min}$, $t_{RC}=\text{min}$, $0V \leq V_{in} \leq V_{CC}$	-	680	mA
	-102			-	640	
Refresh Current #2 (Average Power Supply Current)		I_{CC6}	Self-refresh; $t_{CK}=\text{min}$, CKE $\leq 0.2V$, $0V \leq V_{in} \leq V_{CC}$	-	4	mA

†CL = CAS* Latency

- Notes:
- I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate;
The specified values are obtained with the output open and no termination register.
 - An initial pause (DESL or NOP) of 200 μs is required after power-up followed by a minimum of eight Auto-refresh cycles.

CAPACITANCE

(TA = +25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, CE*, RAS*, CAS*, CS0*)	C _{I1}	25	pF	1
Input Capacitance (DQMBs)	C _{I2}	10	pF	1
Input Capacitance (CLK0)	C _{I3}	21	pF	1
Input Capacitance (CLK1)	C _{I4}	15	pF	1
Input/Output Capacitance (DQ0~DQ63)	C _{I/O}	12	pF	1, 2

- Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTIC: MB81F641642D-(75/102)

(At recommended operating conditions unless otherwise noted) Notes 2,3,4

Parameter		Symbol	Unit	-75		-102		Notes
				Min.	Max.	Min.	Max.	
Clock Period	CAS Latency=2	t _{CK2}	ns	11.5	-	10	-	
	CAS Latency=3	t _{CK3}		7.5	-	10	-	
Clock High Time		t _{CH}	ns	2.5	-	3	-	
Clock Low Time		t _{CL}	ns	2.5	-	3	-	
Input Setup Time		t _{SI}	ns	2	-	2	-	
Input Hold Time		t _{HI}	ns	1	-	1	-	
Access time from Clock (t _{CK=} min)	CAS Latency=2	t _{AC2}	ns	-	7	-	6	5,6
	CAS Latency=3	t _{AC3}			6		6	
Output In Low-Z		t _{LZ}	ns	0	-	0	-	
Output in High-Z	CAS Latency=2	t _{HZ2}	ns	3	7	3	6	7
	CAS Latency=3	t _{HZ3}			6		6	
Output Hold Time	CAS Latency=2	t _{OH}	ns	3	-	3	-	
	CAS Latency=3							
Time between Auto-Refresh command Interval		t _{REFI}	us	-	15.6	-	15.6	
Time between Refresh		t _{REF}	ms	-	64	-	64	
Transition Time		t _T	ns	0.5	2	0.5	2	
CKE Set Up time for Power Down Exit		t _{CKSP}	ns	2.5	-	3	-	

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BASE VALUES FOR CLOCK COUNT/LATENCY: MB81F641642D-(75/102)

Parameter	Symbol	Unit	-75		-102		Notes
			Min.	Max.	Min.	Max.	
RAS Cycle Time	t_{RC}	ns	67.5	-	70	-	8
RAS Precharge Time	t_{RP}	ns	22.5	-	20	-	
RAS Active Time	t_{RAS}	ns	45	110000	50	110000	
RAS to CAS Delay Time	t_{RCD}	ns	22.5	-	20	-	9
Write Recovery Time	t_{WR}	ns	7.5	-	10	-	
Data-in to Precharge Lead Time	t_{DPL}	ns	7.5	-	10	-	
Data-in to Active/ Refresh command period	CAS Latency=2 t_{DAL2}	ns	1 cyc + t_{RP}	-	1 cyc + t_{RP}	-	
	CAS Latency=3 t_{DAL3}		2 cyc + t_{RP}	-	2 cyc + t_{RP}	-	
Mode Register set cycle Time	t_{RSC}	ns	15	-	20	-	
RAS to RAS Bank Active Delay Time	t_{RRD}	ns	15	-	20	-	

CLOCK COUNT FORMULA

(Note 10)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad (\text{Round off a whole number})$$

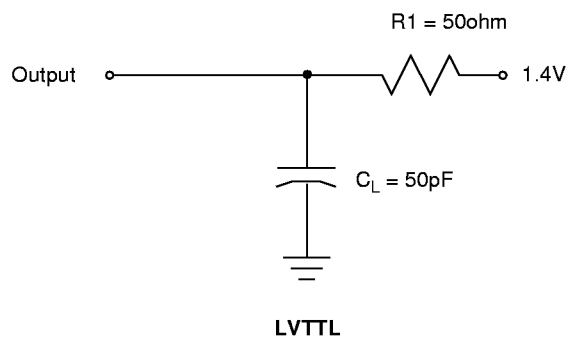
LATENCY-FIXED VALUES: MB81F641642D-(75/102)

(The latency values on these parameters are fixed regardless of clock period)

Parameter	Symbol	Unit	-75	-102	Notes
CKE to Clock Disable	I_{CKE}	cycle	1	1	
DQM to Output in High-Z	I_{DQZ}	cycle	2	2	
DQM to Input Data Delay	I_{DQD}	cycle	0	0	
Last Output to Write Command Delay	I_{OWD}	cycle	2	2	
Write Command to Input Data Delay	I_{DWD}	cycle	0	0	
Precharge to Output in High-Z Delay	CL = 2 I_{ROH2}	cycle	2	2	
	CL = 3 I_{ROH3}		3	3	
Burst Stop Command to Output in High-Z Delay	CL = 2 I_{BSH2}	cycle	2	2	
	CL = 3 I_{BSH3}		3	3	
CAS to CAS Delay (min)	I_{CCD}	cycle	1	1	
CAS Bank Delay (min)	I_{CBD}	cycle	1	1	

- Notes:
- I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
 - An initial pause (DESL or NOP) of 200 μ s is required after power-up followed by a minimum of eight Auto-refresh cycles.
 - AC characteristics assume $t_T = 1$ ns and 50 pF of capacitive load.
 - 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
 - Assumes t_{RCD} is satisfied.
 - t_{AC} also specifies the access time at burst mode.
 - Specified where output buffer is no longer driven.
 - Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}).
 - Operation within the t_{RCD} (min) ensures that access time is determined by t_{RCD} (min) + t_{AC} (max); If t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{AC} .
 - All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off a whole number).

Fig. 4 - EXAMPLE OF AC TEST LOAD CIRCUIT



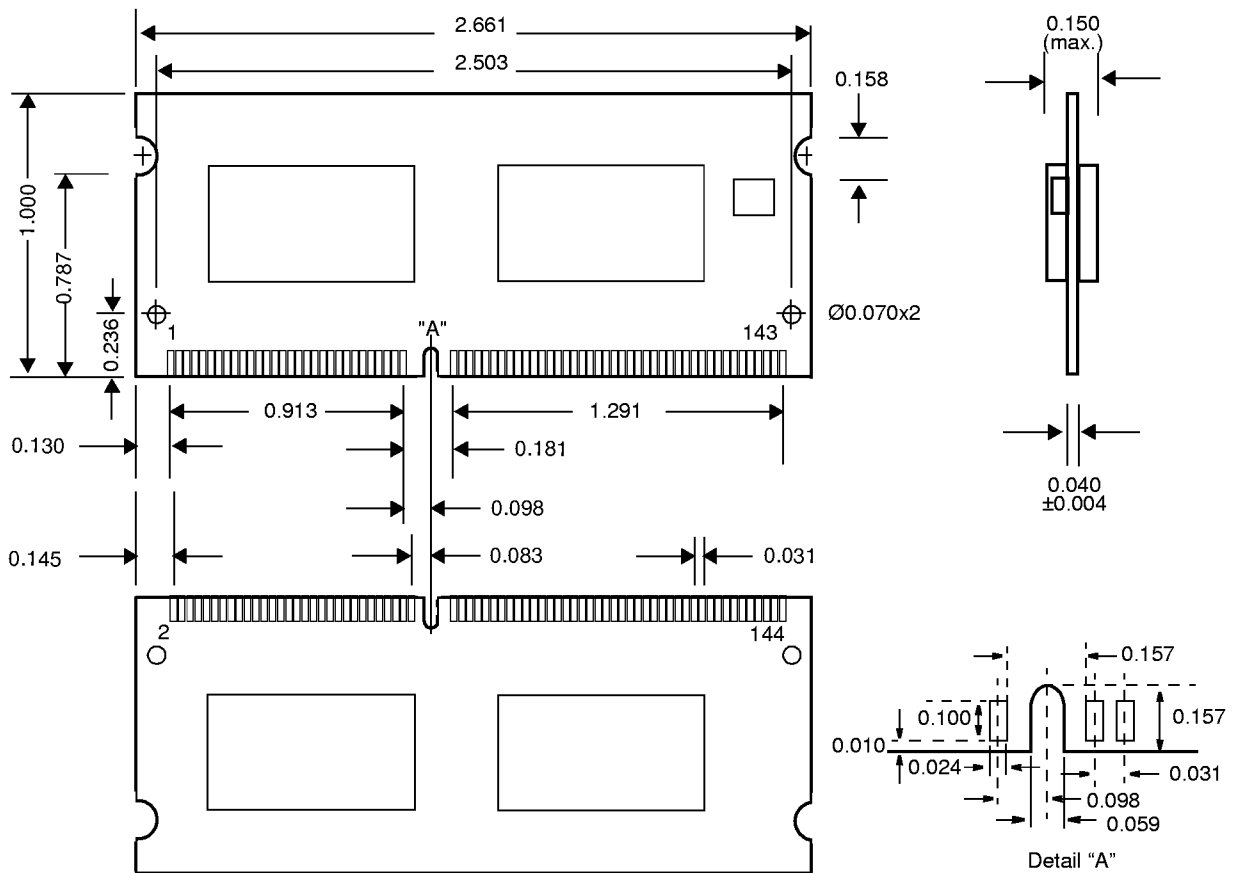
Note: AC characteristics are measured in this condition. This load circuits are not applicable for V_{OH} and V_{OL} .

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Physical Dimensions

144-pin (72x2) DIMM

Front View



Back View

(All dimensions are in inches with 0.005" tolerance unless otherwise specified.)

Ordering Information

P O B 4 U V 64 1 4 C - 102 T - S

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13)

(1) **Memory Type**

S : SDRAM (PC/66)
G : SGRAM
P : SDRAM-Fast (PC/100)

(2) **Module Shape**

S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**

A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**

1 : 1M
2 : 2M
4 : 4M
8 : 8M
16 : 16M
256 : 256K
512 : 512K

(5) **Buffer Type**

B : Buffered
U : Unbuffered
R : Registered

(6) **Operating Voltage & Power Consumption**

V : 3.3V & LVTTTL & Standard Power
L : 3.3V & LVTTTL & Low Power
S : 3.3V & SSTL & Standard Power

(7) **Data Width**

(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**

4 : x4
8 : x8
1 : x16
3 : x32

(9) **Refresh**

2 : 2krf
4 : 4krf
8 : 8krf

(10) **Module Revision / Applied "Standard" *1**

Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**

SDRAM (PC/66)
100 : 100Mhz

SDRAM-Fast (100Mhz, PC/100)

75 : 133MHz (CL=3 t_{RCD}=3, t_{RP}=3)
102 : 100MHz (CL=2; t_{RCD}=2, t_{RP}=2)
103 : 100MHz (CL=3; t_{RCD}=2, t_{RP}=2)
10 : 100MHz (CL=3; t_{RCD}=3, t_{RP}=3)

(12) **Package of Component**

T : TSOP

(13) **Assembly & Test Site**

S : Smart Modular Technologies

POB4UV6414C-(75/102)T-S

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