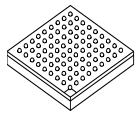
Freescale Semiconductor
Advance Information

MC9328MXS/D
Rev. 0, 1/2005

MC9328MXS



Package Information
Plastic Package
(PBGA–225)

Ordering Information

See Table 2 on page 4

MC9328MXS

1 Introduction

The i.MX (Media Extensions) series provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. The i.MX products specifically address the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The i.MX processor features the advanced and power-efficient ARM920T™ core that operates at speeds up to 100 MHz. Integrated modules, which include a USB device and an LCD controller, support a suite of peripherals to enhance portable products. It is packaged in a 225-contact PBGA package. Figure 1 shows the functional block diagram of the i.MX processor.

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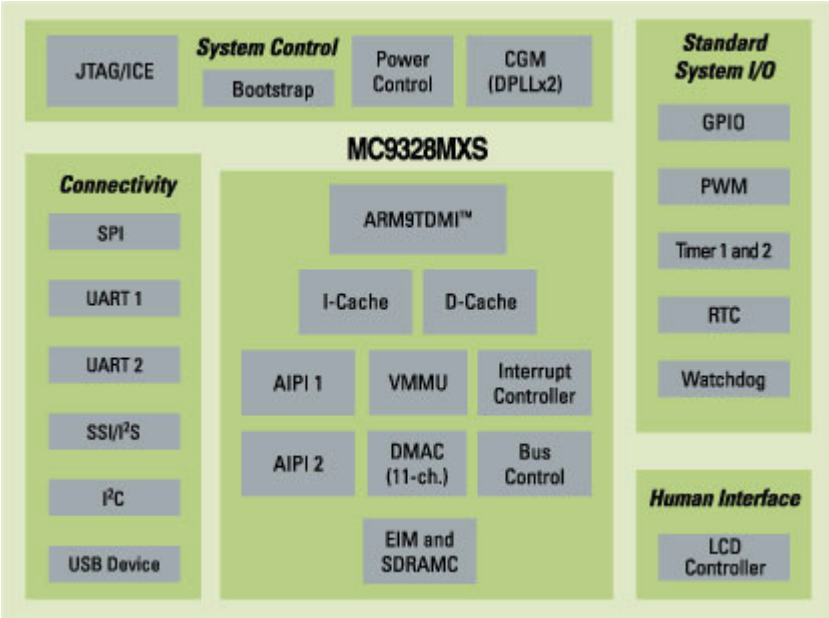


Figure 1. MC9328MXS Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Features

To support a wide variety of applications, the i.MX processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Serial Peripheral Interface (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and Inter-IC Sound (SSI/I^2S) Module
- Inter-IC (I^2C) Bus Module
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 225-contact PBGA Package

1.3 Target Applications

The i.MX processor is targeted for advanced information appliances, smart phones, Web browsers, and messaging applications.

1.4 Revision History

Table 1 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 1. MC9328MXS Data Sheet Revision History for Rev. 0

Revision	
Initial Release	

1.5 Reference Documents

The following documents are required for a complete description of the MC9328MXS and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous DragonBall products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXS Product Brief (order number MC9328MXSP/D)

MC9328MXS Reference Manual (order number MC9328MXSRM/D)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.6 Ordering Information

Table 2 provides ordering information for the 225-contact PBGA package.

Table 2. MC9328MXS Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
225-contact PBGA	100 MHz	-40°C to 85°C	Standard	MC9328MXSCVF10(R2)
			Pb-free	See Note[1]
		0°C to 70°C	Standard	MC9328MXSVF10(R2)
			Pb-free	See Note[1]

1. Contact your distribution center or Freescale sales office.

2 Signals and Connections

Table 3 identifies and describes the i.MX processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 3. MC9328MXS Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
$\overline{OE}$	Memory Output Enable—Active low output enables external data bus.
$\overline{CS}$ [5:0]	Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected.
$\overline{ECB}$	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{LBA}$	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK (burst clock)	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{RW}$	$\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM.
$\overline{DTACK}$	$\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external DTACK signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the i.MX processor upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable
$\overline{CSD0}$	SDRAM Chip-select signal which is multiplexed with the $\overline{CS2}$ signal. These two signals are selectable by programming the system control register.
$\overline{CSD1}$	SDRAM Chip-select signal which is multiplexed with $\overline{CS3}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{CSD1}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
$\overline{RAS}$	SDRAM Row Address Select signal

Table 3. MC9328MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{CAS}}$	SDRAM Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
$\overline{\text{RESET\_SF}}$	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET\_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET\_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET\_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to little endian. If it is driven logic-low at reset, the external chip-select space will be configured to big endian.
$\overline{\text{DMA\_REQ}}$	External DMA request pin.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{\text{ECB}}$, $\overline{\text{LBA}}$, BCLK(burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.

Table 3. MC9328MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SPI 1	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{SS}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{SPI_RDY}$	Serial Data Ready
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
$\overline{USBD\_OE}$	USB $\overline{OE}$
USBD_AFE	USB Analog Front End Enable
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{UART1\_RTS}$	Request to Send
$\overline{UART1\_CTS}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{UART2\_RTS}$	Request to Send
$\overline{UART2\_CTS}$	Clear to Send
$\overline{UART2\_DSR}$	Data Set Ready

Table 3. MC9328MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data
PWM	
PWMO	PWM Output
Test Function	
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
General Purpose Input/Output	
PA[14:3]	Dedicated GPIO
PB[13:8]	Dedicated GPIO
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
AVSS	Quiet ground for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry
Substrate Supply Pins	
SVDD	Supply routed through substrate of package; not to be bonded
SGND	Ground routed through substrate of package; not to be bonded

3 Specifications

This section contains the electrical specifications and timing diagrams for the i.MX processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 9 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NVDD	DC I/O Supply Voltage	-0.3	3.3	V
QVDD	DC Internal (core = 100 MHz) Supply Voltage	-0.3	1.9	V
AVDD	DC Analog Supply Voltage	-0.3	3.3	V
BTRFVDD	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

1. A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.
2. A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 100MHz, and where the whole image is running out of SDRAM. QVDD at 1.9V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MX processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 3 on page 5.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MXSVF10	0	70	°C

Table 5. Recommended Operating Range (Continued)

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MXSCVF10	-40	85	°C
NVDD	I/O supply voltage (if using SPI, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 100 MHz)	1.70	1.90	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the "Power-Up Sequence" section of application note AN2537 on the i.MX application processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MX processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 100 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 100 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 100 MHz, QVDD = 1.9V, temp = 25°C)	–	35	–	µA
$Sidd_4$	Standby current (Core = 100 MHz, QVDD = 1.9V, temp = 55°C)	–	60	–	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
I_{IH}	Input high leakage current ($V_{IN} = V_{DD}$, no pull-up or pull-down)	–	–	±1	μA
I_{OH}	Output high current ($V_{OH} = 0.8V_{DD}$, $V_{DD} = 1.8V$)	–	–	4.0	mA
I_{OL}	Output low current ($V_{OL} = 0.4V$, $V_{DD} = 1.8V$)	-4.0	–	–	mA
I_{OZ}	Output leakage current ($V_{out} = V_{DD}$, output is high impedence)	–	–	±5	μA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 100 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

1. The 16 MHz oscillator is not recommended for use in new designs.

3.6 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

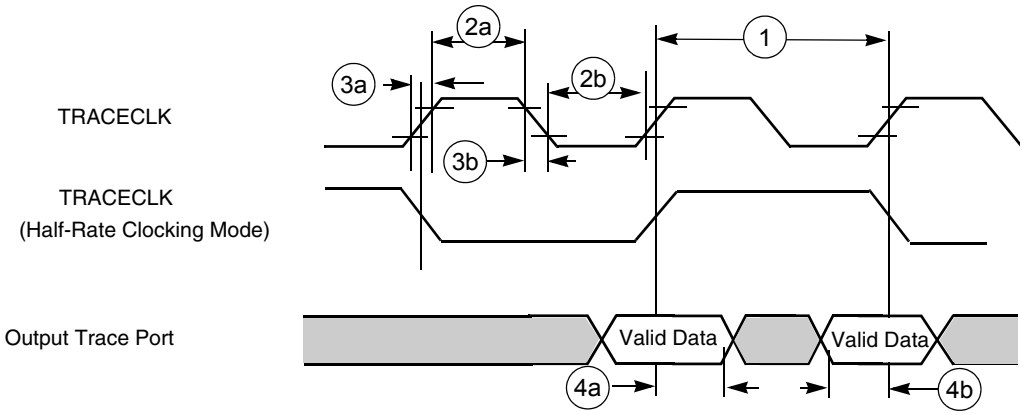


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

3.7 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 10. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock freq range	Vcc = 1.8V	5	–	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	–	30	MHz
Double clock freq range	Vcc = 1.8V	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Pre-multiplier lock-in time	–	–	–	312.5	μsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 μs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 μs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 μs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 μs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.8V	–	1.0 (10%)	1.5	ns
Power supply voltage	–	1.7	–	2.5	V
Power dissipation	FOL mode, integer MF, f_{dck} = 100 MHz, Vcc = 1.8V	–	–	4	mW

3.8 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

NOTE:

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

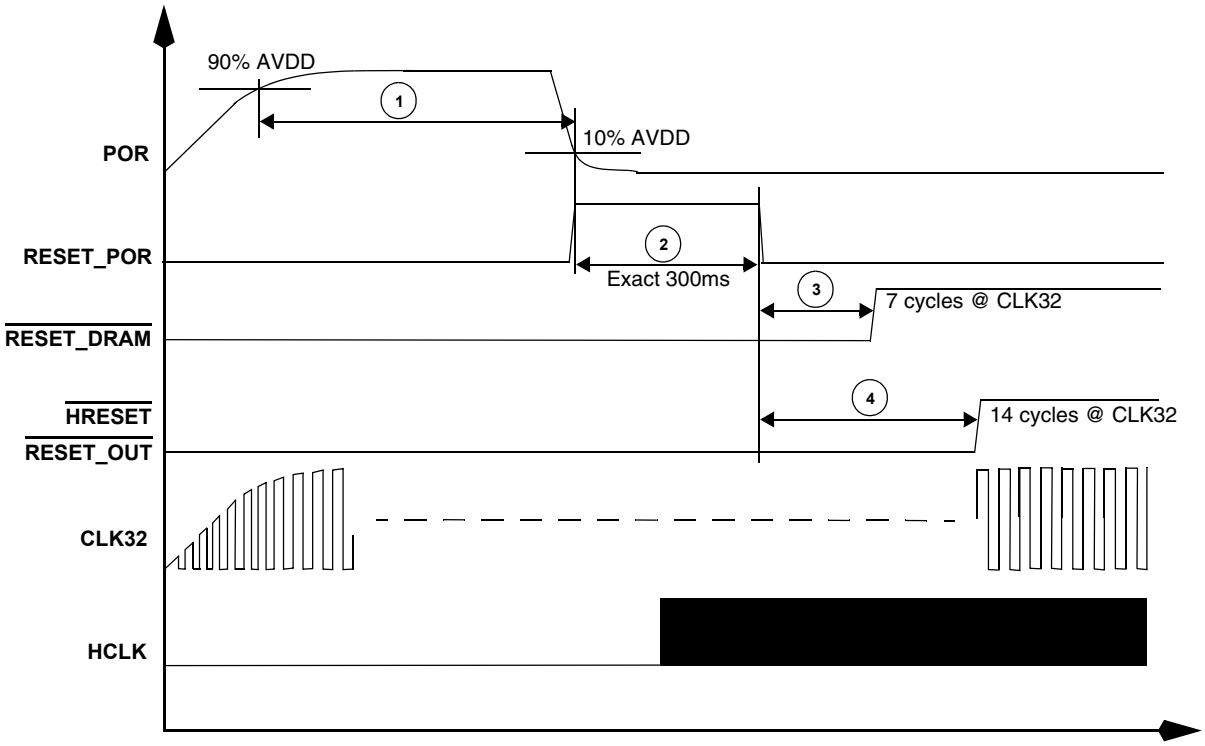


Figure 3. Timing Relationship with POR

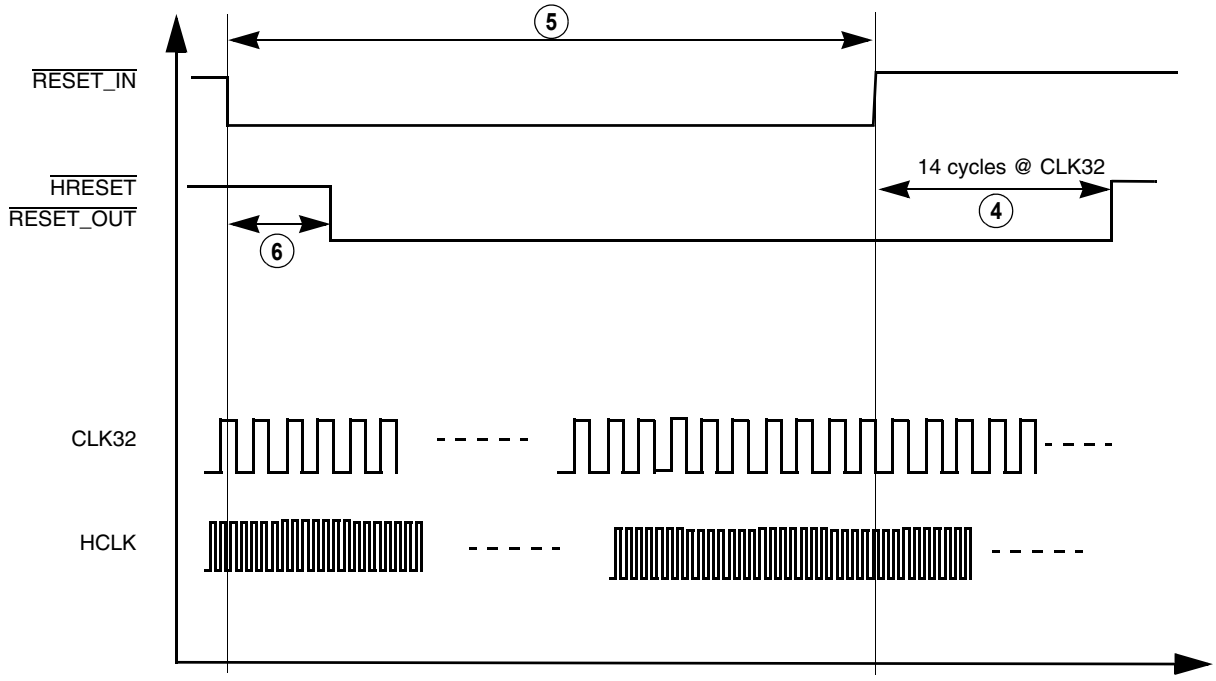


Figure 4. Timing Relationship with $\overline{\text{RESET\_IN}}$

Table 11. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	note[1]	–	note[1]	–	–
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

1. POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal. If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

3.9 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MX processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 on page 16 defines the parameters of signals.

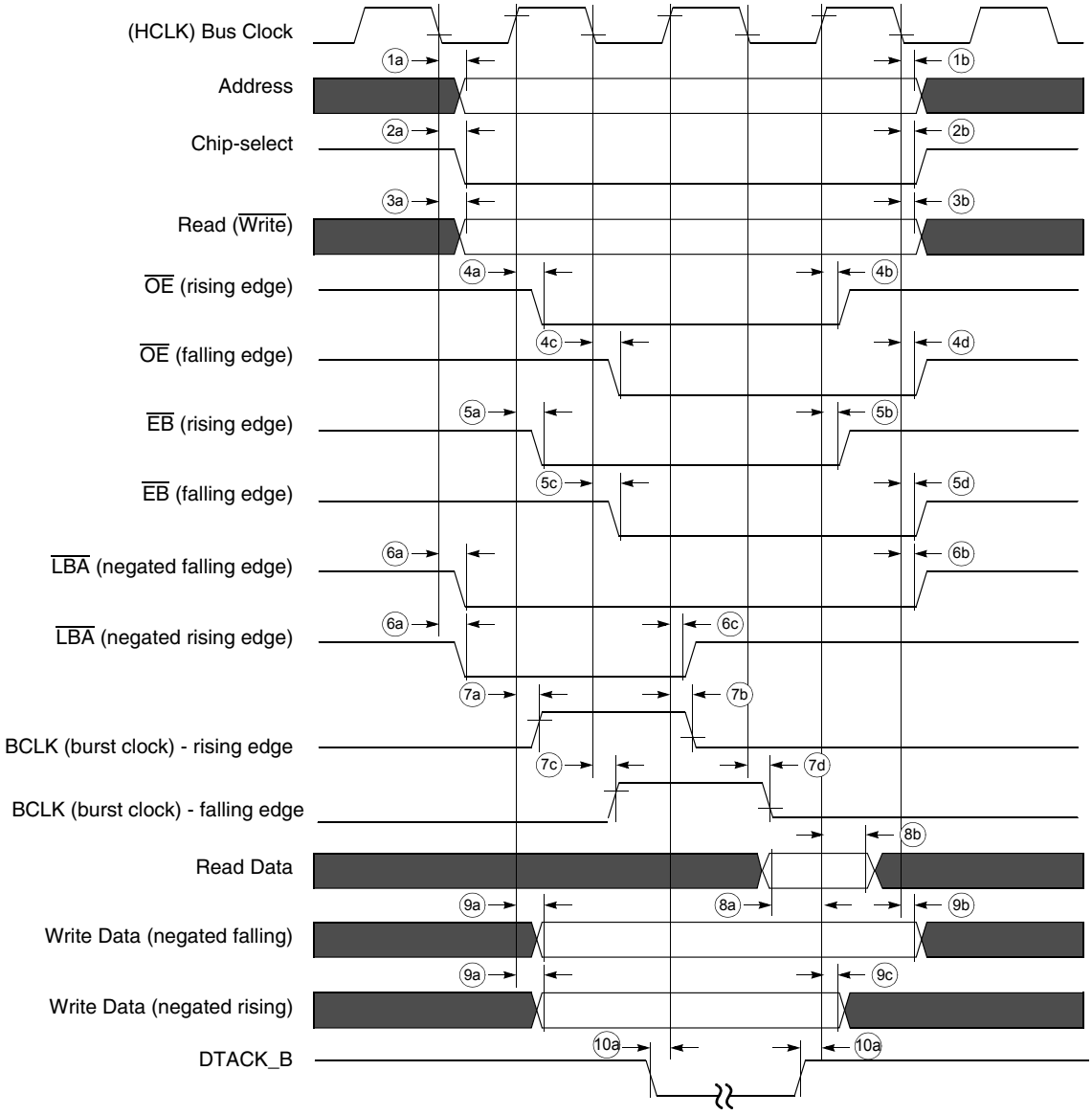


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns
4a	Clock[1] rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock[1] rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock[1] fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock[1] fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock[1] rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock[1] rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock[1] fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock[1] fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock[1] rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock[1] rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock[1]rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock[1] fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock[1] fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock[1] rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock[1] fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock[1] rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

1. Clock refers to the system clock signal, HCLK, generated from the System DPLL

3.9.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

3.9.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

3.9.2.1 DTACK Read Cycle without DMA

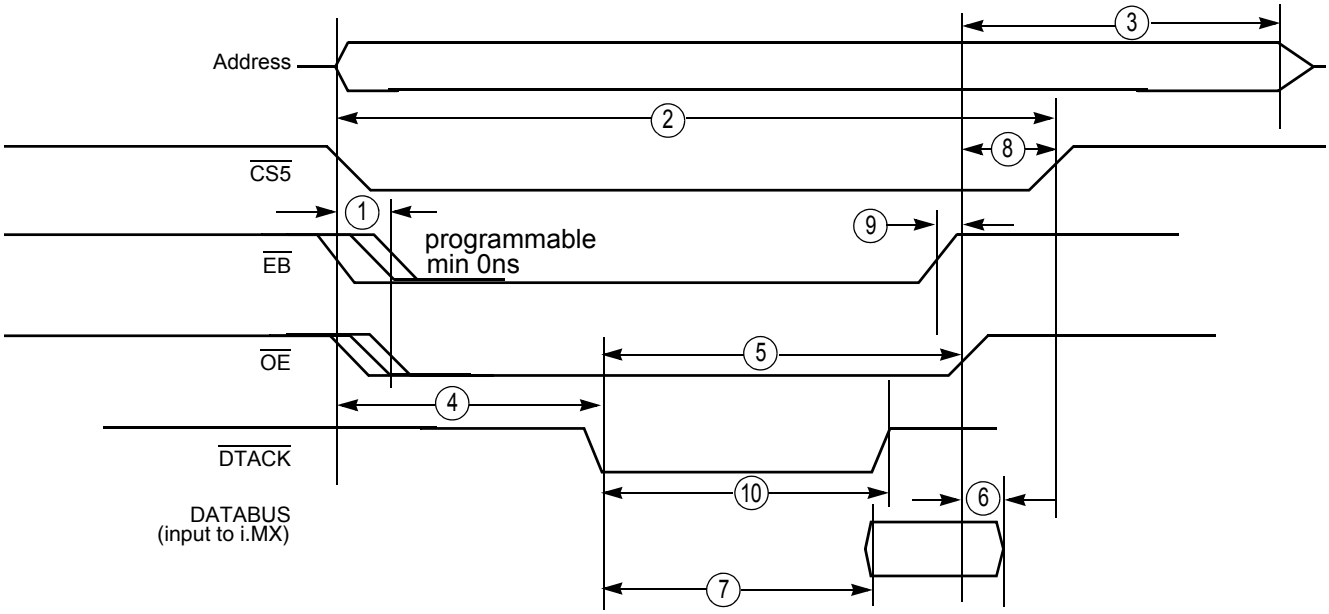


Figure 6. DTACK Read Cycle without DMA

Table 13. Read Cycle without DMA: WSC = 111111, DTACK_SEL=0, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 3	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated to address inactive	46.39	–	ns
4	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	–	1019T	ns
5	$\overline{DTACK}$ asserted to $\overline{OE}$ negated	3T+1.83	4T+6.6	ns
6	Data hold timing after $\overline{OE}$ negated	0	–	ns
7	Data ready after $\overline{DTACK}$ asserted	0	T	ns
8	OE negated to CS negated	0.5T-0.68	0.5T-0.06	ns
9	OE negated after EB negated	0.06	0.18	ns
10	$\overline{DTACK}$ pulse width	1T	3T	ns

Note:
1. $\overline{DTACK}$ asserted means $\overline{DTACK}$ becomes low level.
2. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
3. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
4. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
5. The external $\overline{DTACK}$ input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.2 DTACK Read Cycle DMA Enabled

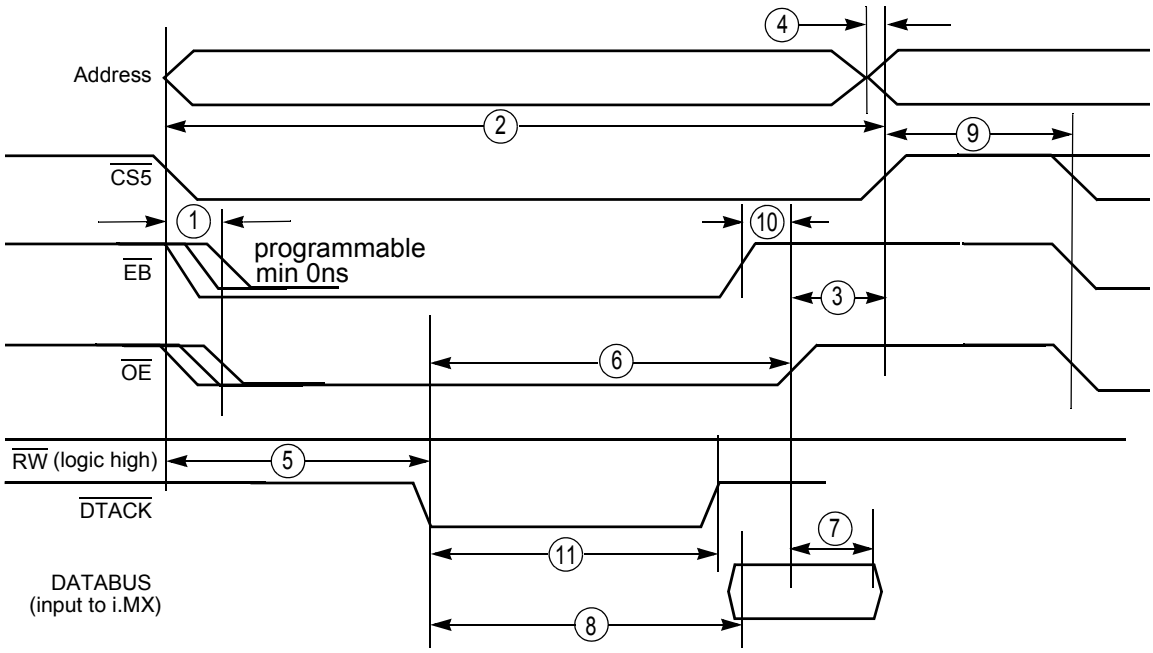


Figure 7. DTACK Read Cycle DMA Enabled

Table 14. Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=0, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 3	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	0.5T-0.68	0.5T-0.06	ns
4	Address inactive before $\overline{CS}$ negated	–	0.3	ns
5	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	–	1019T	ns
6	$\overline{DTACK}$ asserted to $\overline{OE}$ negated	3T+1.83	4T+6.6	ns
7	Data hold timing after $\overline{OE}$ negated	0	–	ns
8	Data ready after DTACK is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
10	OE negate after EB negate	0.06	0.18	ns
11	$\overline{DTACK}$ pulse width	1T	3T	ns

Note:
1. $\overline{DTACK}$ asserted means $\overline{DTACK}$ becomes low level.
2. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
3. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
4. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
5. The external $\overline{DTACK}$ input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.3 DTACK Write Cycle without DMA

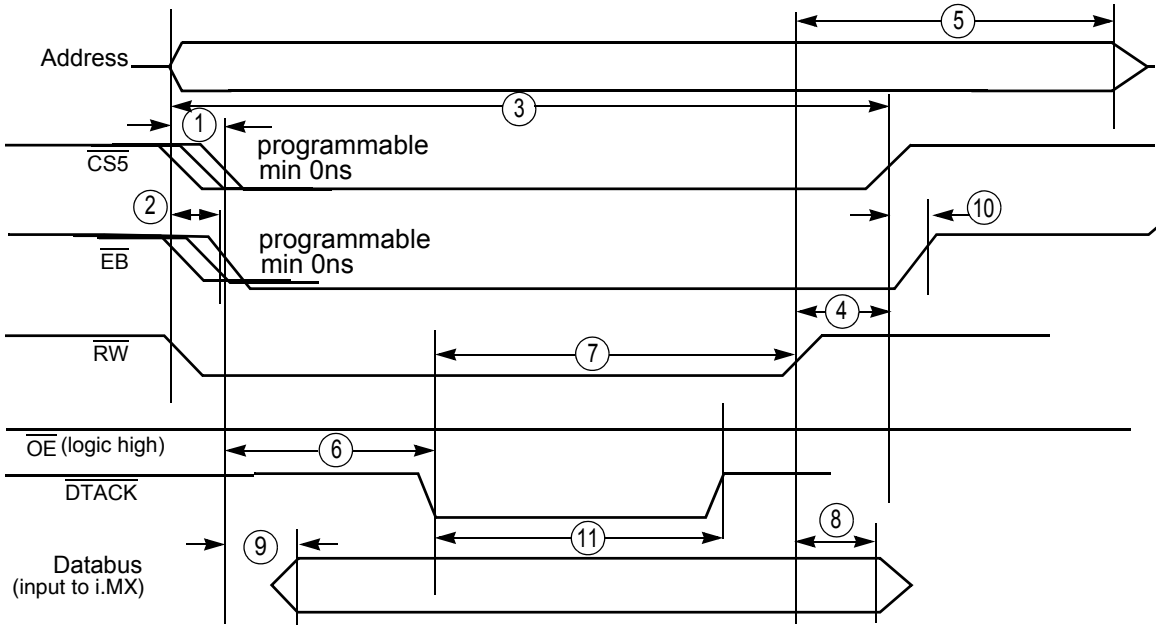


Figure 8. DTACK Write Cycle without DMA

Table 15. Write Cycle without DMA: WSC = 111111, DTACK_SEL=0, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 3	–	ns
2	$\overline{EB}$ assertion time	See note 3	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	1.5T-2.44	1.5T-0.8	ns
5	$\overline{RW}$ negated to address inactive	57.31	–	ns
6	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	–	1019T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	2T+2.37	3T+6.6	ns
8	Data hold timing after $\overline{RW}$ negated	1.5T-3.99	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	0.5T	0.5T+0.5	ns
11	$\overline{DTACK}$ pulse width	1T	3T	ns

Note:
1. $\overline{DTACK}$ asserted means $\overline{DTACK}$ becomes low level.
2. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
3. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programmed by WEA bits in the CS5L register.
4. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
5. The external $\overline{DTACK}$ input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.4 DTACK Write Cycle DMA Enabled

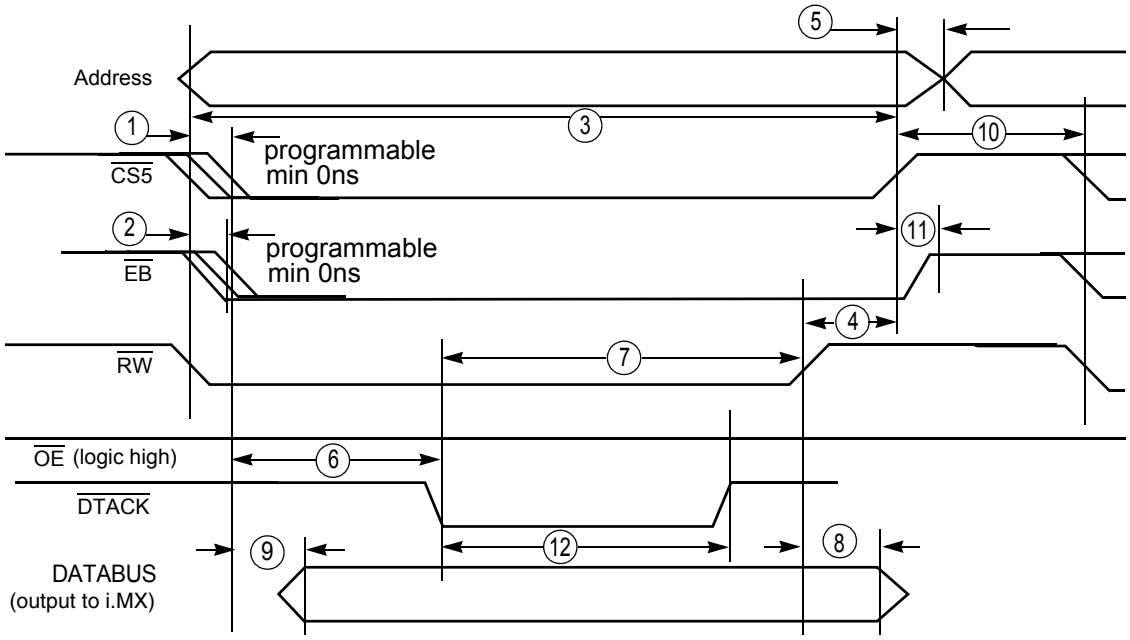


Figure 9. DTACK Write Cycle DMA Enabled

Table 16. Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=0, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 3	–	ns
2	$\overline{EB}$ assertion time	See note 3	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	1.5T-2.44	1.5T-0.8	ns
5	Address inactive after $\overline{CS}$ negated	–	0.3	ns
6	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	–	1019T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	2T+2.37	3T+6.6	ns
8	Data hold timing after $\overline{RW}$ negated	1.5T-3.99	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
11	$\overline{EB}$ negate after $\overline{CS}$ negate	0.5T	0.5T+0.5	ns
12	$\overline{DTACK}$ pulse width	1T	3T	ns

Note:
1. $\overline{DTACK}$ asserted means $\overline{DTACK}$ becomes low level.
2. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
3. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion also can be programmed by WEA bits in the CS5L register.
4. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
5.The external $\overline{DTACK}$ input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.5 WAIT Read Cycle without DMA

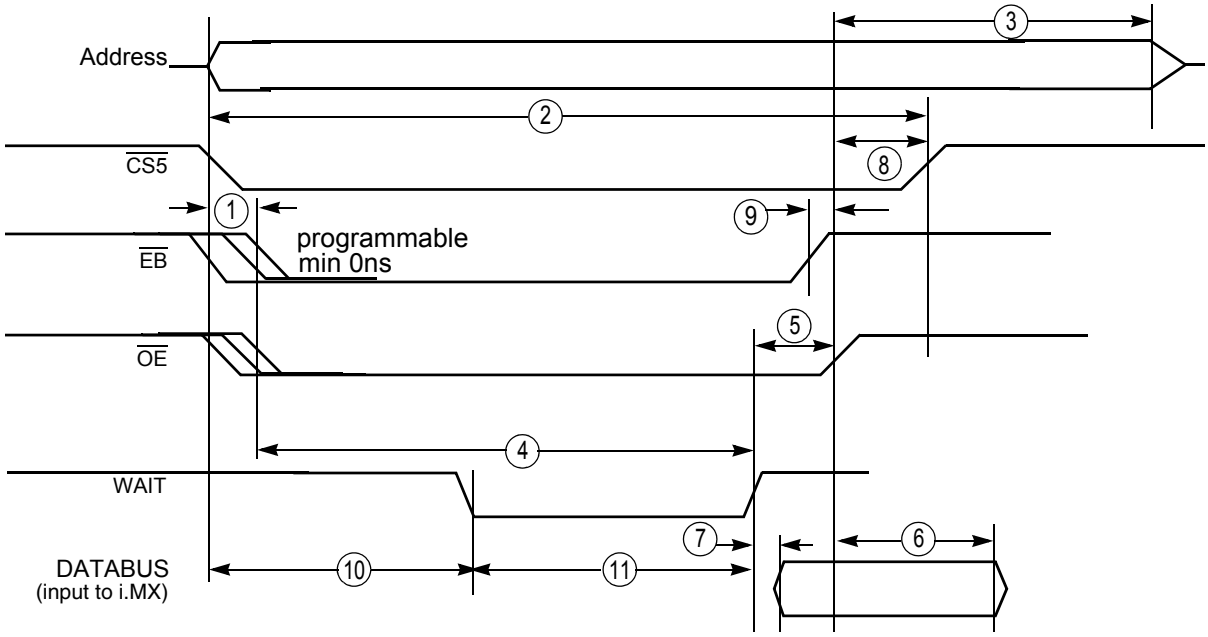


Figure 10. WAIT Read Cycle without DMA

Table 17. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated to address inactive	56.81	57.28	ns
4	Wait asserted after $\overline{OE}$ asserted	–	1020T	ns
5	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
6	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
7	Data ready after wait asserted	0	T	ns
8	OE negated to CS negated	1.5T-0.68	1.5T-0.06	ns
9	OE negated after EB negated	0.06	0.18	ns
10	Become low after CS5 asserted	0	1019T	ns
11	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.6 WAIT Read Cycle DMA Enabled

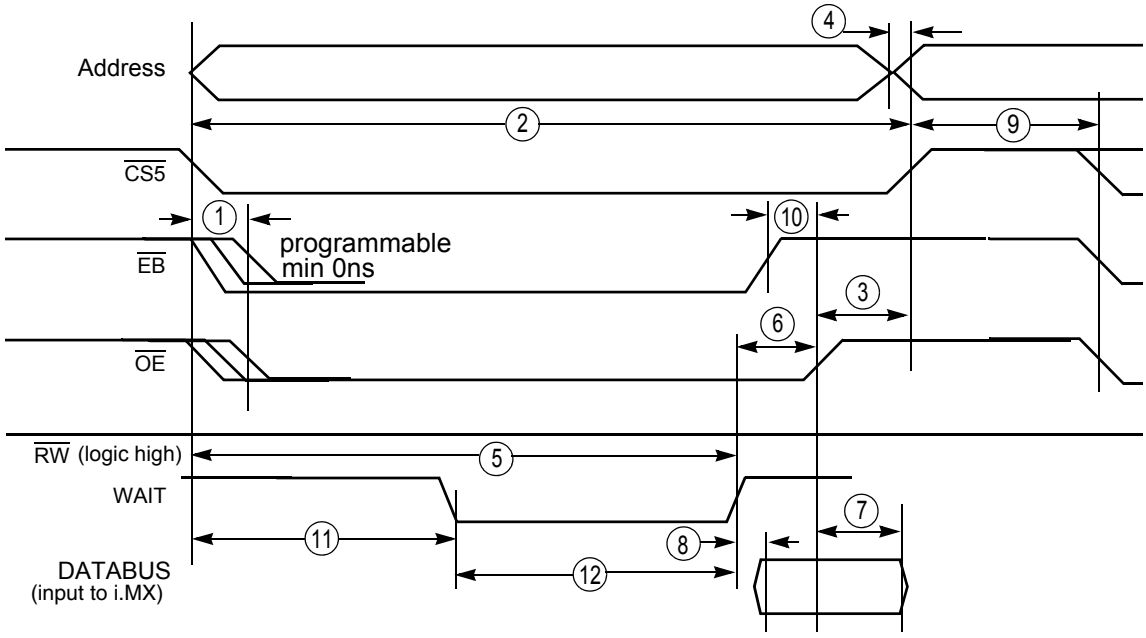


Figure 11. WAIT Read Cycle DMA Enabled

Table 18. WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	1.5T-0.68	1.5T-0.06	ns
4	Address inactived before $\overline{CS}$ negated	–	0.05	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
7	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
8	Data ready after wait is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T		ns
10	OE negate after EB negate	0.06	0.18	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.7 WAIT Write Cycle without DMA

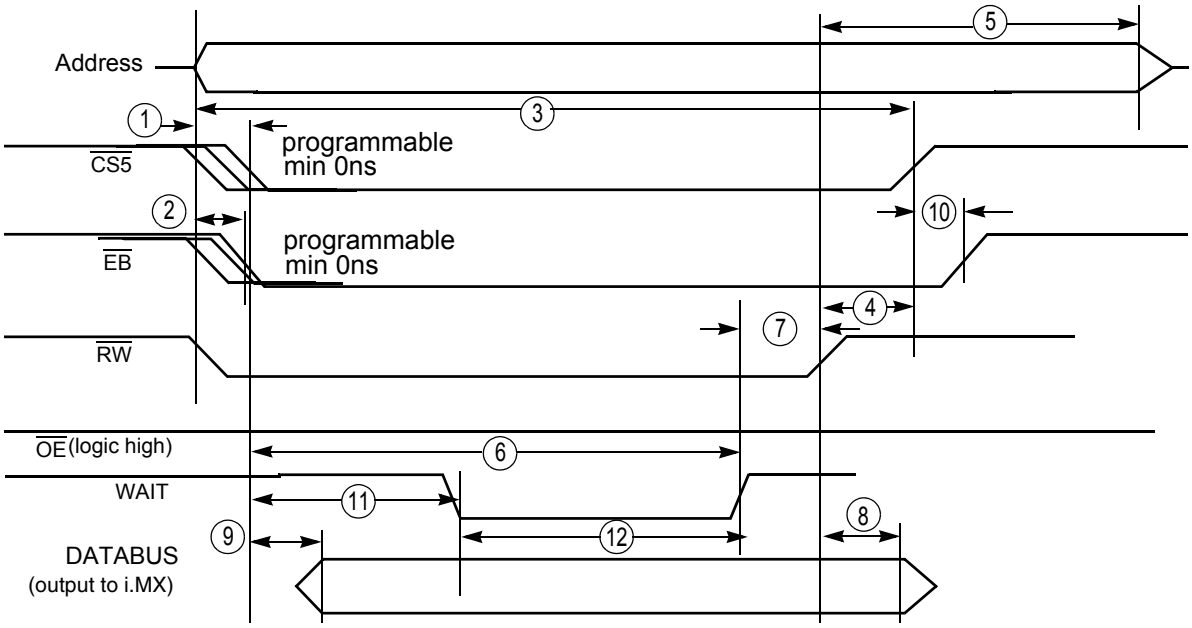


Figure 12. WAIT Write Cycle without DMA

Table 19. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	$\overline{RW}$ negated to Address inactive	64.22	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{RW}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{RW}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	0.5T	0.5T+0.5	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.2.8 WAIT Write Cycle DMA Enabled

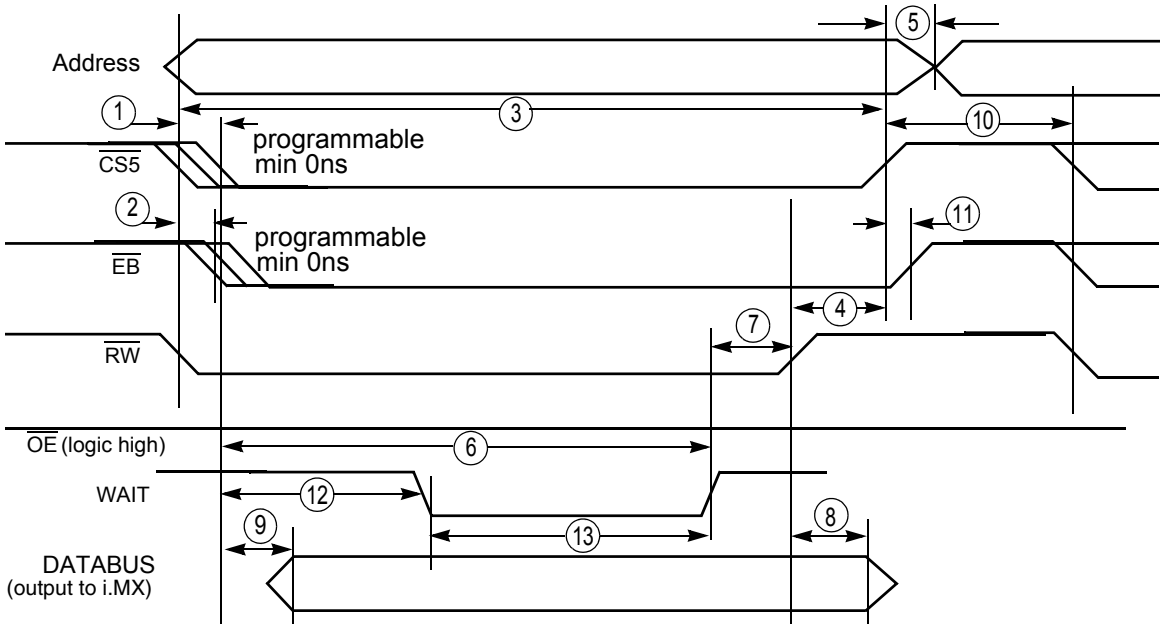


Figure 13. WAIT Write Cycle DMA Enabled

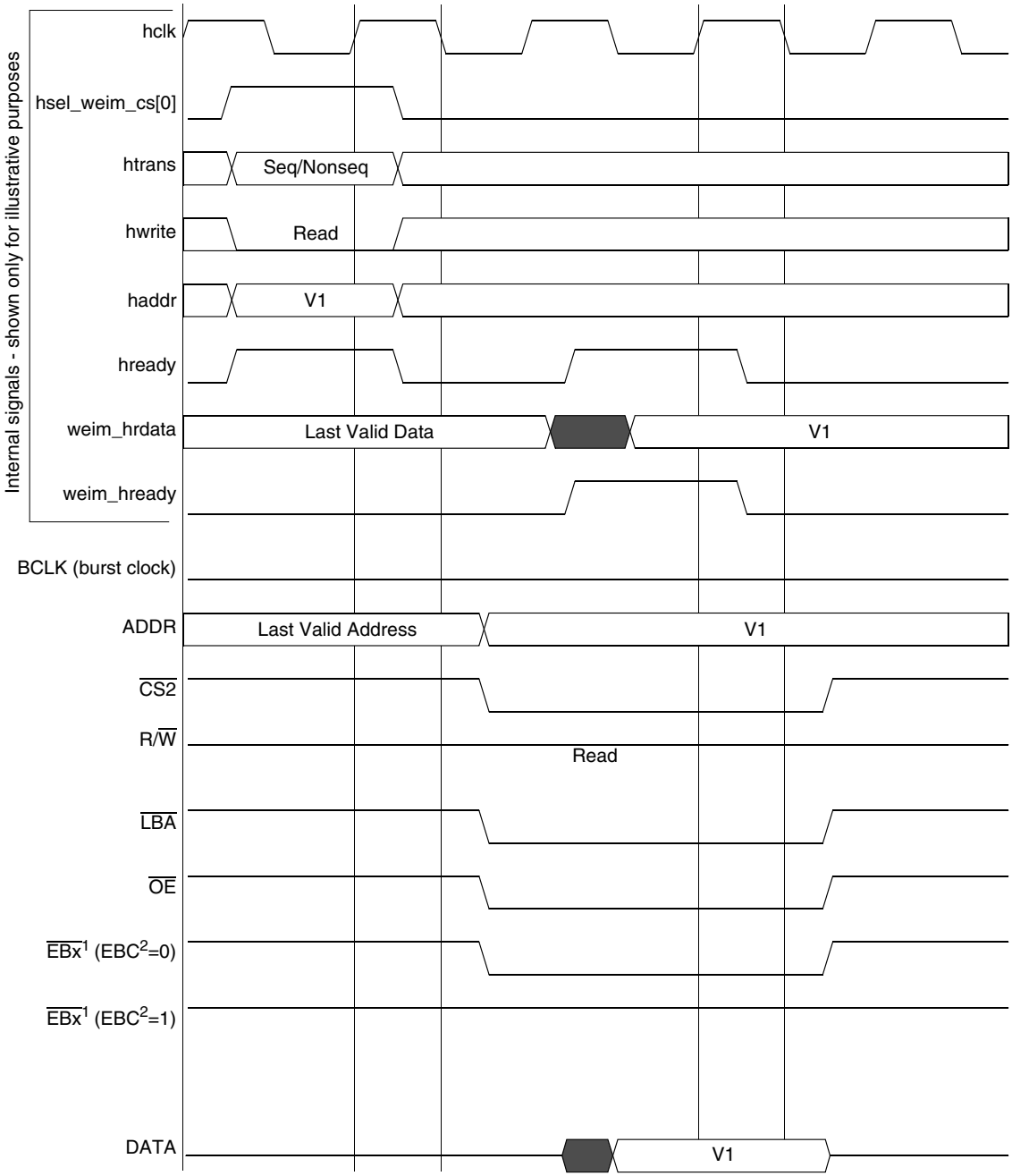
Table 20. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	Address inactived after $\overline{CS}$ negated	–	0.09	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{RW}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{RW}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
11	$\overline{EB}$ negate after $\overline{CS}$ negate	0.5T	0.5T+0.5	
12	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion also can be programable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

3.9.3 EIM External Bus Timing

The following timing diagrams show the timing of accesses to memory or a peripheral.



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 1, A.HALF/E.HALF

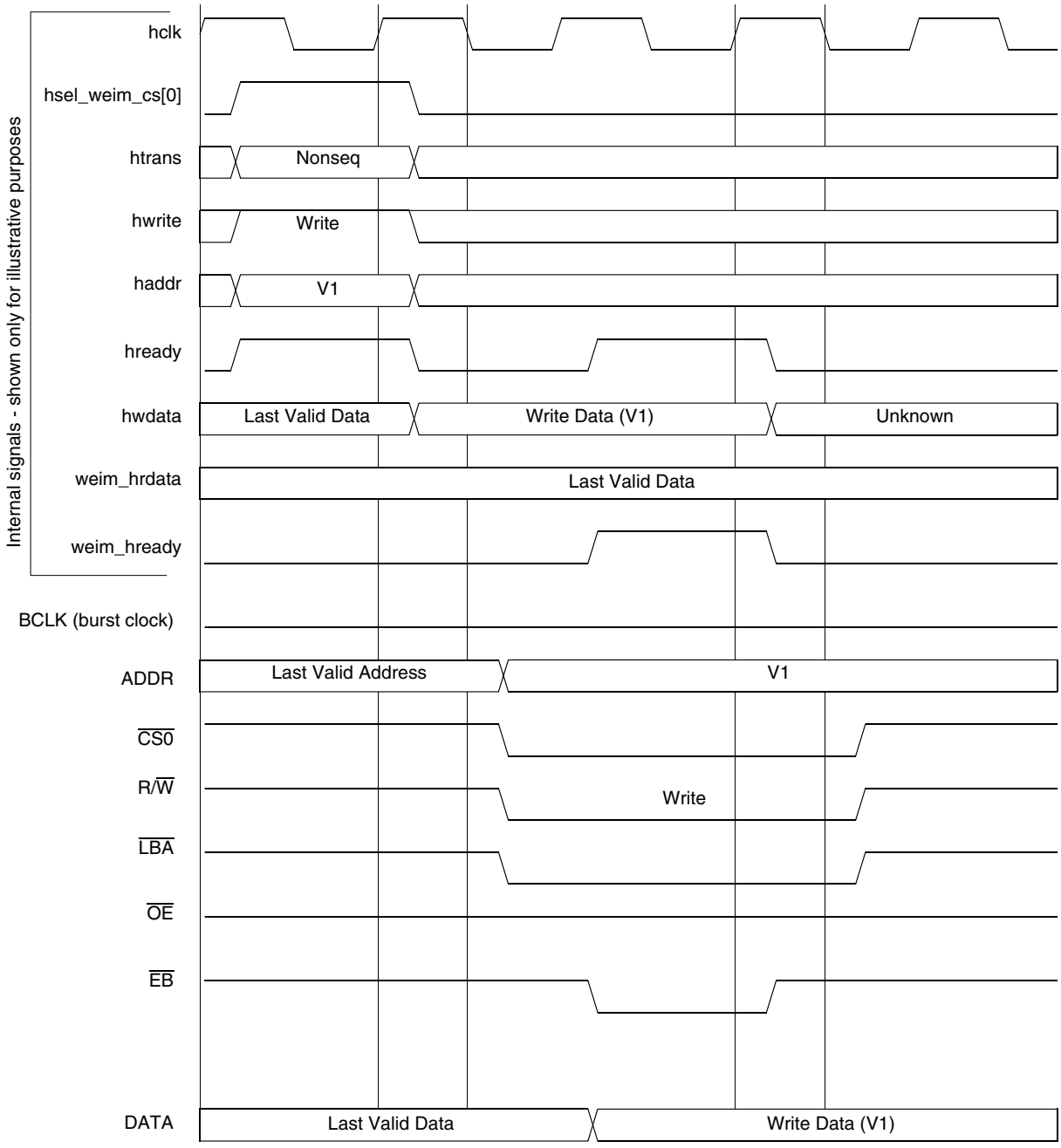
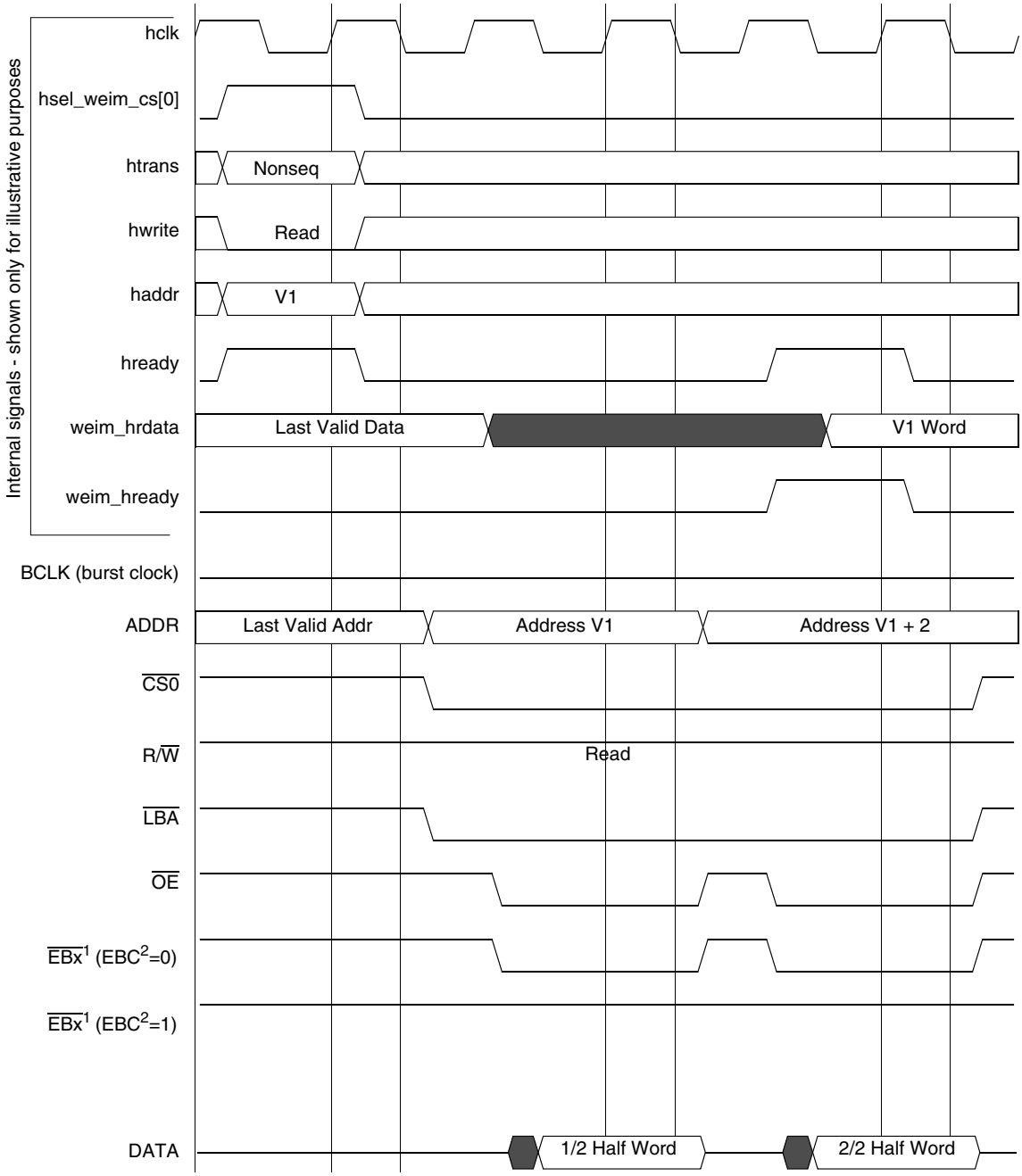


Figure 15. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 16. WSC = 1, OEA = 1, A.WORD/E.HALF

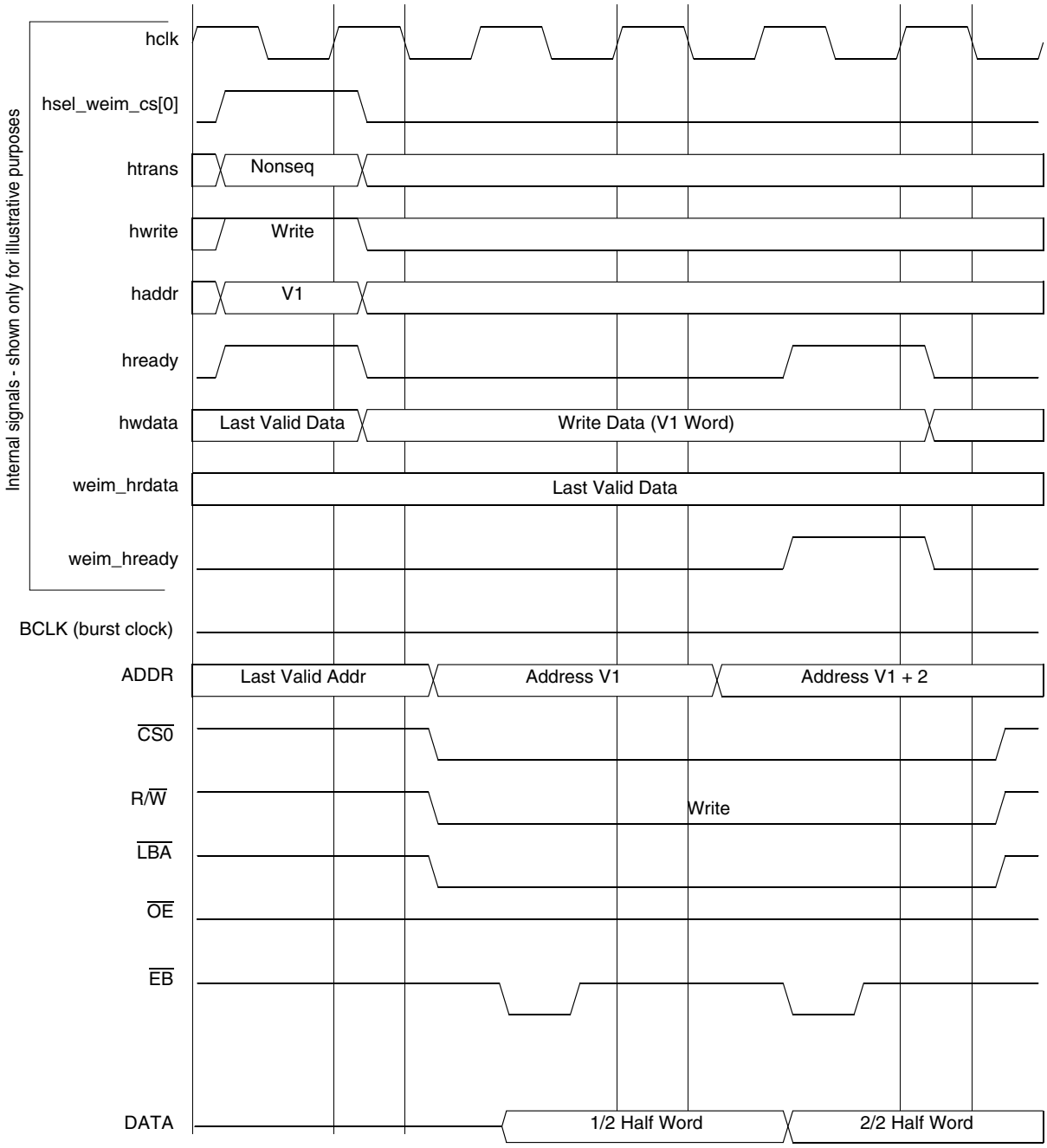
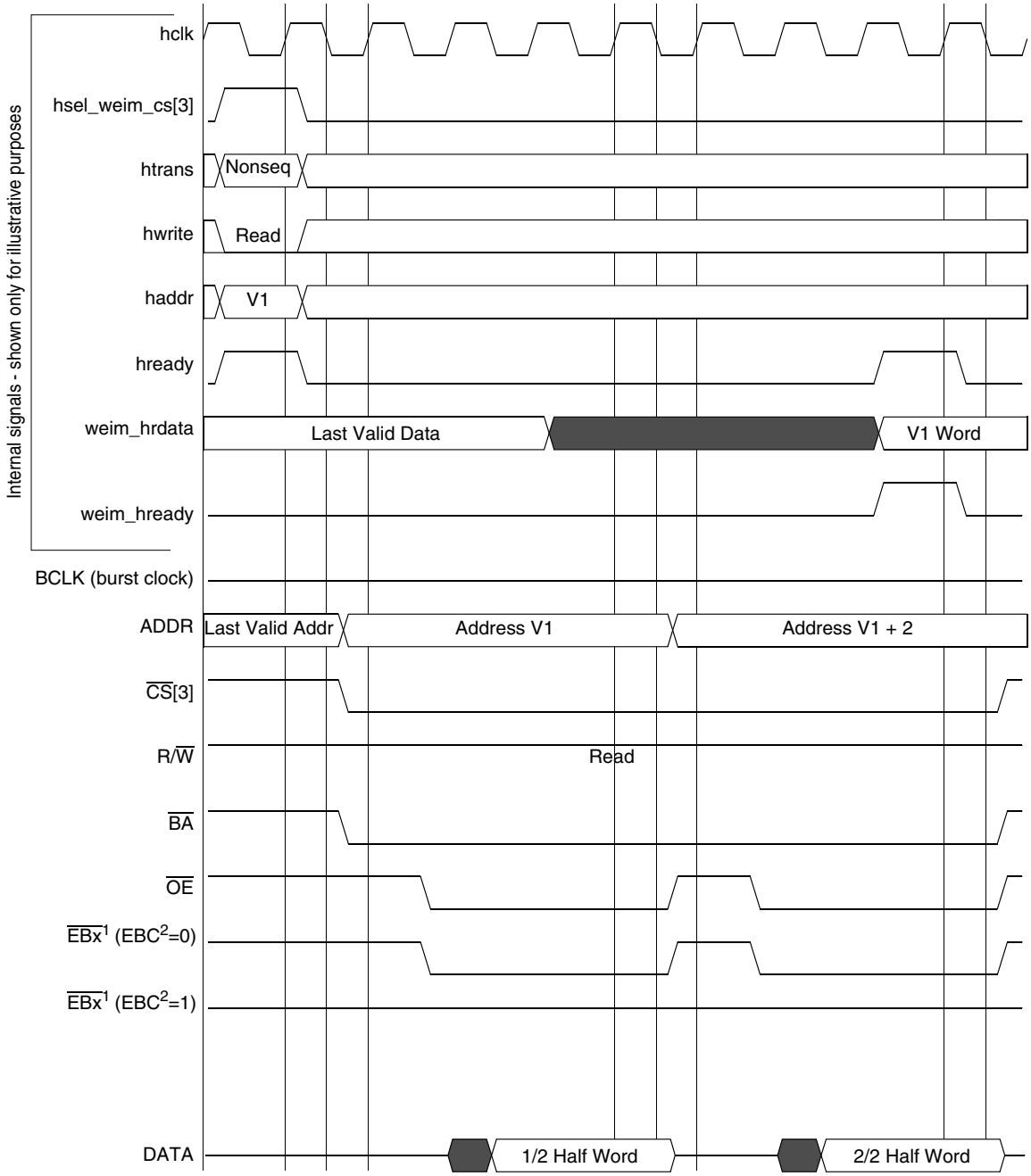


Figure 17. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEA = 2, A.WORD/E.HALF

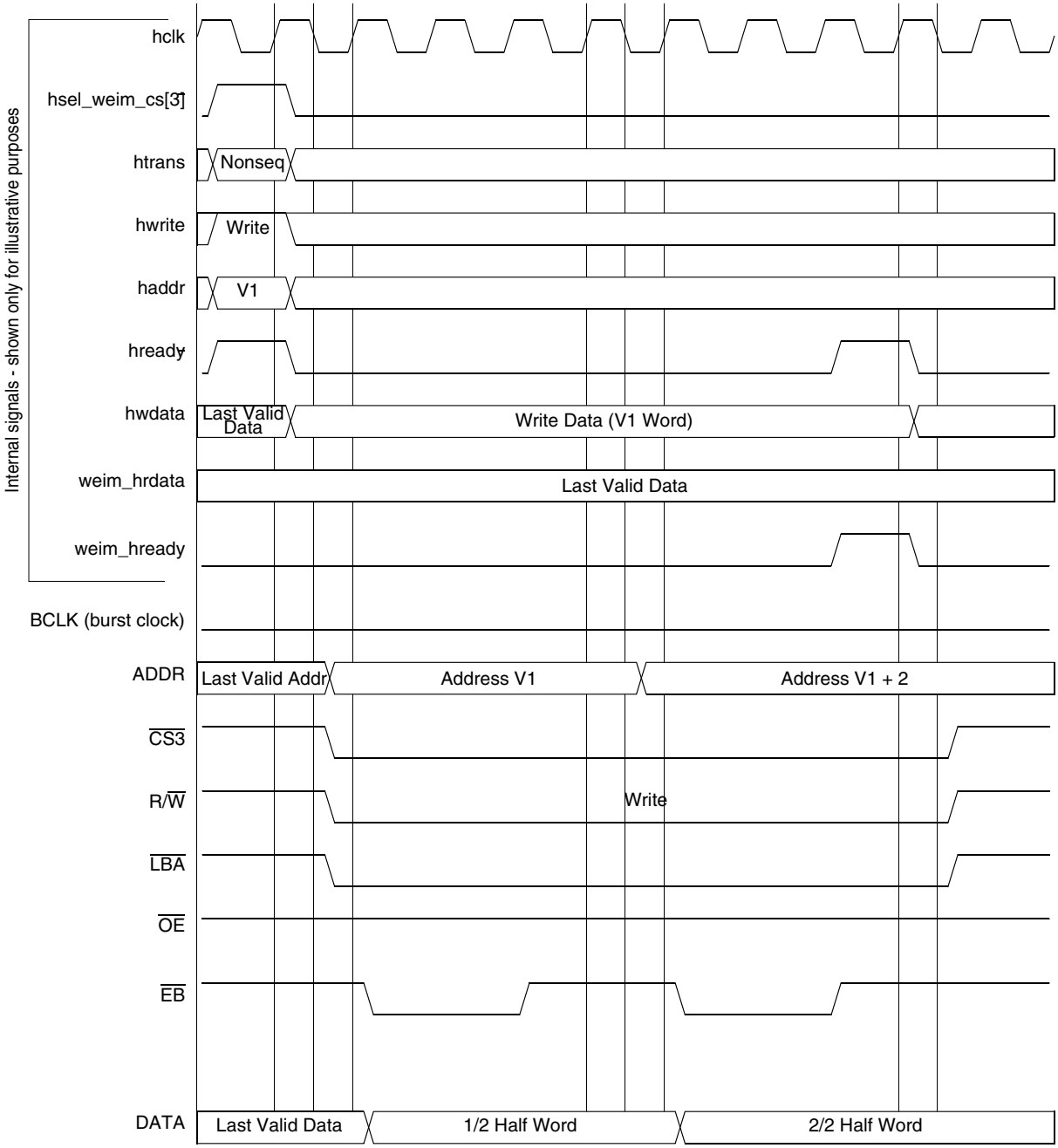
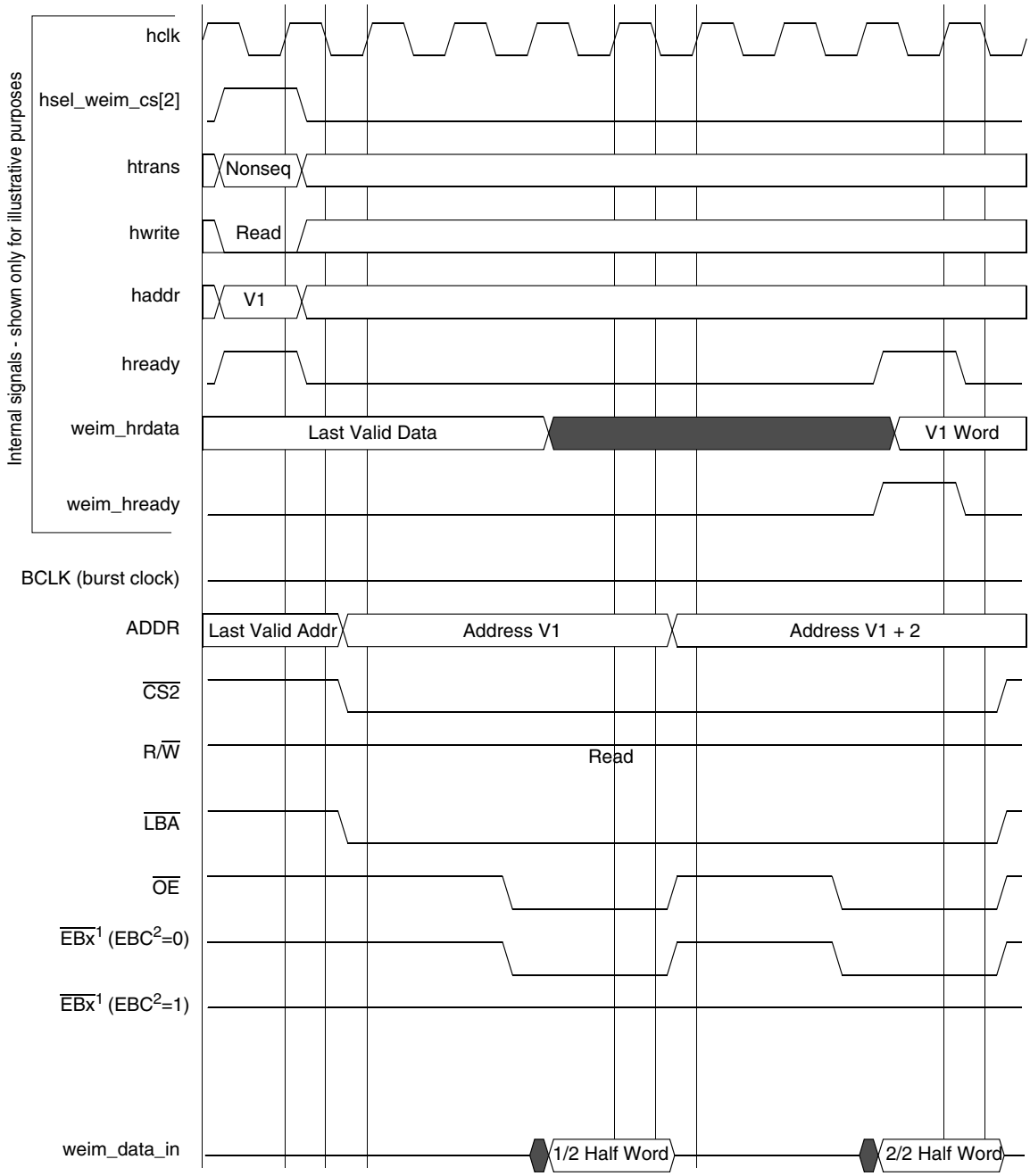


Figure 19. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 20. WSC = 3, OEA = 4, A.WORD/E.HALF

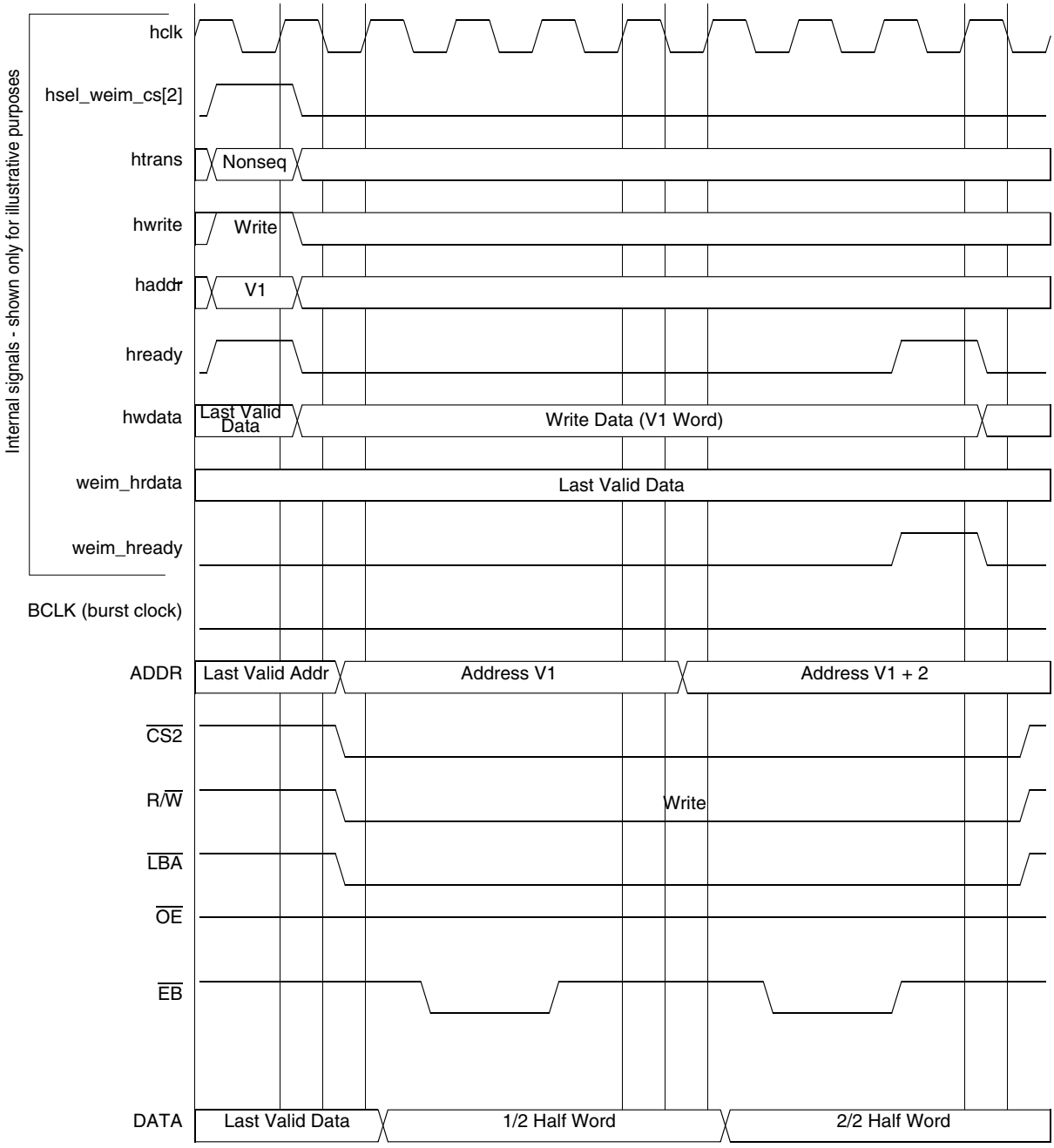
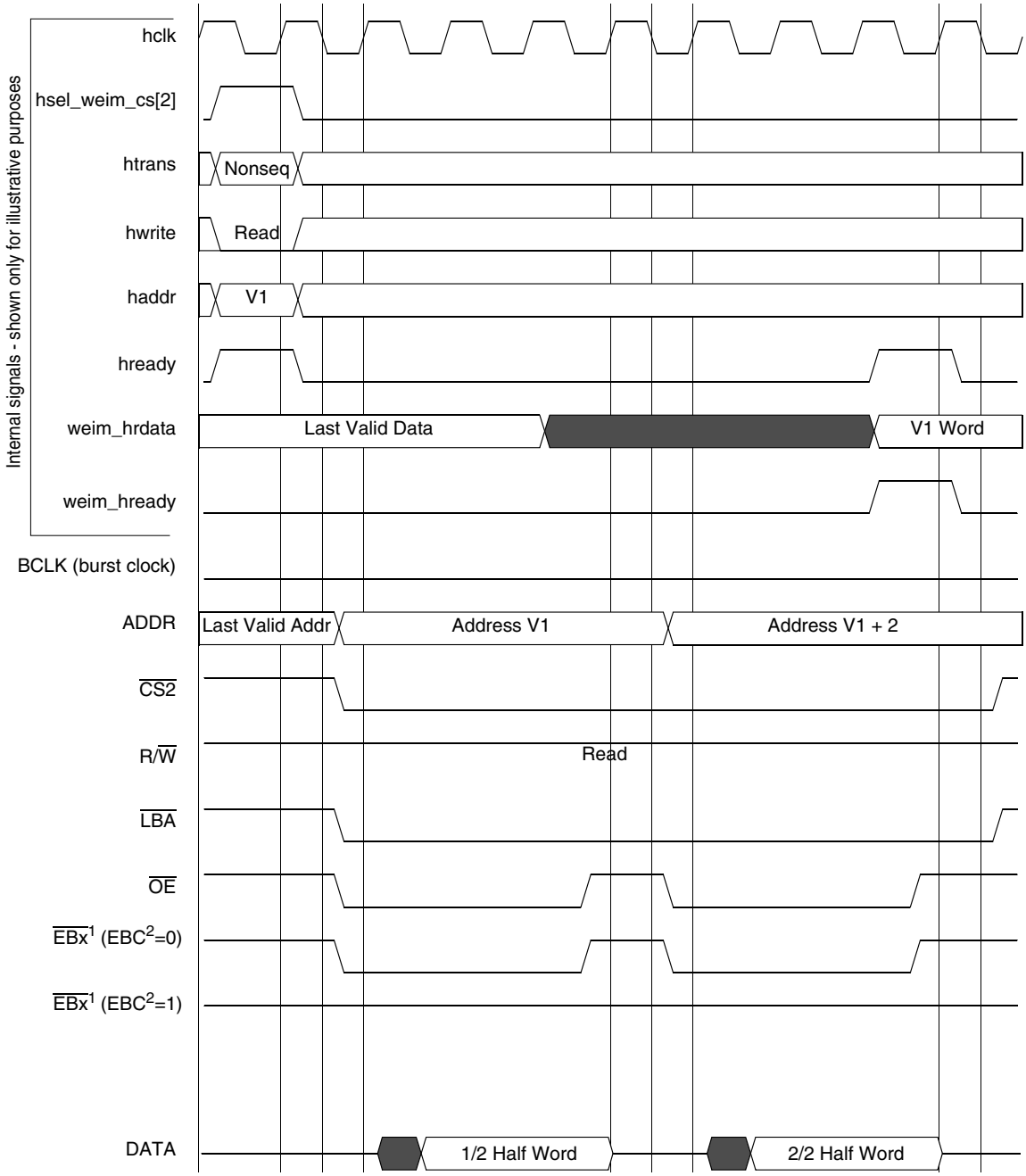
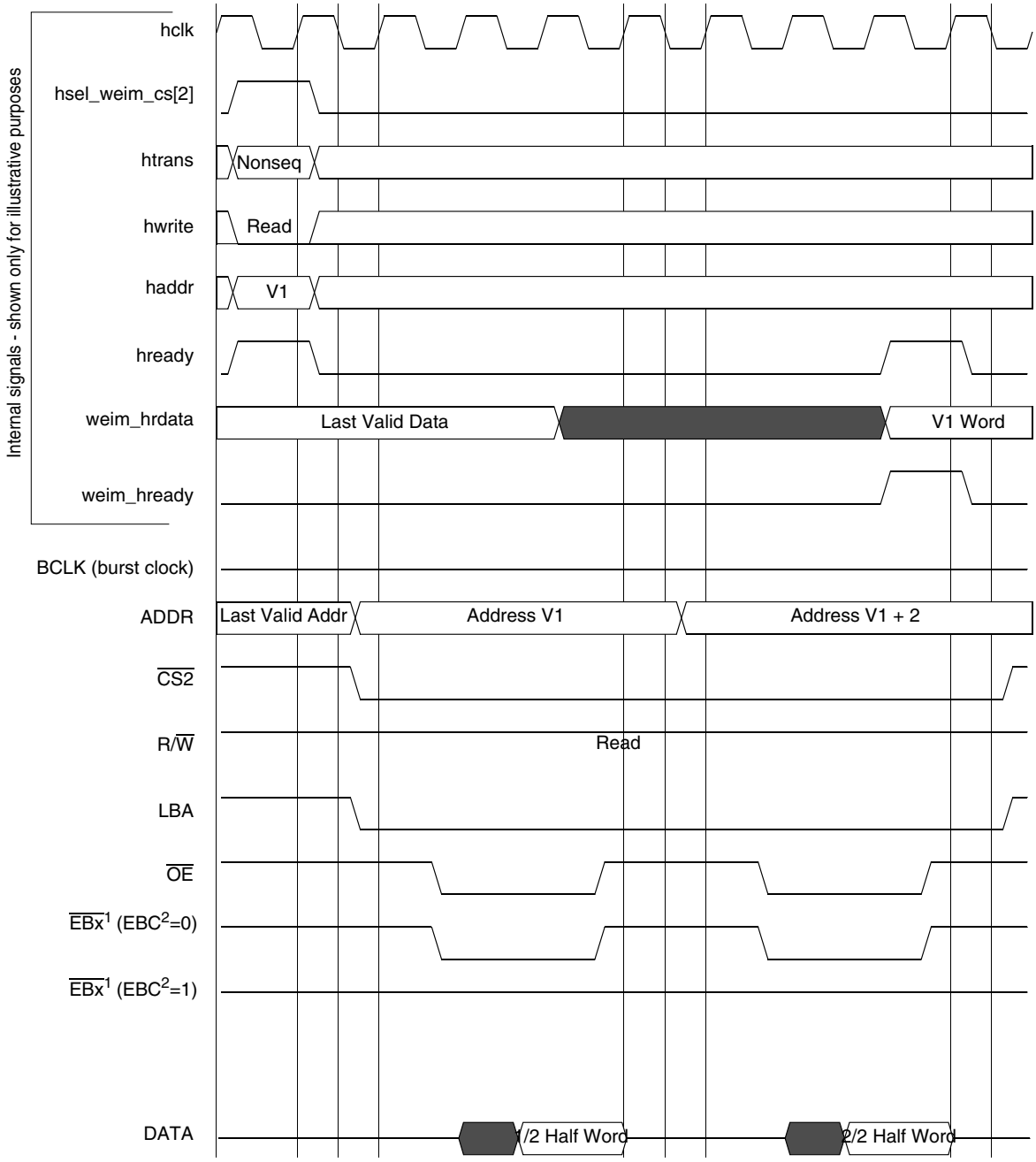


Figure 21. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 3, OEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

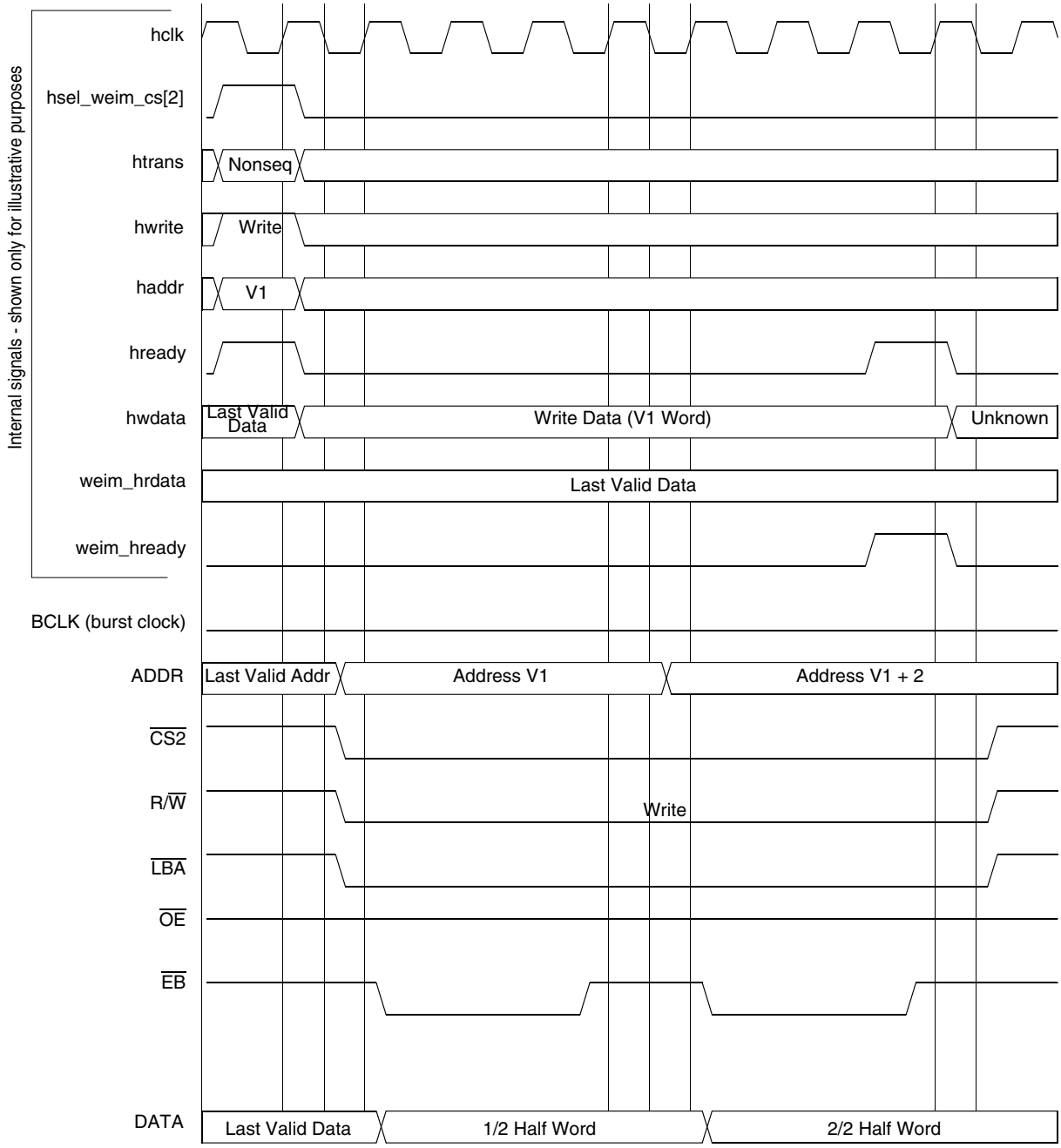


Figure 24. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

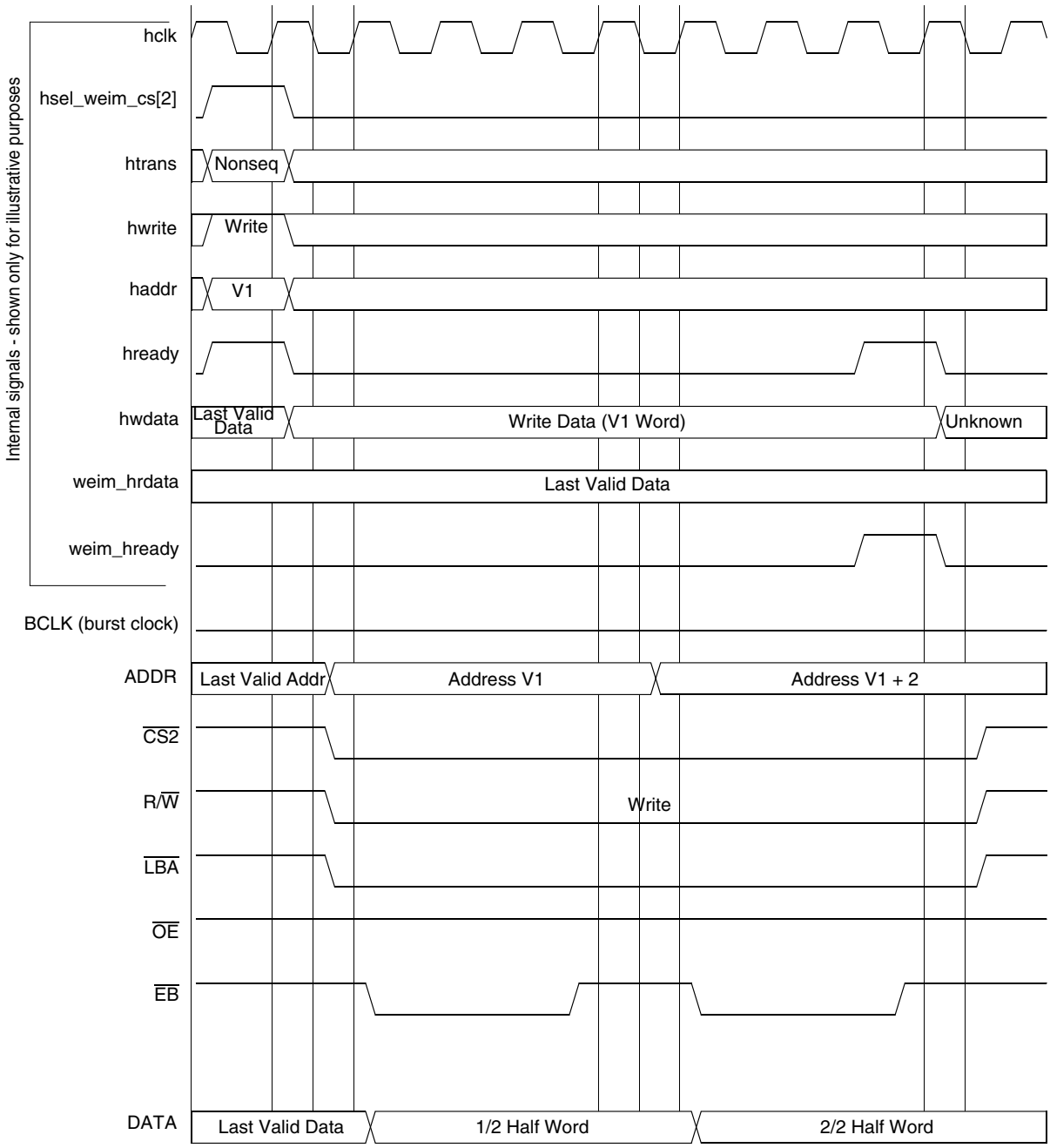
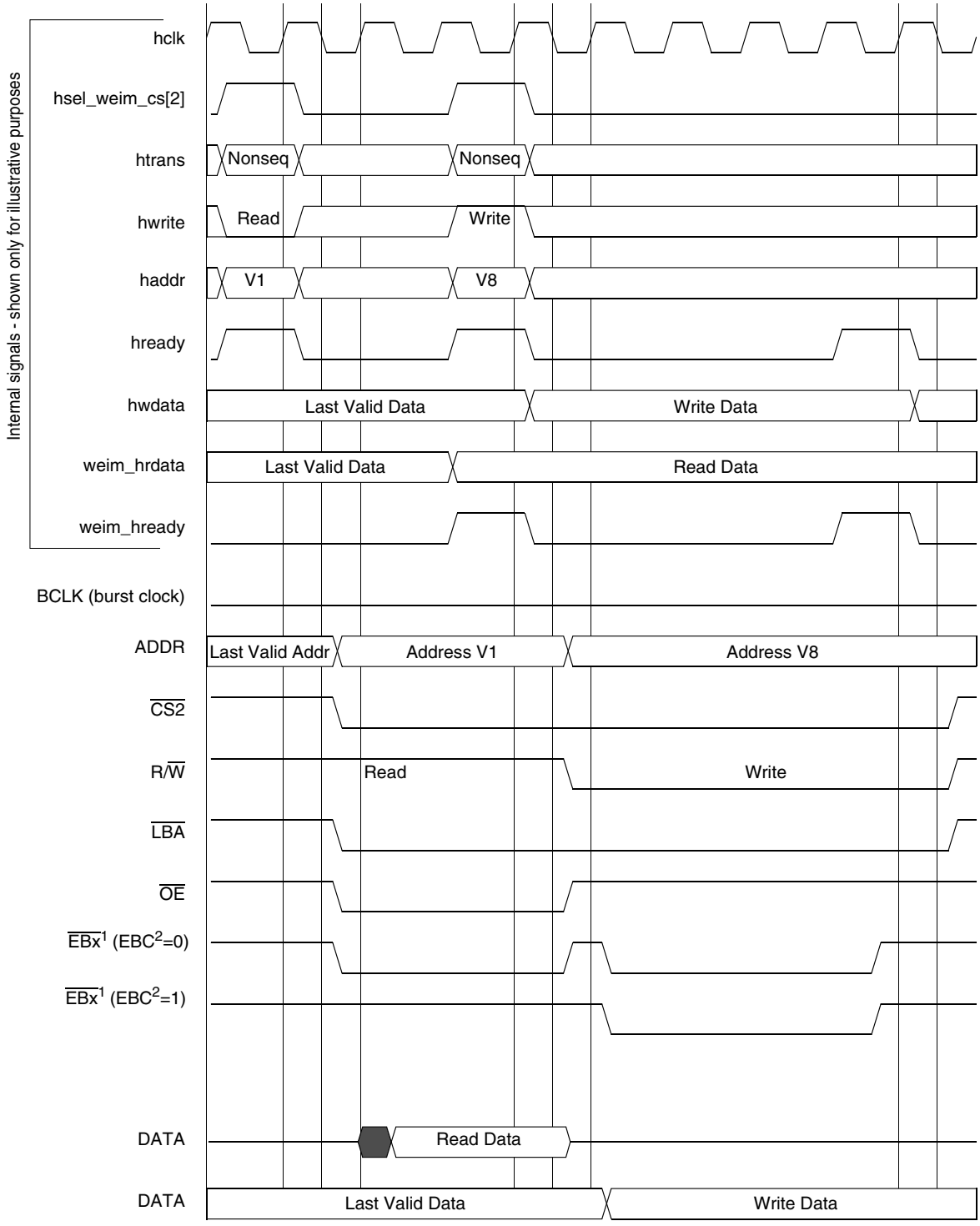
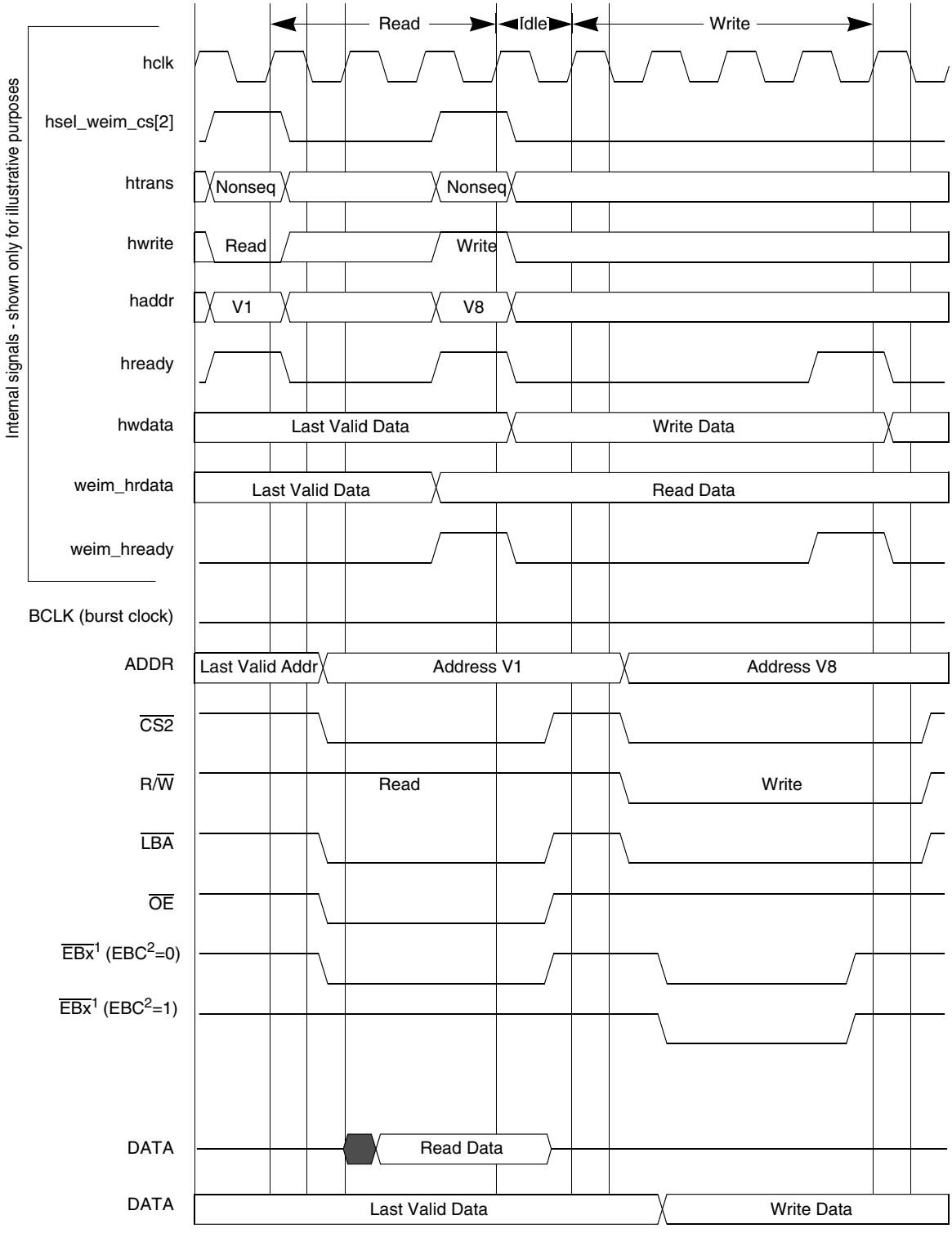


Figure 25. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF

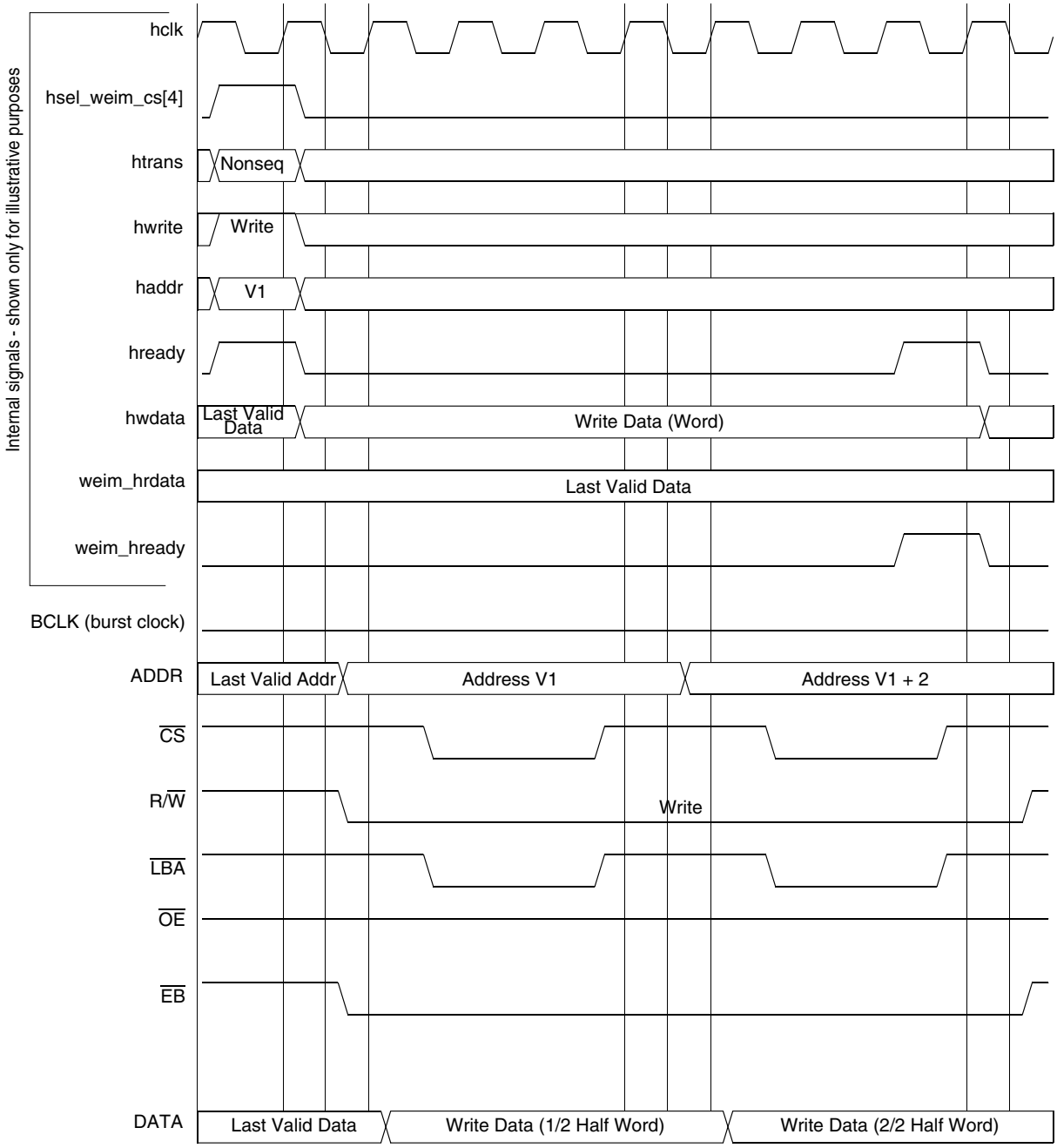
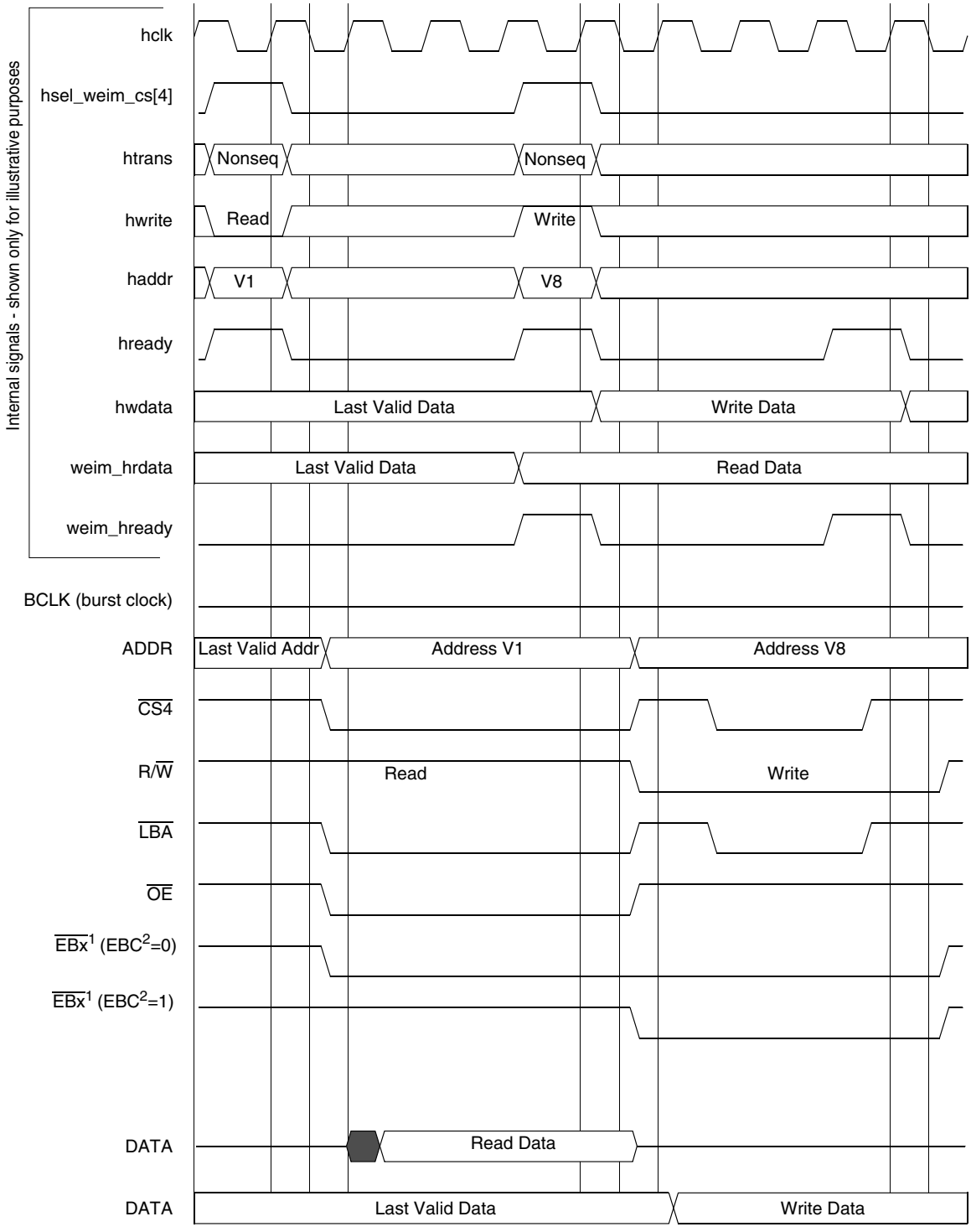
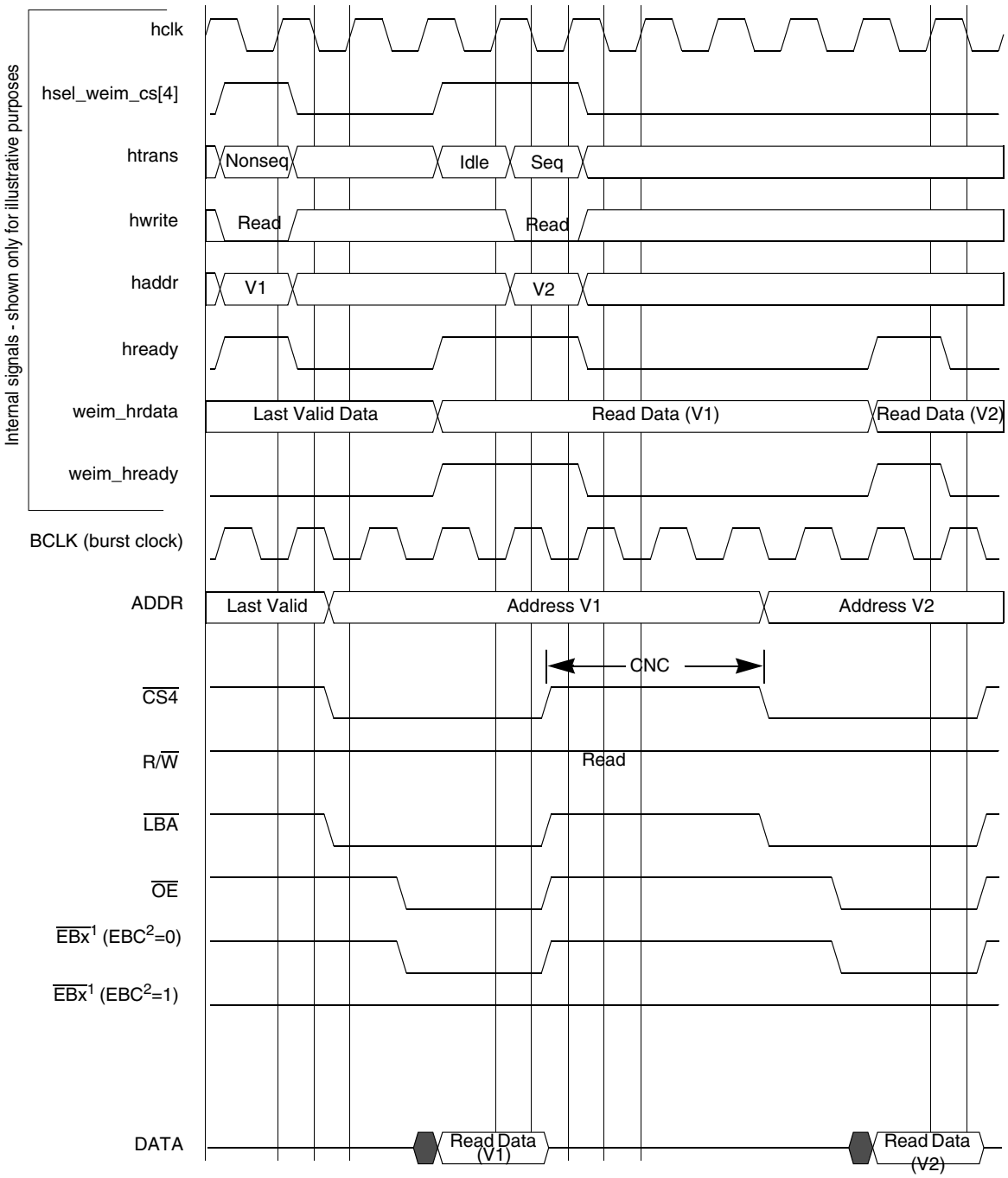


Figure 28. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



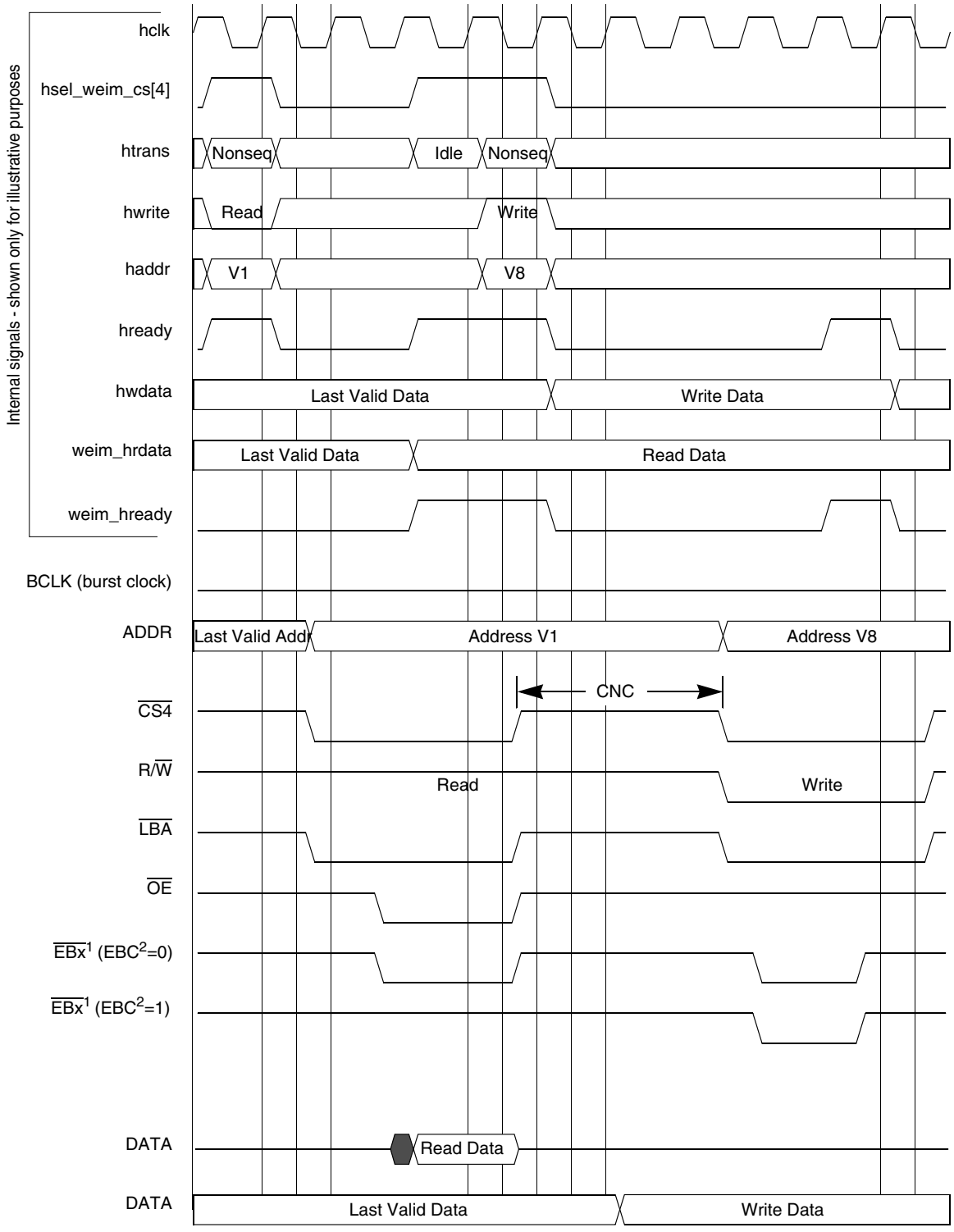
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 3, CSA = 1, A.HALF/E.HALF



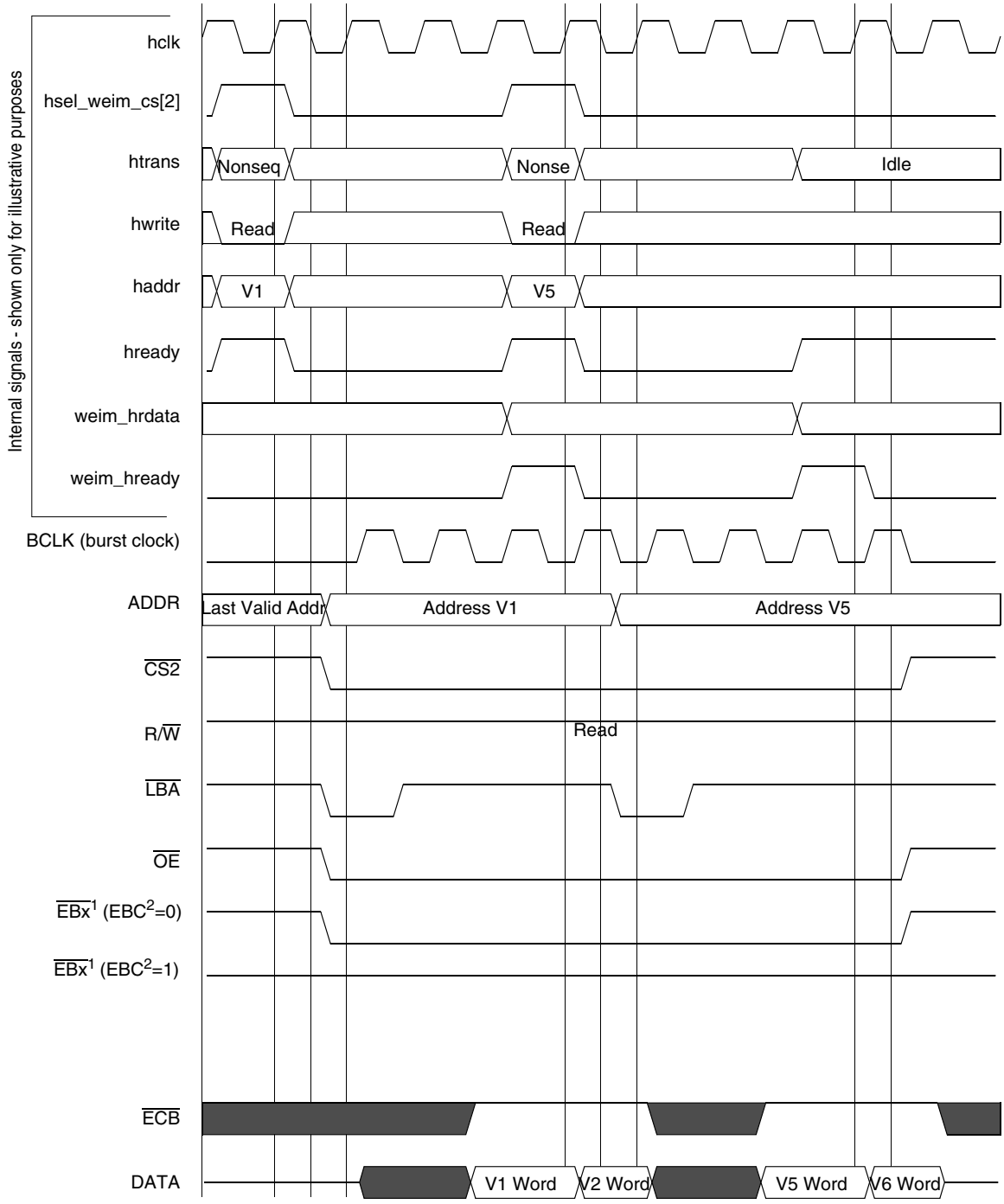
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 30. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF



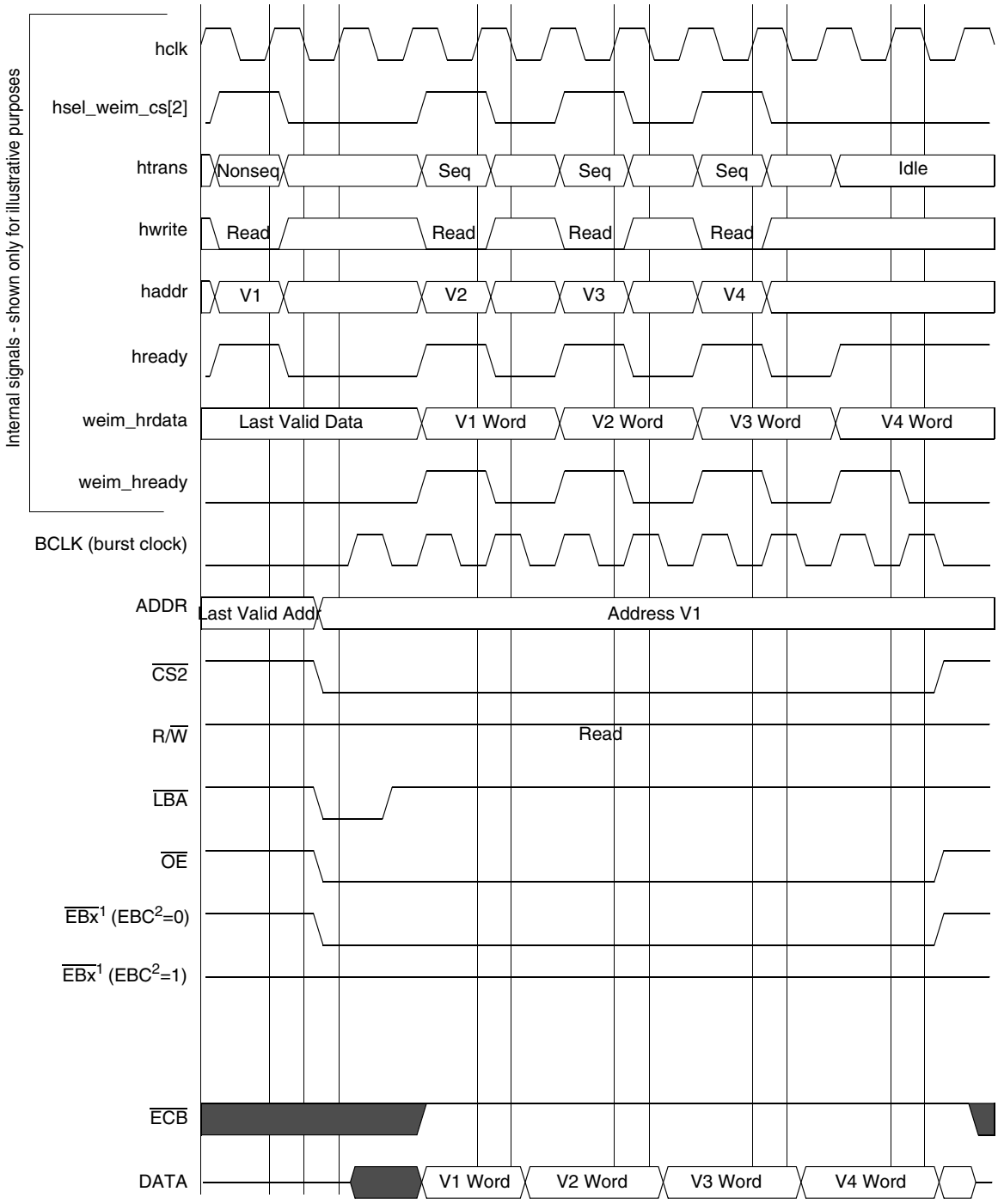
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 31. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



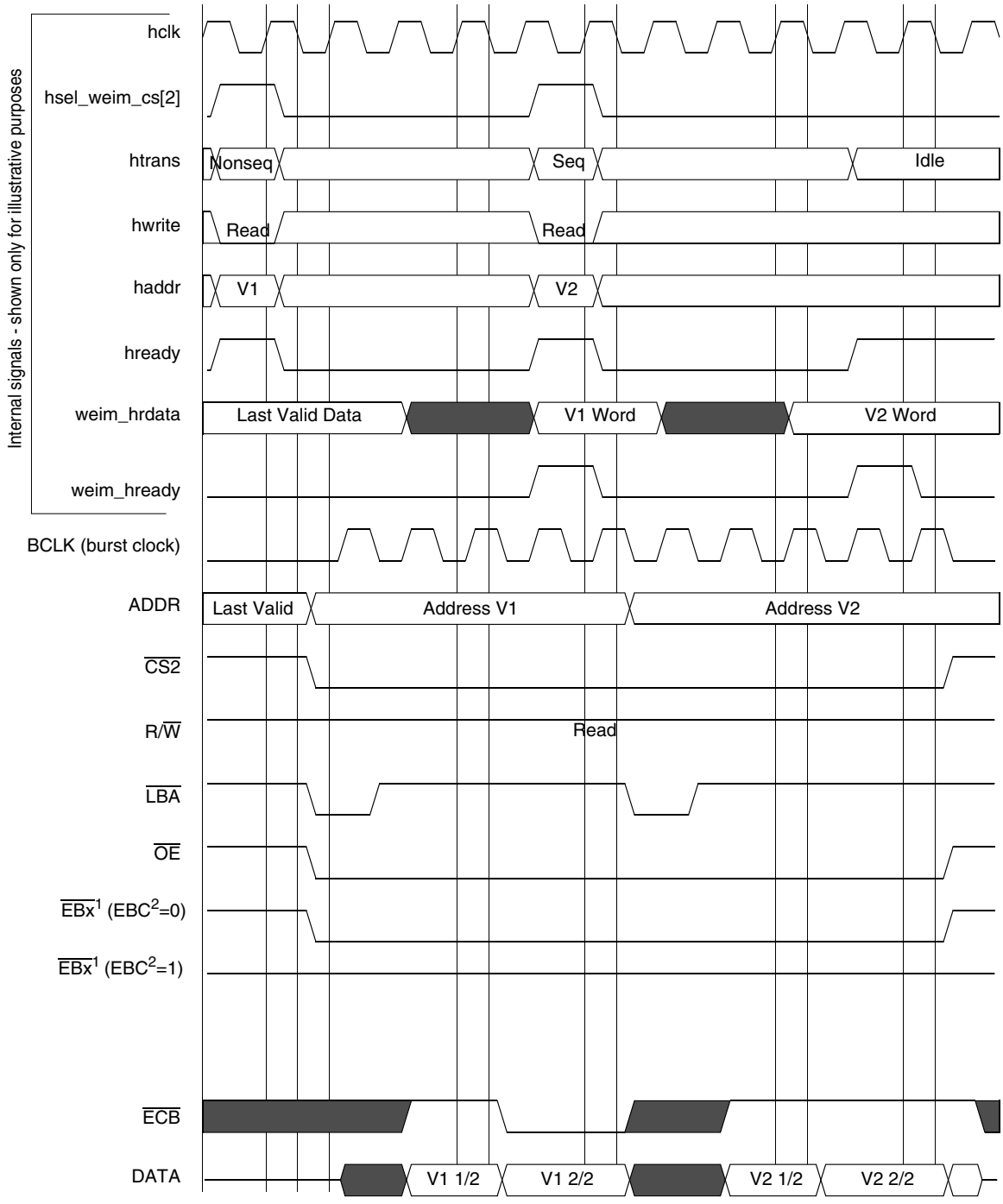
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 32. WSC = 3, SYNC = 1, A.HALF/E.HALF



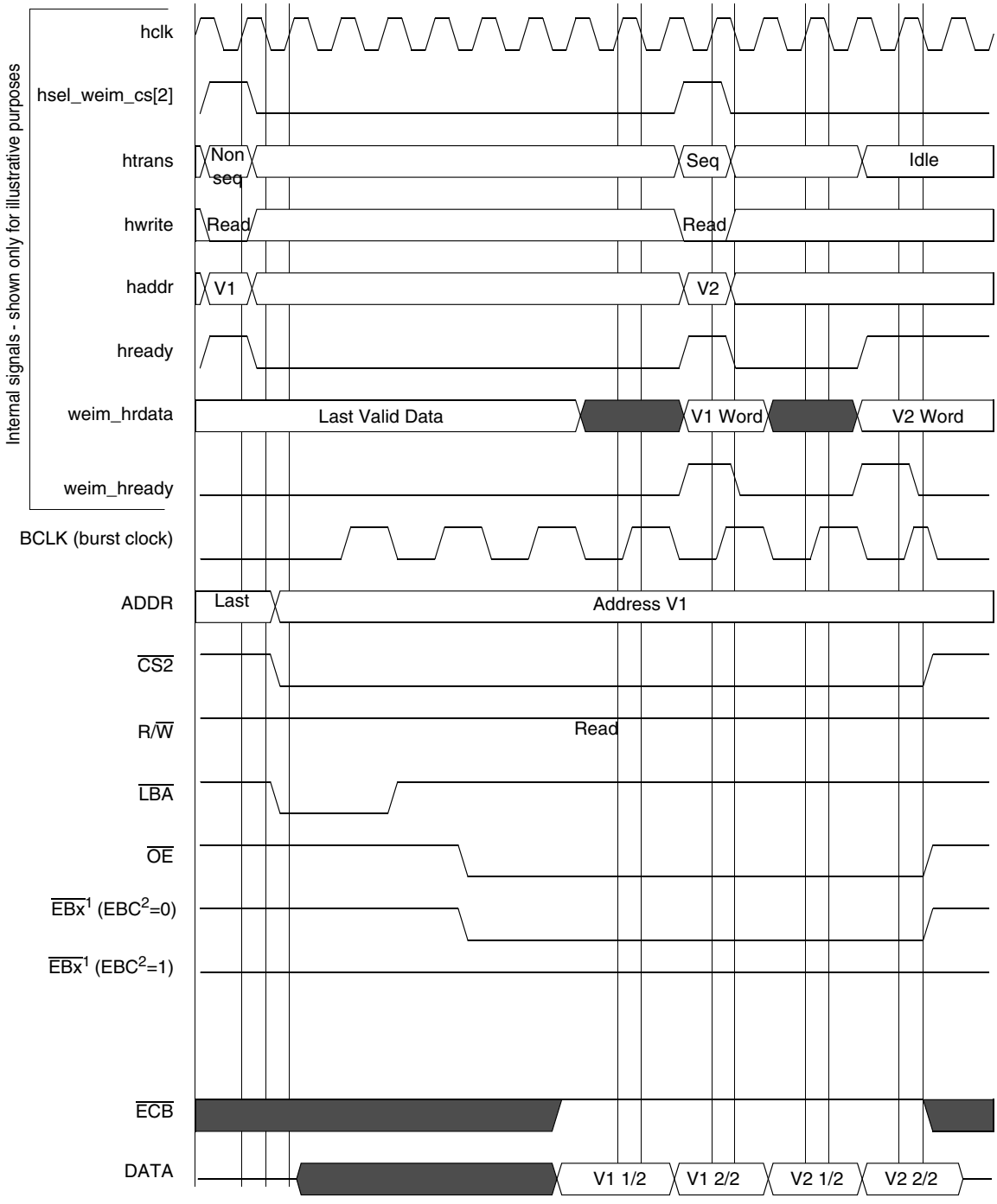
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 33. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD



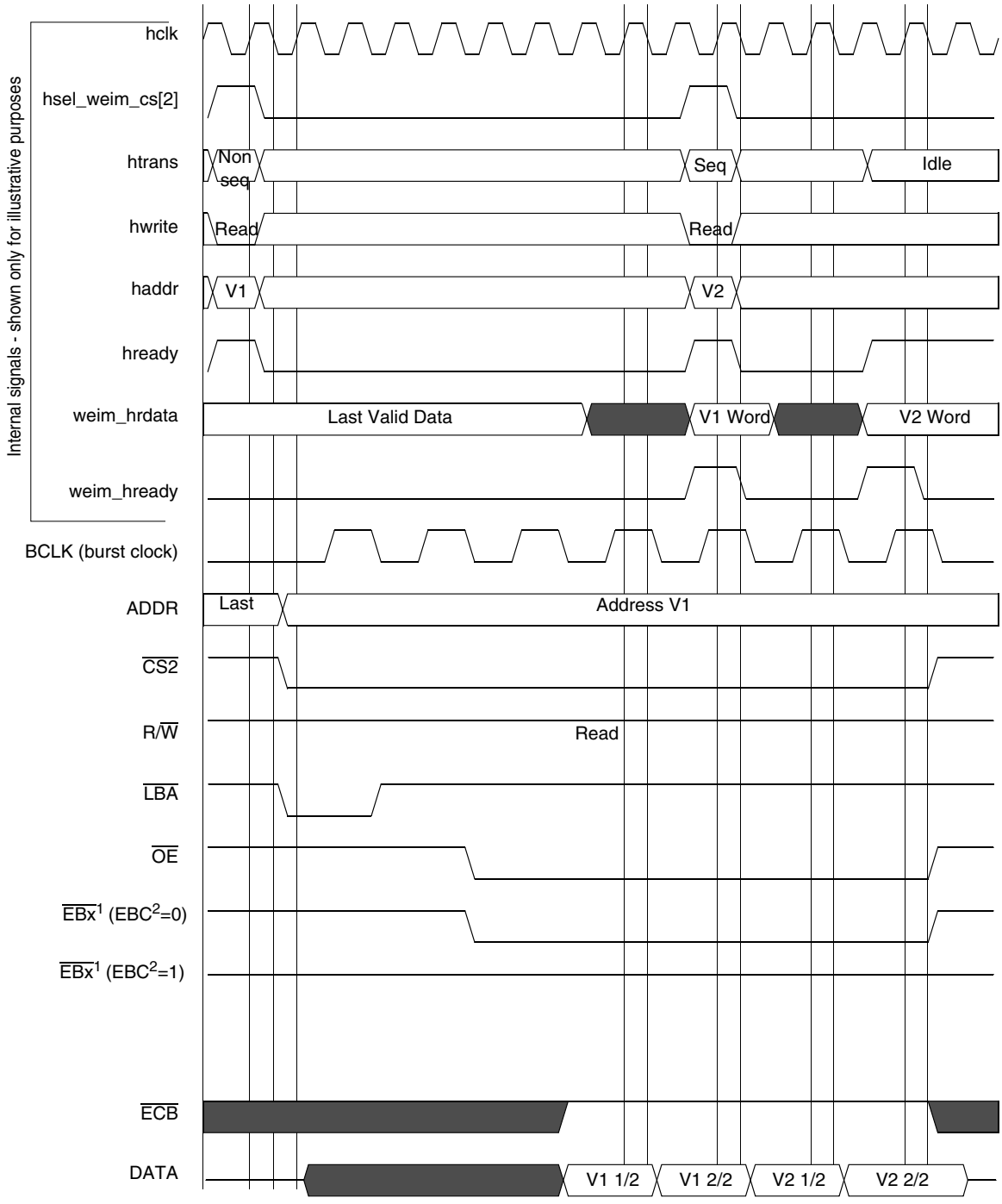
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 34. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 35. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 36. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

3.9.4 Non-TFT Panel Timing

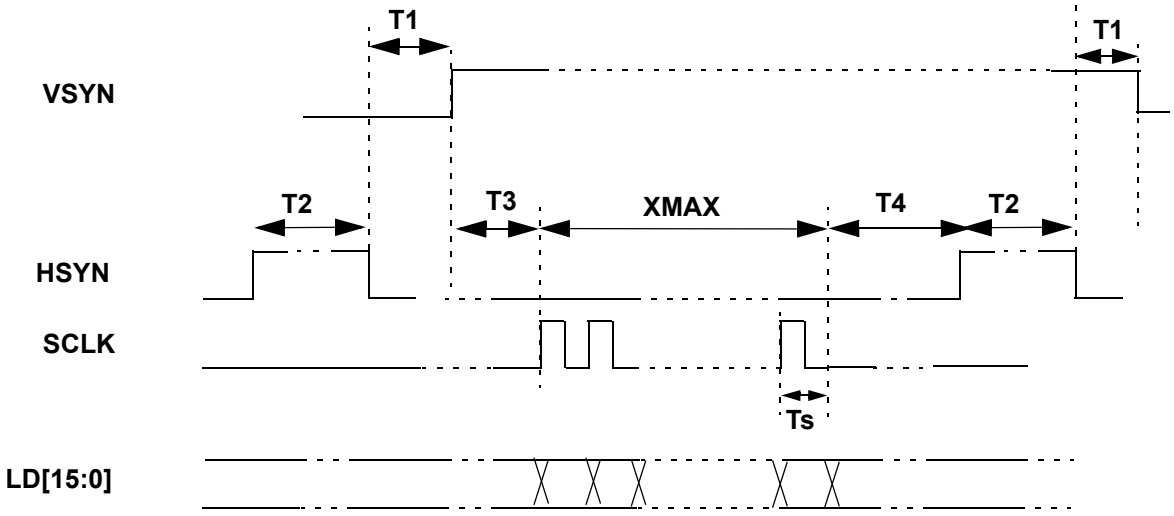


Figure 37. Non-TFT Panel Timing

Table 21. Non TFT Panel Timing Diagram

Symbol	Parameter	Allowed Register Minimum Value	Actual Value	Unit
T1	HSYN to VSYN delay	0	HWAIT2+2	Tpix
T2	HSYN pulse width	0	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	0<= T3<=Ts	–
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

- VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.
- Ts is the shift clock period.
- Ts = Tpix * (panel data bus width).
- Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).
- Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.
- Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

3.10 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) can also be programmed to a fixed data transfer rate. When the SPI module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 38 through Figure 42 show the timing relationship of the master SPI using different triggering mechanisms.

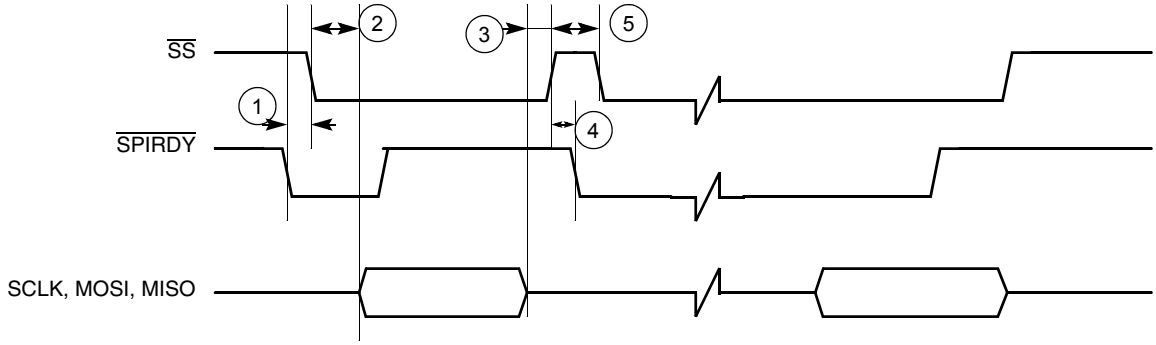


Figure 38. Master SPI Timing Diagram Using $\overline{SPI\_RDY}$ Edge Trigger

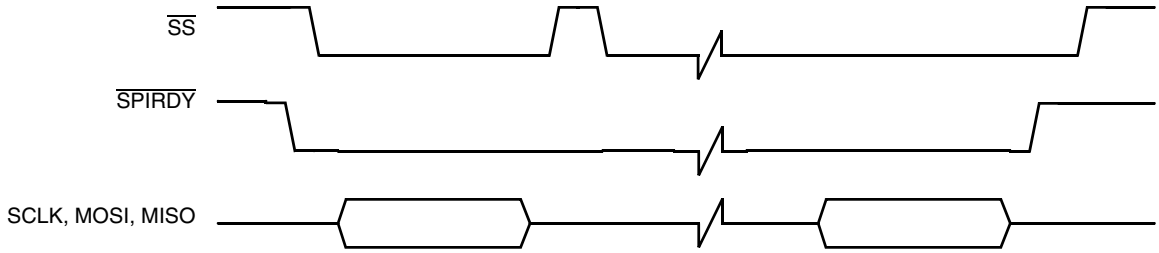


Figure 39. Master SPI Timing Diagram Using $\overline{SPI\_RDY}$ Level Trigger

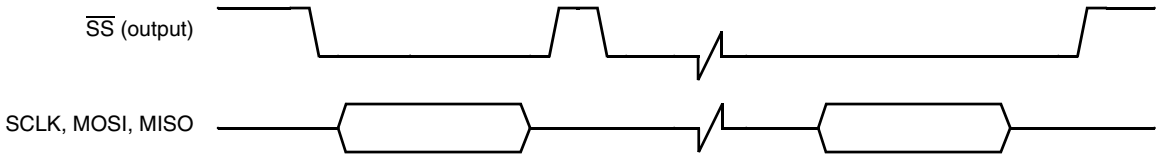


Figure 40. Master SPI Timing Diagram Ignore $\overline{SPI\_RDY}$ Level Trigger

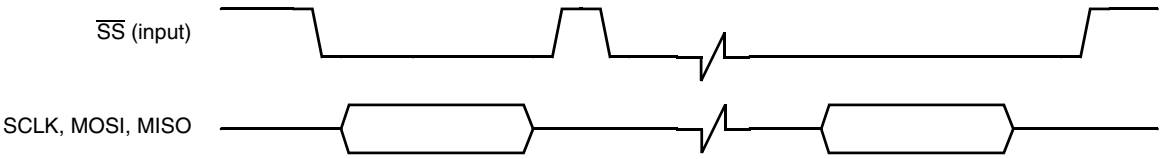


Figure 41. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

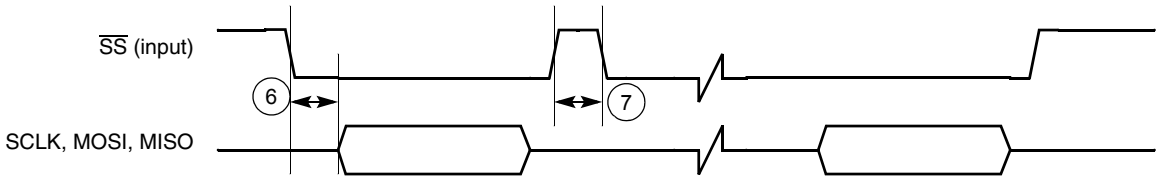


Figure 42. Slave SPI Timing Diagram FIFO Advanced by SS Rising Edge

Table 22. Timing Parameter Table for Figure 38 through Figure 42

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	SPI_RDY to SS output low	2T[1]	–	ns
2	SS output low to first SCLK edge	3 • Tsclk[2]	–	ns
3	Last SCLK edge to SS output high	2 • Tsclk	–	ns
4	SS output high to SPI_RDY low	0	–	ns
5	SS output pulse width	Tsclk + WAIT [3]	–	ns
6	SS input low to first SCLK edge	T	–	ns
7	SS input pulse width	T	–	ns

1. T = CSPI system clock period (PERCLK2).
2. Tsclk = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

3.11 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *i.MX Reference Manual*.

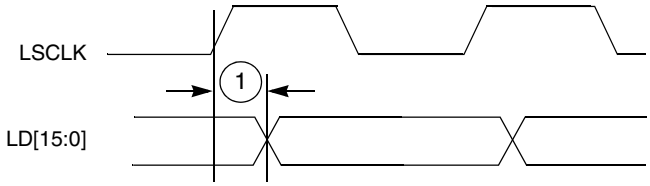


Figure 43. SCLK to LD Timing Diagram

Table 23. LCDC SCLK Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	SCLK to LD valid	–	2	ns

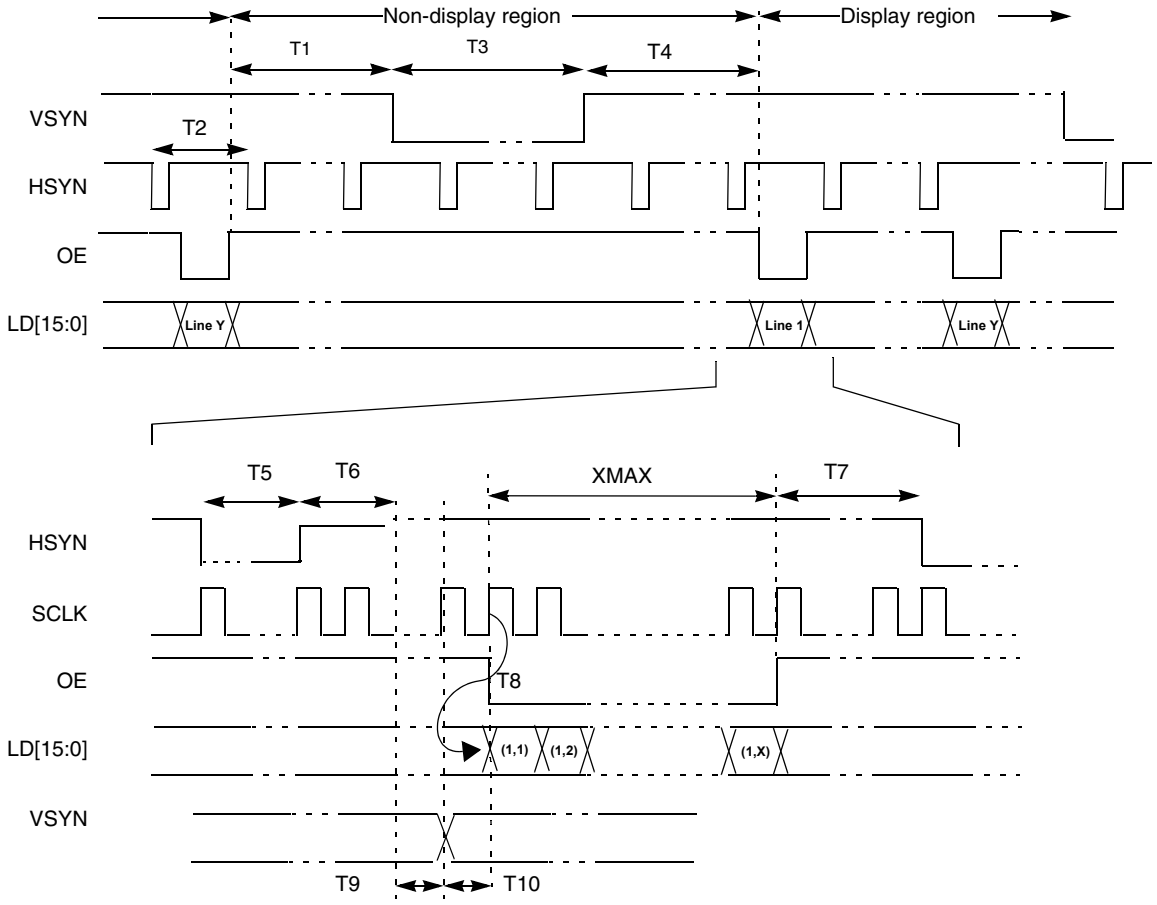


Figure 44. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Table 24. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Corresponding Register Value	Unit
T1	End of OE to beginning of VSYN	T5+T6 +T7+T9	(VWAIT1·T2)+T5+T6+T7+T9	Ts
T2	HSYN period	XMAX+5	XMAX+T5+T6+T7+T9+T10	Ts
T3	VSYN pulse width	T2	VWIDTH·(T2)	Ts
T4	End of VSYN to beginning of OE	2	VWAIT2·(T2)	Ts
T5	HSYN pulse width	1	HWIDTH+1	Ts
T6	End of HSYN to beginning to T9	1	HWAIT2+1	Ts
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts
T8	SCLK to valid LD data	-3	3	ns
T9	End of HSYN idle2 to VSYN edge (for non-display region)	2	2	Ts
T9	End of HSYN idle2 to VSYN edge (for Display region)	1	1	Ts

Table 24. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing (Continued)

Symbol	Description	Minimum	Corresponding Register Value	Unit
T10	VSYN to OE active (Sharp = 0) when VWAIT2 = 0	1	1	Ts
T10	VSYN to OE active (Sharp = 1) when VWAIT2 = 0	2	2	Ts

Note:

- Ts is the SCLK period which equals LCDC_CLK / (PCD + 1). Normally LCDC_CLK = 15ns.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 44, all 3 signals are active low.
- The polarity of SCLK and LD[15:0] can also be programmed.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 44, SCLK is always active.
- For T9 non-display region, VSYN is non-active. It is used as an reference.
- XMAX is defined in pixels.

3.12 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 45 and the parameters are listed in Table 25.

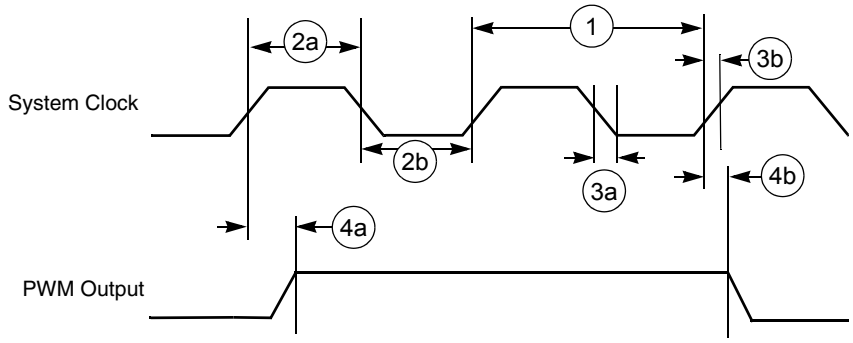


Figure 45. PWM Output Timing Diagram

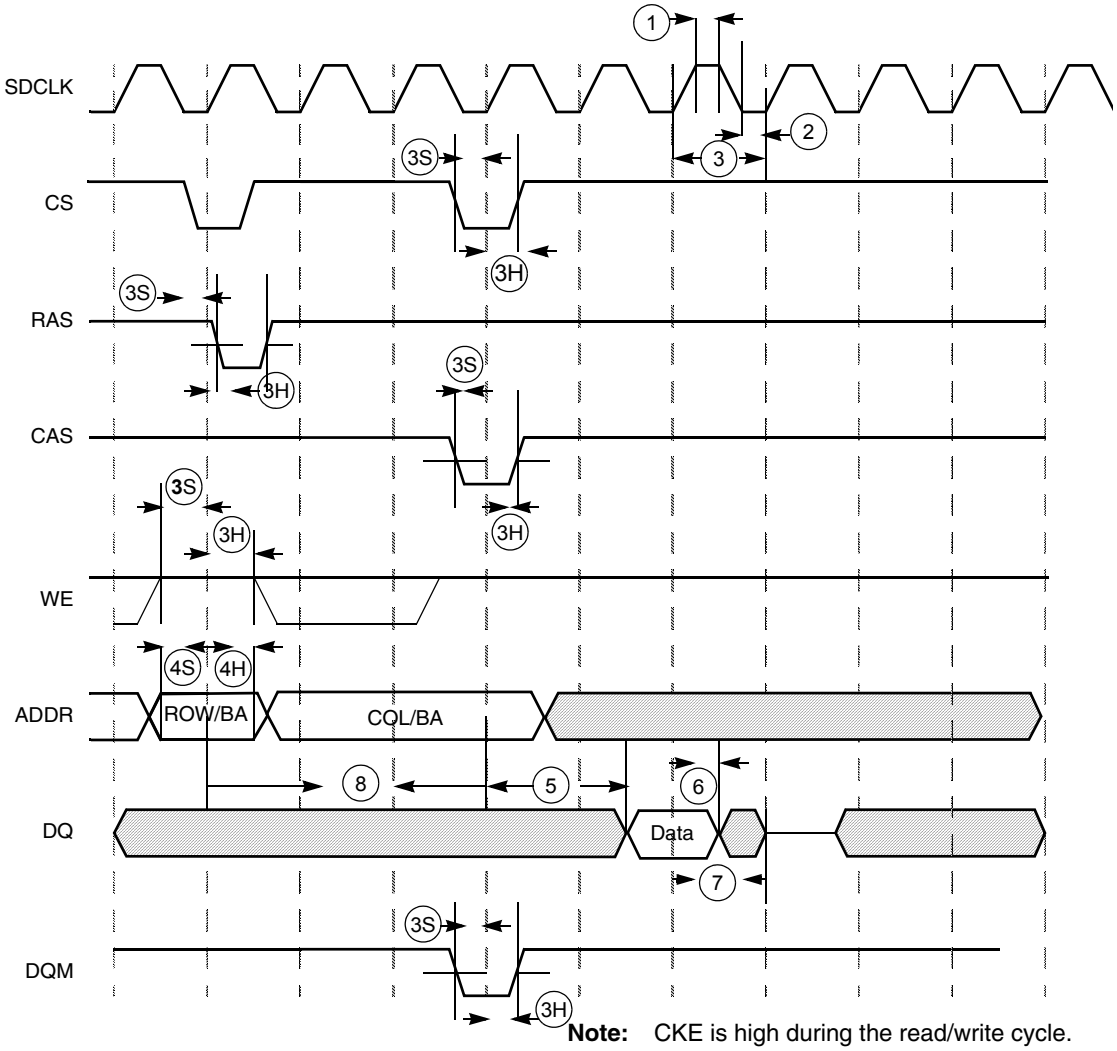
Table 25. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	87	0	100	MHz
2a	Clock high time[1]	3.3	–	5/10	–	ns
2b	Clock low time[1]	7.5	–	5/10	–	ns
3a	Clock fall time[1]	–	5	–	5/10	ns
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

1. C_L of PWMO = 30 pF

3.13 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.



Note: CKE is high during the read/write cycle.

Figure 46. SDRAM Read Cycle Timing Diagram

Table 26. SDRAM Read Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	–	2	–	ns

Table 26. SDRAM Read Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
4S	Address setup time	3.42	–	3	–	ns
4H	Address hold time	2.28	–	2	–	ns
5	SDRAM access time (CL = 3)	–	6.84	–	6	ns
5	SDRAM access time (CL = 2)	–	6.84	–	6	ns
5	SDRAM access time (CL = 1)	–	22	–	22	ns
6	Data out hold time	2.85	–	2.5	–	ns
7	Data out high-impedance time (CL = 3)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 2)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 1)	–	22	–	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}[1]	–	t_{RCD}[1]	–	ns

1. t_{RCD} = SDRAM clock cycle time. This settings can be found in the *i.MX reference manual*.

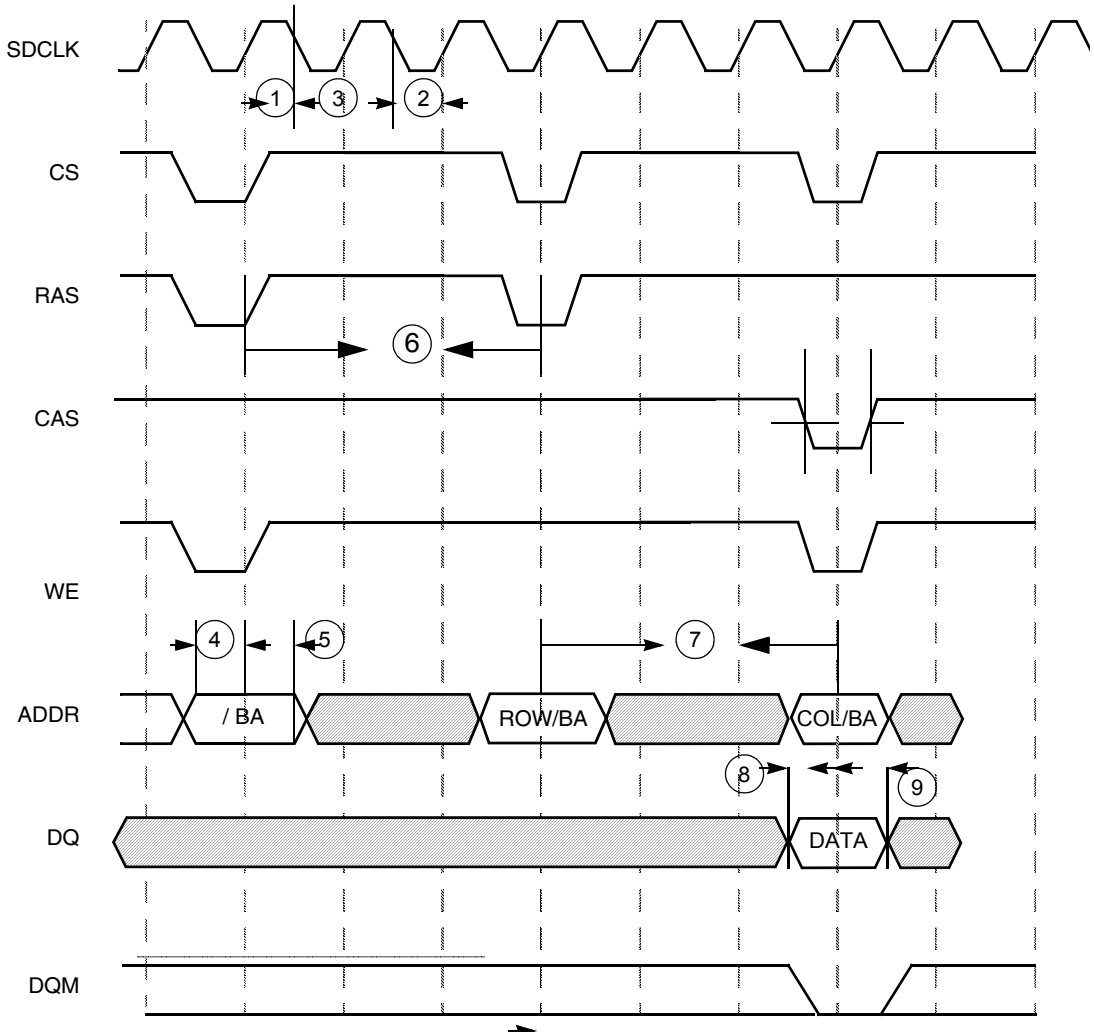


Figure 47. SDRAM Write Cycle Timing Diagram

Table 27. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP}[2]	–	ns
7	Active to read/write command delay	t_{RCD}[2]	–	t_{RCD}[2]	–	ns

Table 27. SDRAM Write Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
8	Data setup time	4.0	–	2	–	ns
9	Data hold time	2.28	–	2	–	ns

1. Precharge cycle timing is included in the write timing diagram.
2. t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the *i.MX reference manual*.

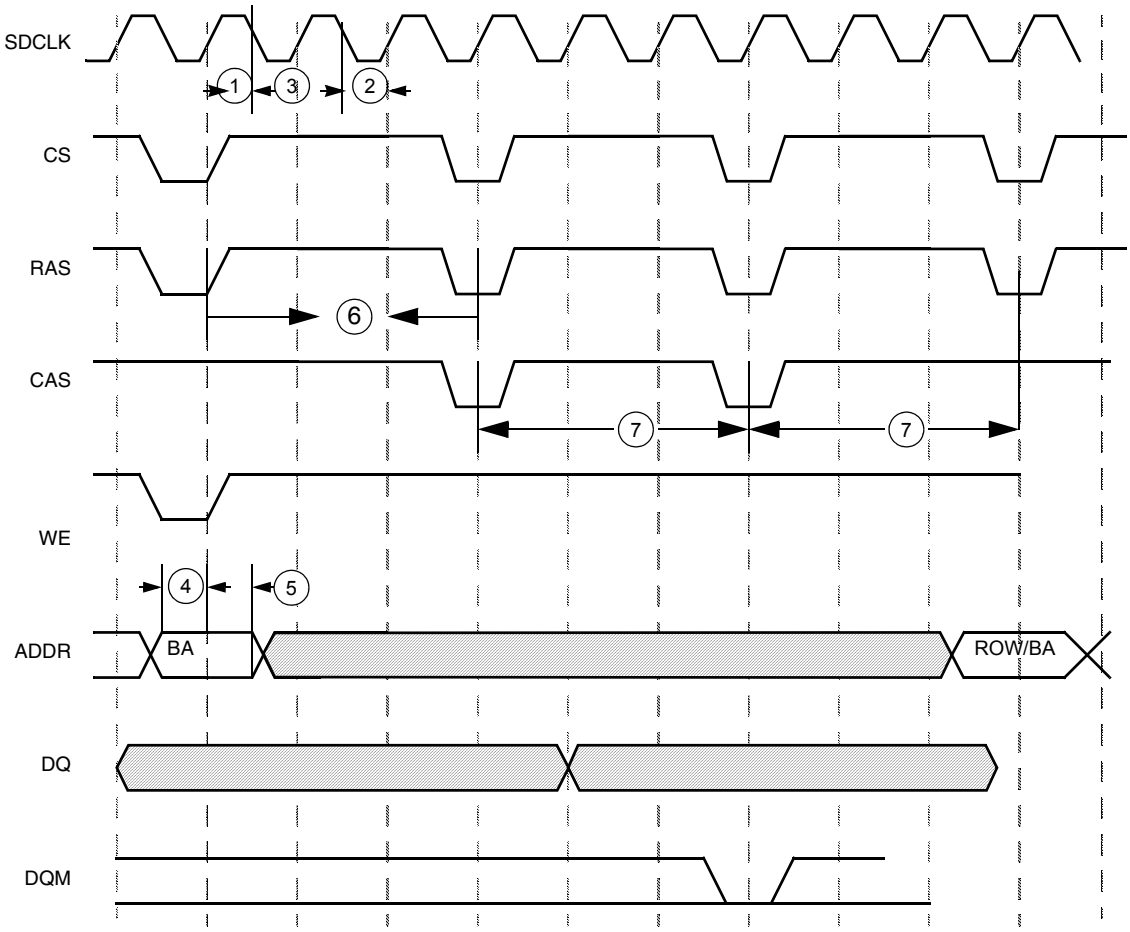


Figure 48. SDRAM Refresh Timing Diagram

Table 28. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	$\overline{\text{SDRAM clock low-level width}}$	6	–	4	–	ns

Table 28. SDRAM Refresh Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP}[1]	–	ns
7	Auto precharge command period	t_{RC}[1]	–	t_{RC}[1]	–	ns

1. t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *i.MX reference manual*.

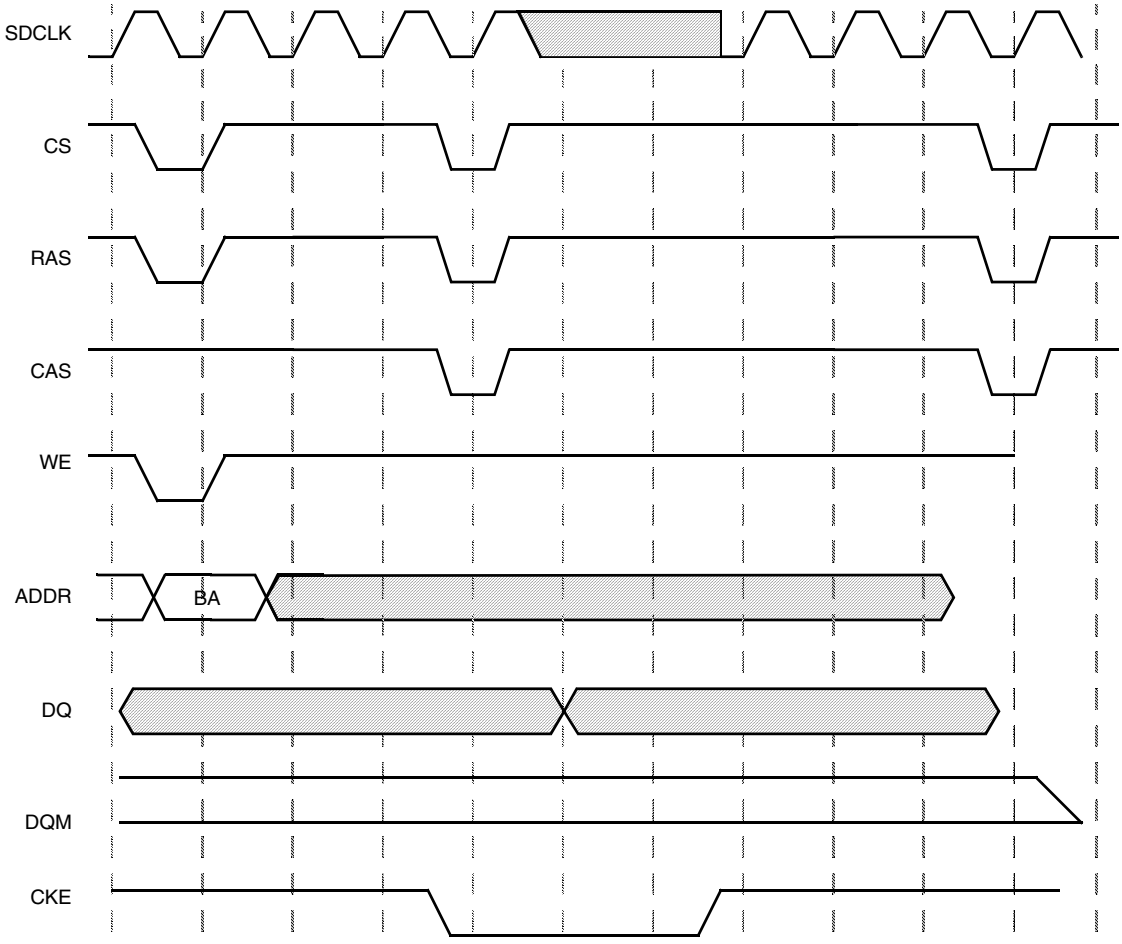


Figure 49. SDRAM Self-Refresh Cycle Timing Diagram

3.14 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

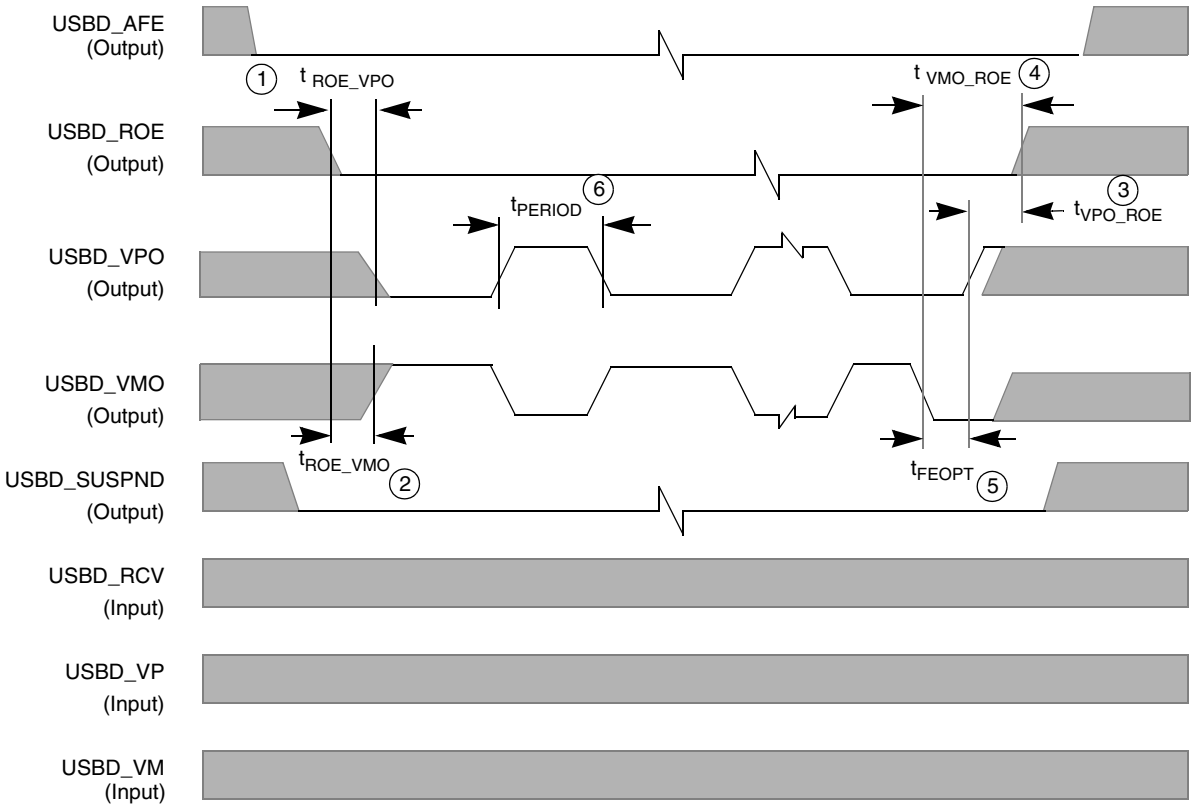


Figure 50. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 29. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{ROE_VPO}; USBD_ROE active to USBD_VPO low	83.14	83.47	ns
2	t_{ROE_VMO}; USBD_ROE active to USBD_VMO high	81.55	81.98	ns
3	t_{VPO_ROE}; USBD_VPO high to USBD_ROE deactivated	83.54	83.80	ns
4	t_{VMO_ROE}; USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.90	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160.00	175.00	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

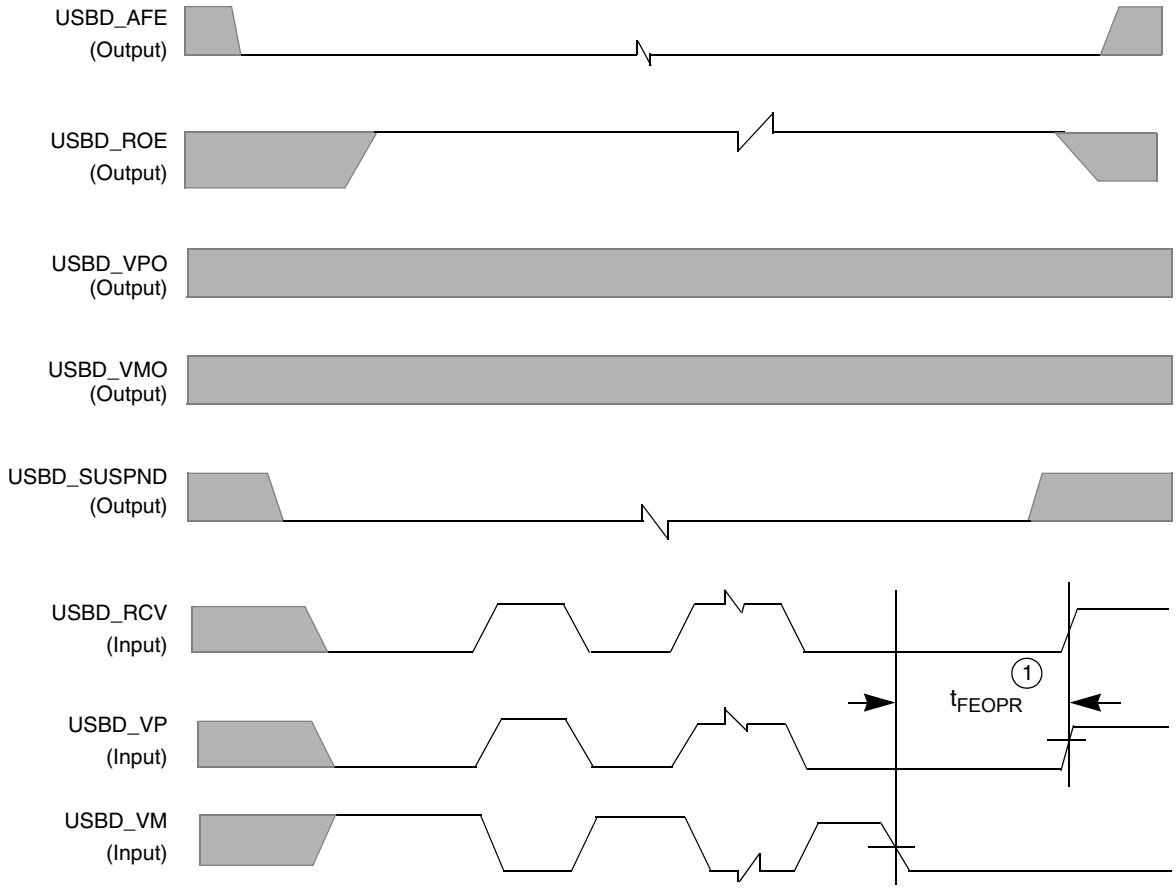


Figure 51. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 30. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	–	ns

3.15 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

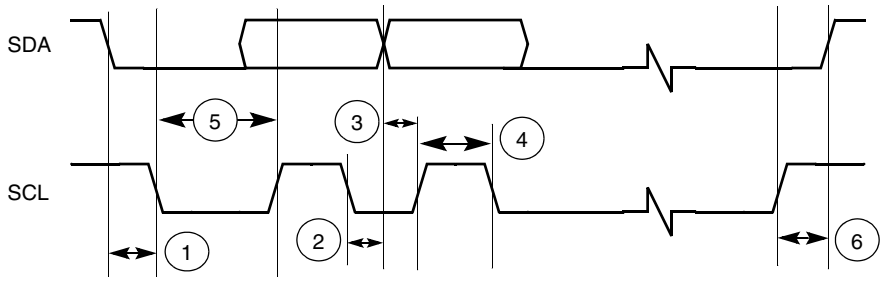


Figure 52. Definition of Bus Timing for I²C

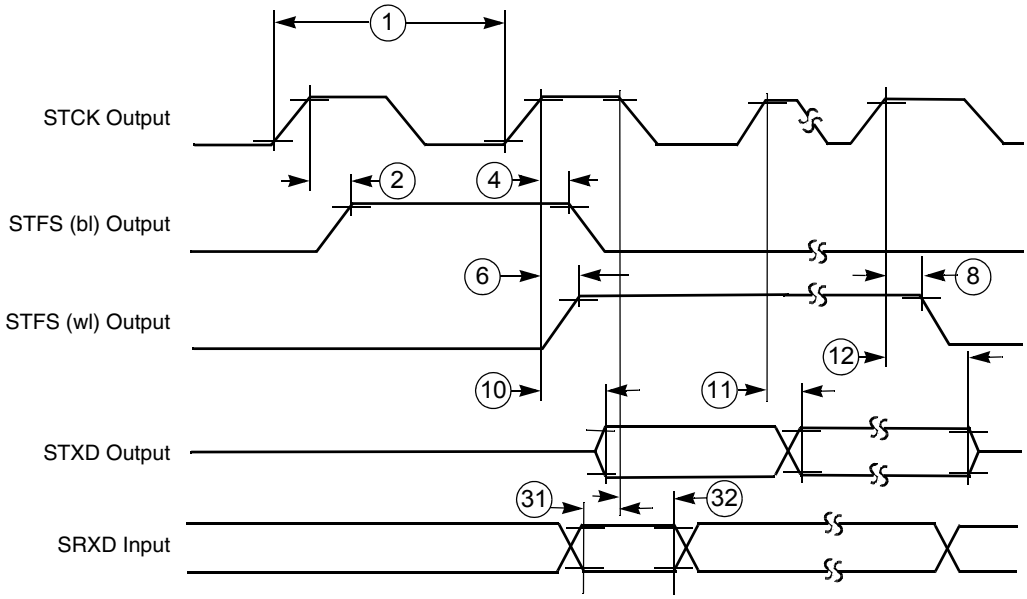
Table 31. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	–	160	–	ns
2	$\overline{\text{Data hold time}}$	0	171	0	150	ns
3	Data setup time	11.4	–	10	–	ns
4	HIGH period of the SCL clock	80	–	120	–	ns
5	LOW period of the SCL clock	480	–	320	–	ns
6	Setup time for STOP condition	182.4	–	160	–	ns

3.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 54 through Figure 56 on page 65.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 53. SSI Transmitter Internal Clock Timing Diagram

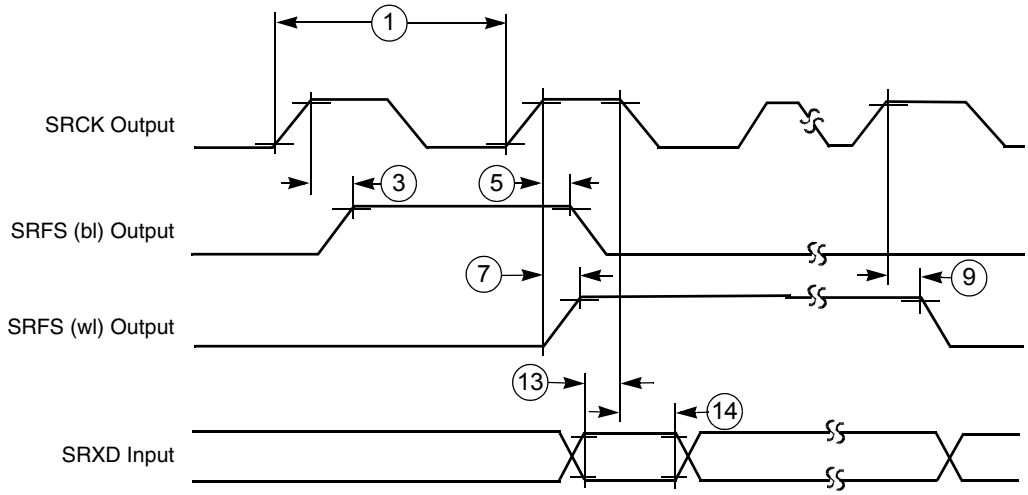
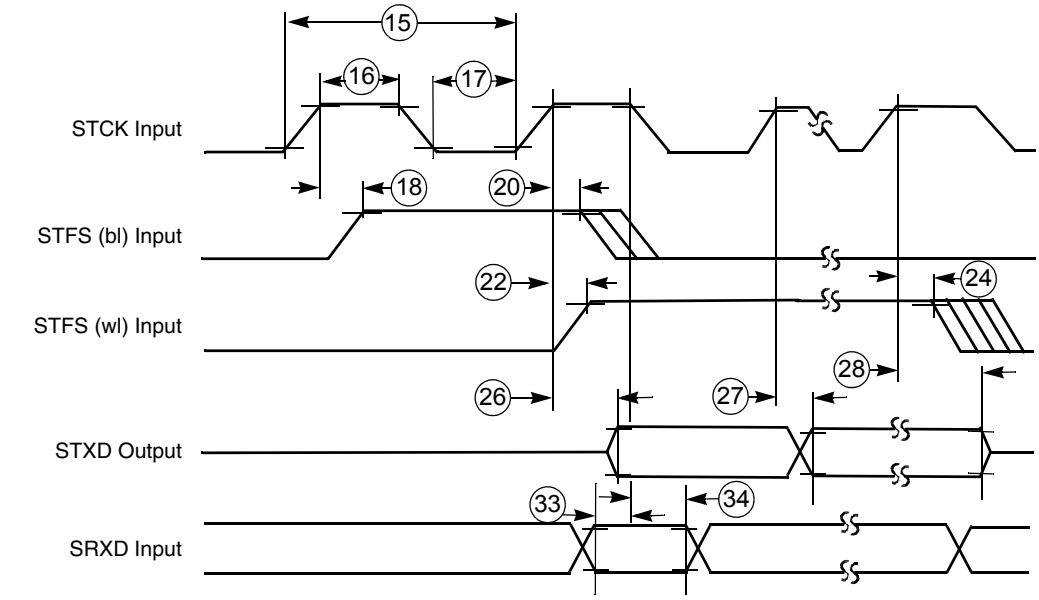


Figure 54. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 55. SSI Transmitter External Clock Timing Diagram

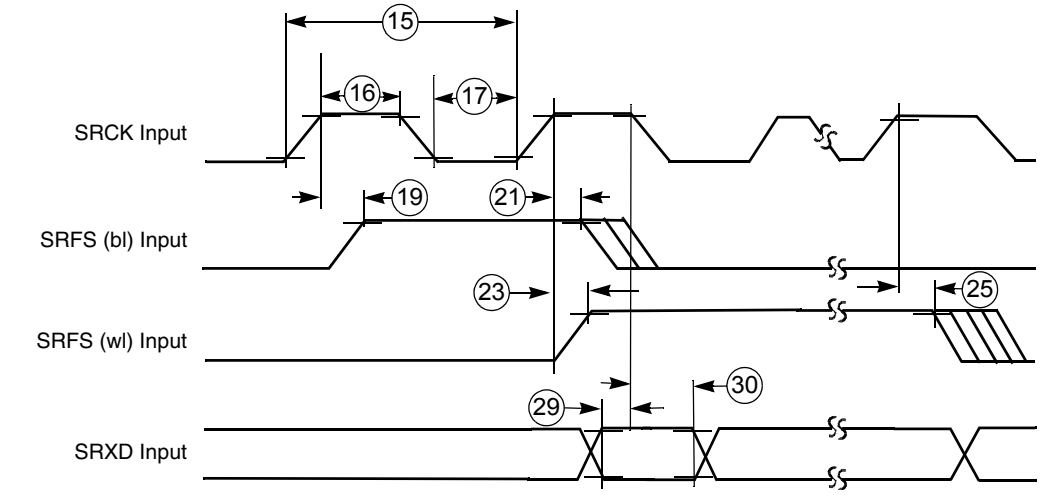


Figure 56. SSI Receiver External Clock Timing Diagram

Table 32. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	-1.1	-1.5	ns

Table 32. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
4	STCK high to STFS (bl) low[3]	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns

Table 32. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Synchronous External Clock Operation (Port C Primary Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length.

Table 33. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns

Table 33. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hold time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port B Alternate Function[2])						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port B Alternate Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length.

4 Pin-Out and Package Information

Table 34 illustrates the package pin assignments for the 225-contact PBGA package.

Table 34. i.MX 225 PBGA Pin Assignments

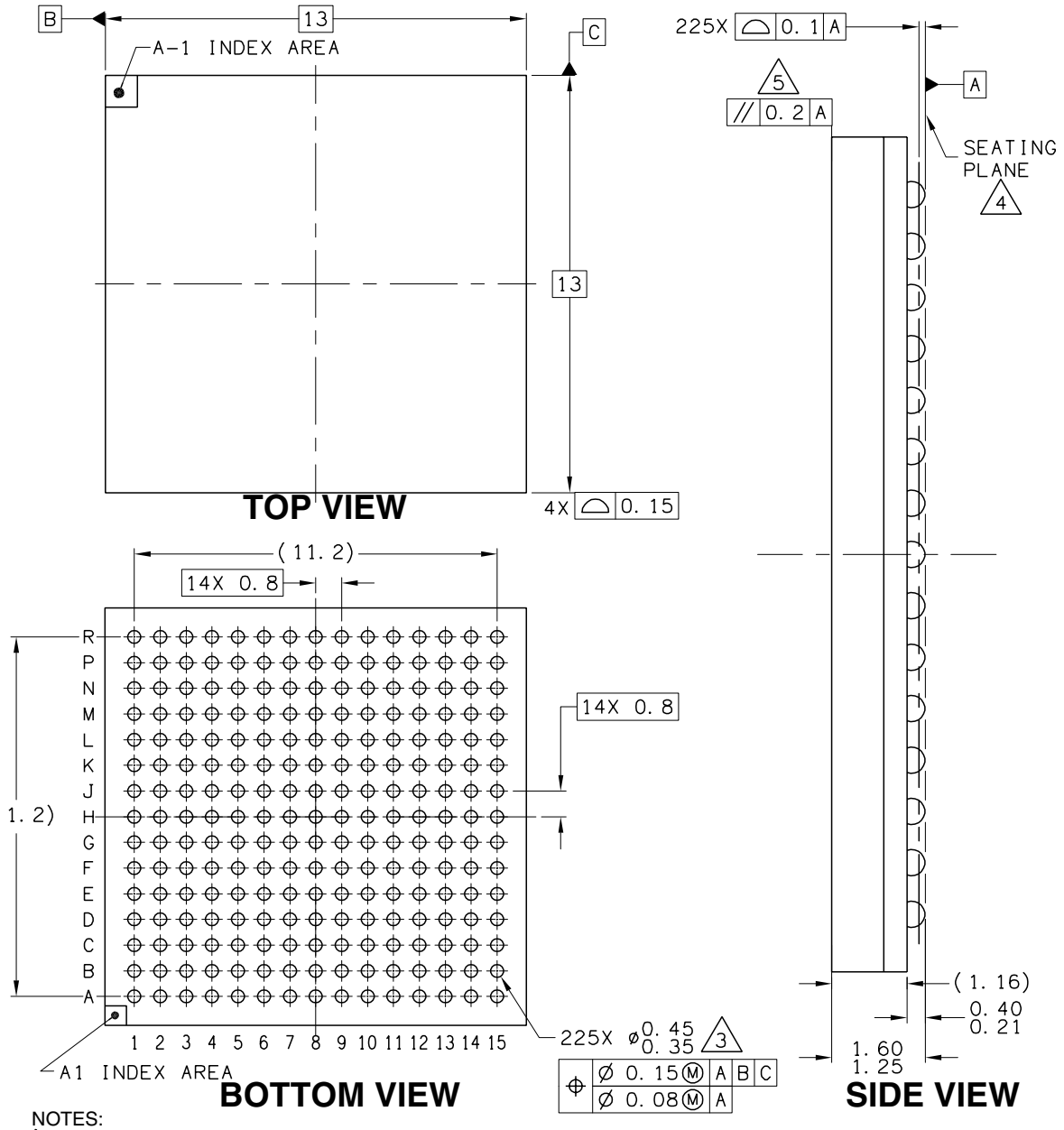
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PB13	SSI1_ RXCLK	SSI1_ TXCLK	USBD_ ROE	USBD_ SUSPND	USBD_VM	SSI0_ RXFS	SSI0_ TXCLK	SPI1_RDY	SPI1_ SCLK	REV	PS	LD2	LD4	LD5
B	PB11	PB12	SSI1_ RXDAT	USBD_ AFE	USBD_ RCV	USBD_ VMO	SSI0_ RXDAT	UART1_ TXD	SPI1_SS	LSCLK	SPL_ SPR	LD0	LD3	LD6	LD7
C	D31	PB8	SSI1_ RXFS	SSI1_ TXFS	PB10	USBD_ VPO	UART2_ RXD	SSI0_ TXFS	UART1_ RTS	CONTRAST	VSYNC	LD8	LD9	LD12	NVDD2
D	A23	A24	PB9	SSI1_ TXDAT	NVDD1	USBD_ VP	QVDD4	UART2_ TXD	NVDD3	SPI1_ MOSI	HSYNC	LD1	LD11	TOUT2	LD13
E	A21	A22	D30	D29	NVDD1	QVSS	UART2_ RTS	UART1_ RXD	UART1_ CTS	SPI1_ MISO	OE_ ACD	LD10	TIN	PA4	PA3
F	A20	A19	D28	D27	NVDD1	NVDD1	UART2_ CTS	SSI0_ RXCLK	SSI0_ TXDAT	CLS	QVDD3	LD14	LD15	PA6	PA8
G	A17	A18	D26	D25	NVDD1	NVSS	NVDD4	NVSS	NVSS	QVSS	PWMO	PA7	PA11	PA13	PA9
H	A15	A16	D23	D24	D22	NVSS	NVSS	NVSS	NVSS	NVDD2	PA5	PA12	PA14	I2C_DATA	TMS
J	A14	A12	D21	D20	NVDD1	NVSS	NVSS	QVDD1	NVSS	PA10	I2C_ CLK	TCK	$\overline{\text{TDO}}$	BOOT1	BOOT0
K	A13	A11	$\overline{\text{CS2}}$	D19	NVDD1	NVSS	QVSS	NVDD1	NVSS	D1	BOOT2	TDI	BIG_ ENDIAN	$\overline{\text{RESET\_OUT}}$	XTAL32K
L	A10	A9	D17	D18	NVDD1	NVDD1	$\overline{\text{CS5}}$	D2	$\overline{\text{ECB}}$	NVSS	NVSS	POR	QVSS	XTAL16M	EXTAL32K
M	D16	D15	D13	D10	$\overline{\text{EB3}}$	NVDD1	$\overline{\text{CS4}}$	$\overline{\text{CS1}}$	BCLK[1]	$\overline{\text{RW}}$	NVSS	BOOT3	QVDD2	$\overline{\text{RESET\_IN}}$	EXTAL16M
N	A8	A7	D12	$\overline{\text{EB0}}$	D9	D8	$\overline{\text{CS3}}$	$\overline{\text{CS0}}$	PA17	D0	DQM2	DQM0	SDCKE0	TRISTATE	$\overline{\text{TRST}}$
P	D14	A5	A4	A3	A2	A1	D6	D5	MA10	MA11	DQM1	$\overline{\text{RAS}}$	SDCKE1	CLKO	$\overline{\text{RESETSF}}$[2]
R	A6	D11	$\overline{\text{EB1}}$	$\overline{\text{EB2}}$	$\overline{\text{OE}}$	D7	A0	SDCLK[2]	D4	$\overline{\text{LBA}}$	D3	DQM3	$\overline{\text{CAS}}$	$\overline{\text{SDWE}}$	AVDD1

1. Burst Clock
2. These signals are not used on the MC9328MXS and should be floated in an actual application.

4.1 PBGA 225 Package Dimensions

Figure 57 illustrates the 225 PBGA 13 mm × 13 mm package.

Case Outline 1304B



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 57. i.MX Processor's 225 PBGA Mechanical Drawing

NOTES

How to Reach Us:

USA/Europe/Locations Not Listed:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

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2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

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Rev. 0
1/2005