Safe Operating Area Testing Without A Heat Sink

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Introduction

Most manufacturers of PowerMOS transistors specify the **S**afe **O**perating **A**rea for their devices at 25^{O}C case temperature and derate them linearly to zero at the maximum rated junction temperature. The circuits to maintain a fixed current and voltage on the **D**evice **U**nder **T**est are easy to devise[1], but it is impractical to keep the case temperature at 25^{O}C. The problem is that the uncontrolled heat sink begins to rise in temperature, heated by the DUT, making it impossible to maintain a controlled reference point temperature[2]. This note explains a test method which does not use a heat sink on the DUT but depends upon the thermal capacitance (C_T) of the package to allow prediction of the case temperature during SOA testing.

Determining the Thermal Capacitance of a Modern PowerMOS Transistor Package

Most power transistor packages today consist of a copper header or base plate and copper leads fastened together with epoxy plastic which also covers the active transistor die. When the package is not mounted to a heat sink, the thermal resistance across the header and leads is small compared to the thermal resistance external to the header, so the package is essentially an isotherm. Since the package is an isotherm, it can be represented accurately as a “lumped” thermal capacitance in the familiar electrical analogue for the thermal circuit. The estimation of the value of that capacitance is simplified because the thermal capacitance or specific heat of most epoxy plastics is small compared to that of copper. The plastic portion of the package can be removed easily by crushing it with an ordinary set of pliers. Weighing the remaining portion of the package will give a good estimate of the amount of copper contained in the package. The weight of the silicon die is usually negligible. Multiplying the weight of the copper by the thermal capacitance of copper (0.385J/g^{O}C [3] was used in the rest of this note) will give a good estimate of the thermal capacitance of the package. See Table 1.

Applying the Package Thermal Capacitance to SOA Testing

The problem in testing SOA on a transistor without heat sinking it is that the case temperature increases during the test. Heat flows from the silicon die into the copper of the package at a very predictable rate since constant power circuits are usually used in SOA testing. There is also heat flow from the package to the ambient which is proportional to the temperature difference between the package and the ambient. The thermal resistance of the package to ambient air (θ_{CA}) is usually quite high and if the temperature difference between the package and the air is kept small (Usually by doing a short test) the heat flow out can be neglected. However, SOA testing should be done in a draft free ambient to avoid undertesting the DUT. See Table 2.

TABLE 1. SOME THERMAL CAPACITANCE ESTIMATES FOR FAIRCHILD POWER TRANSISTOR PACKAGES DEVELOPED BY THIS TECHNIQUE

PACKAGE	WEIGHT OF COPPER (g)	THERMAL CAPACITANCE C_T (J/^{O}C)
TO-247	4.07	1.57
TO-218	3.50	1.35
TO-220	1.40	0.54
TO-251	0.32	0.12
4 Lead DIP	0.27	0.10

NOTE: These values were determined in August 1993 on Fairchild parts. Do not use them on other manufacturers’ parts or even on Fairchild parts manufactured at a later date without verifying them

TABLE 2.

PACKAGE	MAXIMUM θ_{JA} THERMAL RESISTANCES
TO-247	30 ^{O}C/W
TO-218	30^{O}C/W
TO-220	80^{O}C/W
TO-251	100^{O}C/W
Hex DIP	115^{O}C/W

NOTE: These maximum values are published to keep customers from damaging transistors when they use them in free air and are very conservative. Actual values for thermal resistance to air may be half these values. Indeed in the calculation of thermal time constants for packages below, half the thermal resistance values listed above was used.

If the heat flow out from the DUT can be ignored, the increase in temperature of the case due to SOA testing is simply the input energy divided by the thermal capacitance of the package. The internal parts of a PowerMOS transistor have thermal resistances and thermal capacitances associated with them also. The thermal time constants of these internal parts are usually quite short, in the order of 1ms to 10ms. SOA testing should be done at times relatively long compared to the internal time constants of the transistor, but short compared to the thermal time constant of the package to ambient thermal circuit. Table 3 is a list of the thermal time constants for the Fairchild packages listed previously, using half the maximum free air thermal resistance value listed previously.

TABLE 3.

PACKAGE	θ_{CA} FREE AIR THERMAL RESISTANCE ($^oC/W$)	C_T THERMAL CAPACITANCE ($J/^oC$)	THERMAL TIME CONSTANT (s)
TO-247	15	1.57	23.6
TO-218	15	1.35	20.3
TO-220	40	0.54	21.6
TO-251	50	0.12	6.0
4 Pin Hex DIP	58	0.10	5.8

If we arbitrarily use a ratio of 10 to 1 from both the internal time constants and the package to air time constant, the time range over which satisfactory measurements can be made is 100ms to 580ms.

However, the earlier assumption that the case temperature should not be very far above ambient, so we can assume no heat out flow from the package, would encourage us to use the shorter time. A few examples will illustrate the technique and let us check our assumptions.

Examples of Free Air SOA Tests to Verify SOA Capability

Techniques

In the examples to follow, the rise in case temperature will initially be estimated at 20^oC and an SOA (Constant Power) pulse equal to the rated SOA capability at 45^oC at 100ms will be applied to the transistor. No heat sink will be attached to the unit. The SOA used in these calculations was the DC SOA, the calculation would be slightly more accurate if the SOA were increased slightly to account for the difference in capability from DC to 100ms. The actual case temperature rise will then be calculated and the SOA capability recomputed. This will be iterated until the difference between the estimated case temperature and the final case temperature is less than 1^oC. This will define a test suitable for that transistor. This approach to solving the problem, successive approximation, may be carried to the accuracy required. The problem can be solved exactly as shown in Appendix A.

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First Iteration:

Estimated Rise in $T_{CASE} = 20^oC$, $T_{CASE} = 45^oC$

SOA Capability at $45^oC = P_D \bullet (T_{JMAx} - 45)/(T_{JMAX} - 25)$

SOA Capability at $45^oC = 150 \bullet (175 - 45)/(175-25)$

SOA Capability at $45^oC = 130W$

SOA Energy = SOA Power • Time

SOA Energy = 130 • 0.1

SOA Energy = 13.0J

Case Temperature Rise = SOA Energy/C_T

Case Temperature Rise = 13.0/0.54

(C_T for TO-220 from Table 3)

Case Temperature Rise = 24.1^oC

Second Iteration:

Estimated Rise in $T_{CASE} = 24.1^oC$, $T_{CASE} = 49.1^oC$

SOA Capability at $49.1^oC = 150 \bullet (175 - 49.1)/(175 - 25)$

SOA Capability at $49.1^oC = 125.9W$

SOA Energy = 125.9 • 0.1

SOA Energy = 12.59J

Case Temperature Rise = 12.59/0.54

Case Temperature Rise = 23.3^oC

Third Iteration:

Estimated Rise in $T_{CASE} = 23.3^oC$, $T_{CASE} = 48.3^oC$

SOA Capability at $48.3^oC = 150 \bullet (175 - 48.3)/(175 - 25)$

SOA Capability at $48.3^oC = 126.7W$

SOA Energy = 126.7 • 0.1

SOA Energy = 12.67J

Case Temperature Rise = 12.67/0.54

Case Temperature Rise = 23.5^oC

Checking our assumption that the heat flow out during test is negligible:

$T_{AVERAGE} = T_{MAX}/2$

$T_{AVERAGE} = 23.5/2$

$T_{AVERAGE} = 11.8^oC$ Rise Above Ambient

$E_{FLOW} = (T \bullet t) / \theta_{CA}$

$E_{FLOW} = (11.8 \bullet 0.1) /40$ (Using 1/2 the θ_{CA} Listed in Table 2)

$E_{FLOW} = 0.03J$

$\Delta T = E_{FLOW} / C_T$

$\Delta T = 0.03 /0.54$ (C_T from Table 3)

$\Delta T = 0.055^oC$ Temperature Change Due to Heat Flow Out During Test, Obviously Negligible

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First Iteration:

Estimated Rise in $T_{CASE} = 20^oC$, $T_{CASE} = 45.0^oC$

SOA Capability at $45^oC = P_D \bullet (T_{JMAX} - 45)/(T_{JMAX} - 25)$

SOA Capability at $45^oC = 53 \bullet (175 - 45)/(175 - 25)$

SOA Capability at $45^oC = 47.7W$

SOA Energy = SOA Power • Time

SOA Energy = 47.7 • 0.1

SOA Energy = 4.77J

Case Temperature Rise = SOA Energy/C_T

Case Temperature Rise = 4.77/0.12 (C_T for TO-251 from Table 3)

Case Temperature Rise = $39.75\ ^oC$

Second Iteration:

Estimated Rise in T_{CASE} = 39.75°C, T_{CASE} = 64.75°C

SOA Capability at 64.75°C = 53 • (175 - 64.75)/(175 - 25)

SOA Capability at 64.75°C = 38.96W

SOA Energy = 38.96 • 0.1

SOA Energy = 3.90J

Case Temperature Rise = 3.90/0.12

Case Temperature Rise = 32.46°C

Third Iteration:

Estimated Rise in T_{CASE} = 32.5°C, T_{CASE} = 57.5°C

SOA Capability at 57.5°C = 53 • (175 - 57.5)/(175 - 25)

SOA Capability at 57.5°C = 41.53W

SOA Energy = 41.53 • 0.1

SOA Energy = 4.15J

Case Temperature Rise = 4.15/0.12

Case Temperature Rise = 34.6°C

Fourth Iteration:

Estimated Rise in T_{CASE} = 34.6°C, T_{CASE} = 59.6°C

SOA Capability at 59.6°C = 53 • (175 - 59.6)/(175 - 25)

SOA Capability at 49.1°C = 40.77W

SOA Energy = 40.77 • 0.1

SOA Energy = 4.77J

Case Temperature Rise = 4.08/0.12

Case Temperature Rise = 34.0°C

Checking our assumption that the heat flow out during test is negligible:

$T_{AVERAGE} = T_{MAX}/2$

$T_{AVERAGE}$ = 34.3/2

$T_{AVERAGE}$ = 17.2°C Rise Above Ambient

$E_{FLOW} = (T \bullet t)/\theta_{CA}$

E_{FLOW} = (17.2 • 0.1) / 25 (Using 1/2 the θ_{CA} Listed in Table 2)

E_{FLOW} = 0.034J

$\Delta T = E_{FLOW} / C_T$

ΔT = 0.034 /0.12 (C_T from Chart Above)

ΔT = 0.29°C Temperature Change Due to Heat Flow Out During Test, Obviously Negligible

Conclusions

This is a simple, effective way to verify SOA capability of PowerMOS transistors. It can be applied to almost any transistor available on the market today.

References

[1] Samuel J. Passaflume and William J. Nicholas, “Determining a MOSFET's Real FBSOA, Powertechnics Magazine, June 1989.

[2] David L. Blackburn, “A Review of Thermal Characterization of Power Transistors”, Semi-Therm, February 1988

[3] CRC Handbook of Chemistry and Physics, 59th edition, pages F-316 and D-21.

Appendix A

Exact Solution For SOA Test Pulse

W Width of SOA Test Pulse in Seconds

P_T SOA Test Level in Watts

P_R SOA Rating at Pulse Width in Watts

C_T Thermal Capacitance of Package in J/°C

ΔT_C Change in Case Temperature Due to Test Pulse

T_{JMAX} Maximum Rated Junction Temperature

Assuming the test starts at 25°C:

$$\frac{P_T}{P_R} = \frac{T_{JMAX} - (\Delta T_C + 25)}{T_{JMAX} - 25} \quad \text{(EQ. 1)}$$

$$\Delta T_C = \frac{W \times P_T}{C_T} \quad \text{(EQ. 2)}$$

$$\frac{P_T}{P_R} = \frac{T_{JMAX} - \left(\frac{W \times P_T}{C_T}\right) - 25}{T_{JMAX} - 25} \quad \text{(EQ. 3)}$$

$$\frac{P_T}{P_R} = \frac{C_T \times T_{JMAX} - W \times P_T - C_T \times 25}{C_T \times (T_{JMAX} - 25)} \quad \text{(EQ. 4)}$$

$$P_T \times \left\{\frac{1}{P_R} + \frac{W}{C_T \times (T_{JMAX} - 25)}\right\} = \frac{T_{JMAX} - 25}{T_{JMAX} - 25} = 1 \quad \text{(EQ. 5)}$$

$$P_T = \frac{P_R \times C_T \times (T_{JMAX} - 25)}{C_T \times (T_{JMAX} - 25) + W \times P_R} \quad \text{(EQ. 6)}$$

Exact SOA Test Condition Calculations

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Inputs:

Pulse Width (W) = 100ms

SOA Rating at 100ms (P_R) = 150W

Thermal Capacitance (C_T) = 0.54J/°C

Maximum Junction Temperature (T_{JMAX}) = 175°C

Outputs:

P_T = 126.6W (Equation 6)

Delta T_{CASE} (ΔT_C) = 23.4°C (Equation 2)

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Inputs:

Pulse Width (W) = 100ms

SOA Rating at 100ms (P_R) = 53W

Thermal Capacitance (C_T) = 0.12J/°C

Maximum Junction Temperature (T_{JMAX}) = 175°C

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