



May 2004

RMBA19500A

## RMBA19500A

### PCS1900 2 Watt GaAs MMIC Power Amplifier

#### General Description

The RMBA19500A is a highly linear Power Amplifier. The two stage circuit uses our pHEMT process. It has been designed for use as a driver stage for PCS1900 base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for PCS operation.

#### Features

- 2 Watt linear output power at 36 dBc ACPR1 for CDMA operation
- OIP3  $\geq$  43 dBm at 27 and 30 dBm output
- Small Signal Gain of  $> 30$  dB
- Small outline SMD package

#### Absolute Ratings

Symbol	Parameter	Ratings	Units
V <sub>d</sub>	Drain Supply Voltage <sup>1</sup>	+10	V
V <sub>g</sub>	Gate Supply Voltage (max absolute)	-5	V
P <sub>IN</sub>	RF Input Power (from 50 $\Omega$ source)	+5	dBm
T <sub>C</sub>	Operating Case Temperature Range	-30 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-40 to +100	°C

#### Electrical Characteristics<sup>2</sup>

Parameter	Min	Typ	Max	Units
Frequency Range	1930		1990	MHz
Gain (Small Signal) Over 1930–1990 MHz	30			dB
Gain Variation				
Over Frequency Range		$\pm 1.0$		dB
Over Temperature Range		$\pm 1.5$		dB
Noise Figure		6		dB
P1dB Output		30		dBm
Output Power @ CDMA <sup>3</sup>	33			dBm
PAE @ 33 dBm Pout		24		%
OIP3 <sup>4</sup>	43	45		dBm
Drain Voltage (V <sub>dd</sub> )		7.0		V
Gate Voltage (VG1, 2 and VG3) <sup>5</sup>	-2		-0.25	V
Quiescent currents (Idq1, 2 and Idq3) <sup>5</sup>		180, 445		mA
Thermal Resistance (Channel to Case) R <sub>JC</sub>		11		°C/W

#### Notes:

1. Only under quiescent conditions—no RF applied.
2. V<sub>DD</sub> = 7.0V, T<sub>C</sub> = 25°C. Part mounted on evaluation board with input and output matching to 50 $\Omega$ .
3. 9 Channel Forward Link QPSK Source; 1.23 Mbps modulation rate. CDMA ACPR1 is measured using the ratio of the average power within the 1.23 MHz channel at band center to the average power within a 30 KHz bandwidth at an 885 KHz offset. Minimum CDMA output power is met with ACPR1  $> 36$  dBc.
4. OIP3 specifications are achieved for power output levels of 27 and 30 dBm per tone with tone spacing of 1.25 MHz at band-center with adjusted supply and bias conditions of V<sub>dd</sub> = 6.5V and IdqTotal = 625mA (see Note 5).
5. VG1,2 and VG3 must be individually adjusted to achieve IDQ1,2 and IDQ3. A single VGG bias supply adjusted to achieve IDQTOTAL = 625mA can be used with nearly equivalent performance. Values for IDQ1,2 and IDQ3 shown have been optimized for CDMA operation. IDQ1, 2 and IDQ3 (or IDQTOTAL) can be adjusted to optimize the linearity of the amplifier for other modulation systems.

The device requires external input and output matching to 50 $\Omega$  as shown in Figure 3 and the Parts List.

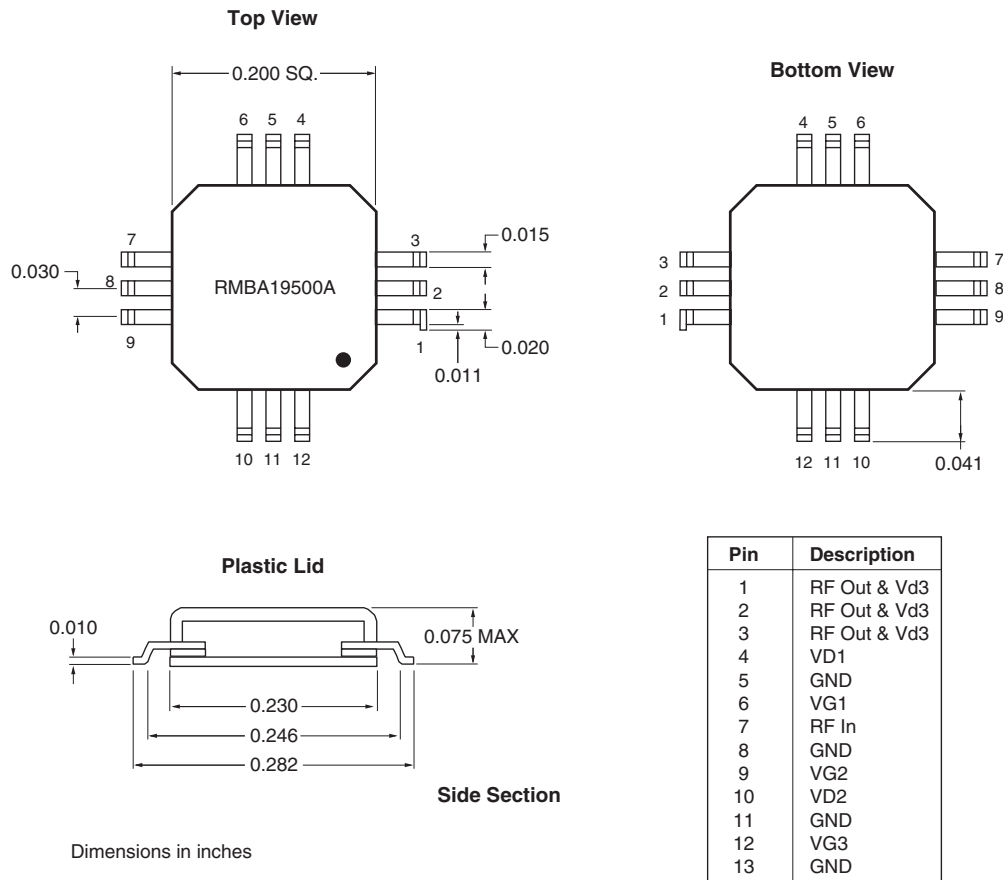
# Application Information

## CAUTION: THIS IS AN ESD SENSITIVE DEVICE

The following describes a procedure for evaluating the RMBA19500A, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for PCS1900 Base station or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. The RMBA19500A requires external passive components for DC bias and RF input and output matching circuits as shown in Figure 3 and the Parts List. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of Figure 3. The following designations should be noted:

- (1) Pin designations are as shown in Figure 2.
- (2)  $V_{g1}$ ,  $V_{g2}$ , and  $V_{g3}$  are the Gate Voltages (negative) applied at the pins of the package.
- (3)  $V_{gg1}$ , 2, and  $V_{gg3}$  are the negative supply voltages at the evaluation board terminals ( $V_{g1}$  and  $V_{g2}$  are tied together).
- (4)  $V_{d1}$ ,  $V_{d2}$ , and  $V_{d3}$  are the Drain Voltages (positive) applied at the pins of the package.
- (5)  $V_{dd}$  is the positive supply voltage at the evaluation board terminal ( $V_{d1}$ ,  $V_{d2}$ , and  $V_{d3}$  are tied together).

Note: The base of the package must be soldered on to a heat sink for proper operation.



**Figure 1. Package Outline and Pin Designations**

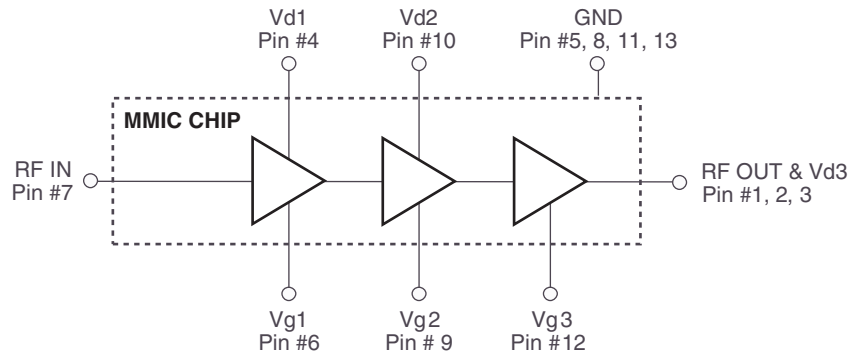


Figure 2. Functional Block Diagram

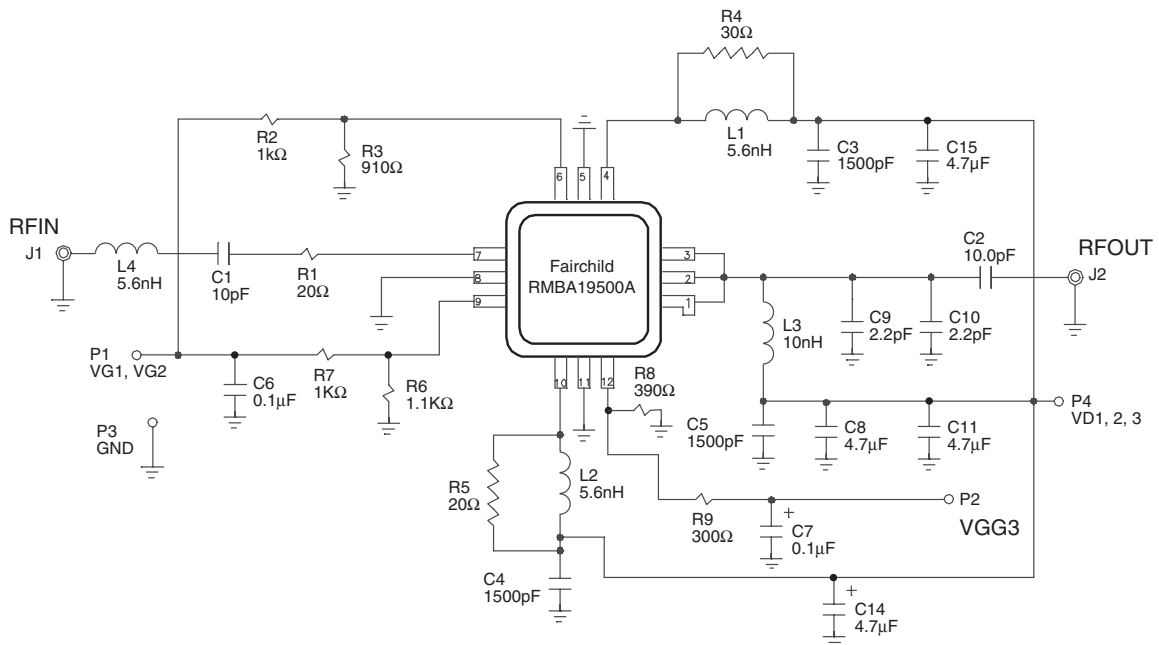


Figure 3. Schematic of Application Circuit Showing External Components

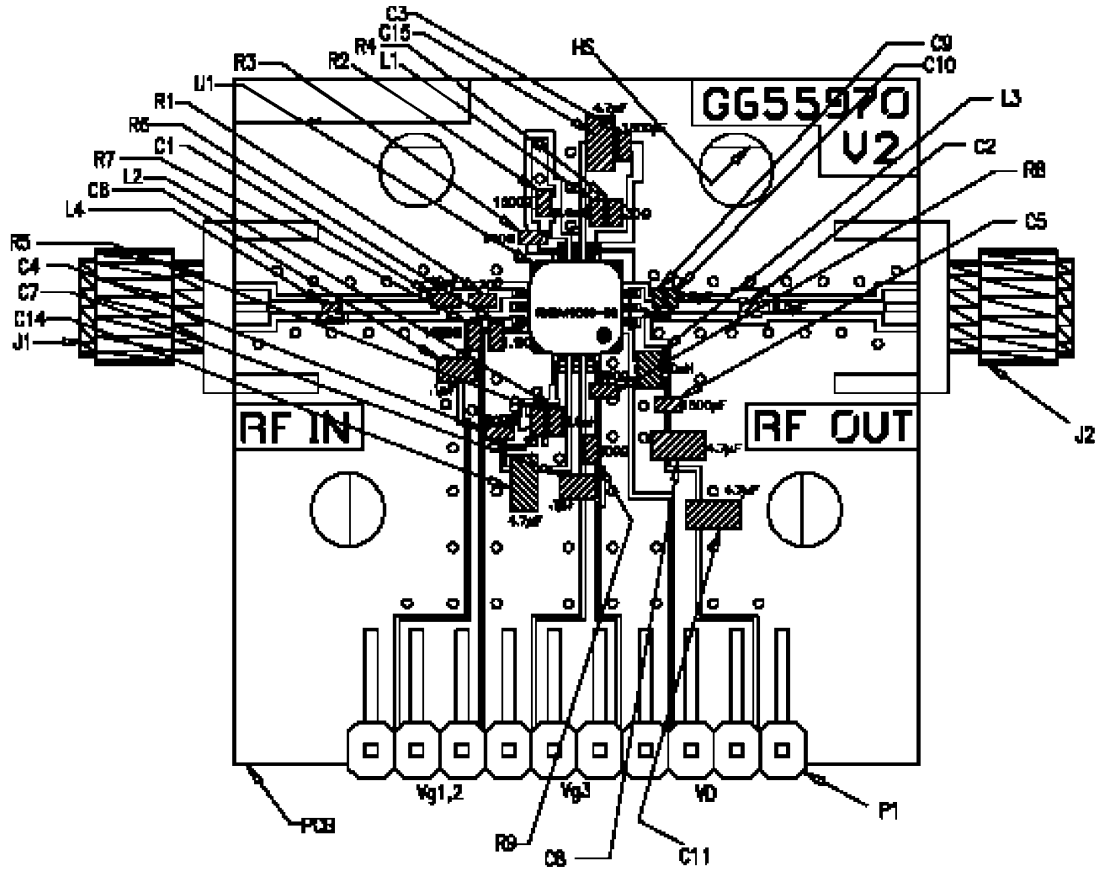


Figure 4. Layout of Test Evaluation Board (RMBA19500A-TB, G655971)

## Test Procedure for the Evaluation Board (RMBA19500A-TB)

**CAUTION: LOSS OF GATE VOLTAGES (Vg1, Vg2, Vg3) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.**

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA19500A.)

**Step 1:** Turn off RF input power.

**Step 2:** Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vg1, Vg2 and Vg3 to -4V (pinch-off).

**Step 3:** Slowly apply drain supply voltages of +7V to the board terminal Vdd ensuring that there is no short.

**Step 4:** Adjust Vg3 up from -3V until the drain current (with no RF applied) increases to Idq3 as per supplied result sheet. Then adjust Vg1, 2 until the total drain current becomes equal to the sum of Idq1, 2 and Idq3.

**Step 5:** After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

**Step 6:** Follow turn-off sequence of:

- (i) Turn off RF Input Power
- (ii) Turn down and off drain voltage Vdd.
- (iii) Turn down and off gate voltages Vg1, Vg2 and Vg3.

**Parts List for Test Evaluation Board (RMBA19500A-TB, G654188/G654942)**

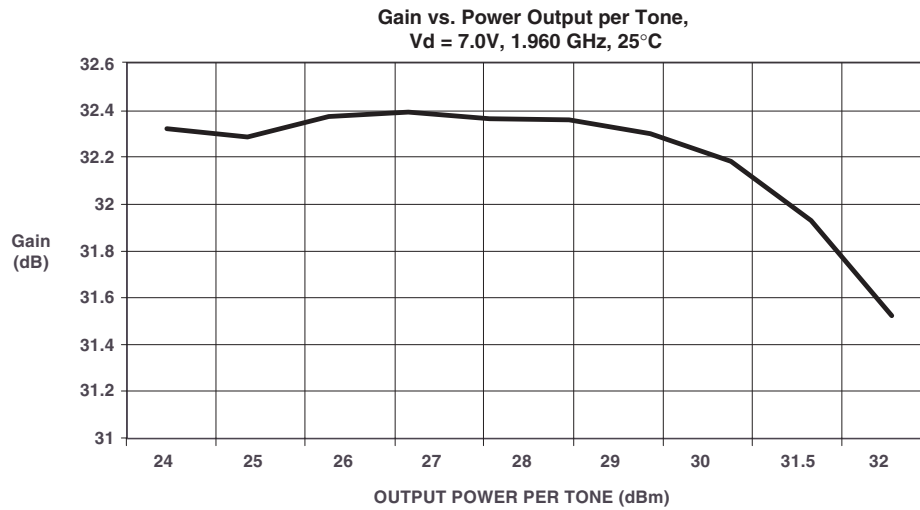
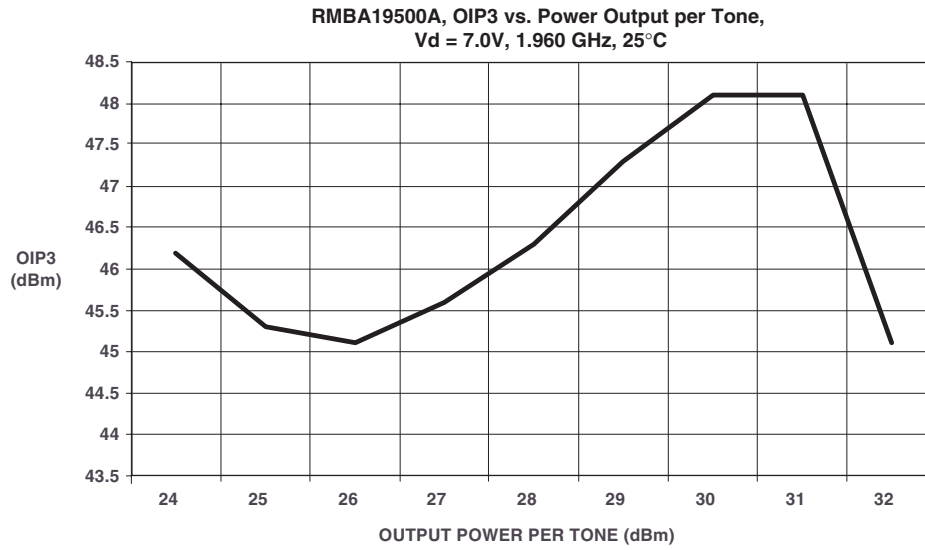
Part	Value	Size (EIA)	Vendor(s)
L1, L2, L4	5.6nH	.06" x .03"	Toko (LL1608-F5N6)
L3	10nH	.085" x .060"	Coilcraft (0805HT-10NTKBC)
C1	10pF	.067" x .036"	Murata (GRM39COG100J050AD)
C9	2.2pF	.042" x .022"	Murata (GRM36COG2R2J050BD)
C3, C4, C5	1500pF	.067" x .036"	Murata (GRM39Y5V152Z50V)
C10	2.0pF		Murata (GRM36COG2R20J050BD)
C2	15.0pF	.042" x .022"	Murata (GRM36COG150J050)
C8, C11, C14, C15	4.7μF	.134" x .071"	TDK (C3216XR1A475KT)
C6, C7	0.1μF	.183" x .054"	Murata (GRM39Y5V104Z50)
R1, R5	20Ω	.069" x .037"	IMS (RCI-0603-20R0J)
R2, R7	1000Ω	.069" x .037"	IMS (RCI-0603-1001J)
R3	910Ω	.069" x .037"	IMS (RCI-0603-9100J)
R4	30Ω	.069" x .037"	IMS (RCI-0603-30R0J)
R6	1.1KΩ	.069" x .037"	IMS (RCI-0603-1101J)
R8	390Ω		IMS (RCI-0603-3900J)
R9	300Ω		IMS (RCI-0603-3000J)
U1	RMBA19500-58	.31" x .41"	Fairchild
HS	Heatsink		Fairchild, G655548
P1	Terminals		3M (2340-5211TN)
J1, J2	SMA Connectors		E.F. Johnson (142-0701-841)
Board	FR4		Fairchild Dwg# G654187/G654941

**Thermal Considerations for Heat Sinking the RMBA19500**

The PWB must be prepared with either an embedded copper slug in the board where the package is to be mounted or a heat sink should be attached to the backside of the PWB where the package is to be mounted on the front side. The slug or the heat sink should be made of a highly electrically and thermally conductive material such as copper or aluminum. The slug should be at least the same thickness as the PWB. In the case of the heat sink, a small pedestal should protrude through a hole in the PWB where the package bottom is directly soldered. In either

configuration, the top surface of the slug or the pedestal should be made coplanar with the package lead mounting plane i.e., the top surface of the PWB. Use Sn96 solder (96.5% Sn and 3.5% Ag) at 220°C for 20 seconds or less to attach the heat sink to the backside of the PWB. Then, using Sn63, the package bottom should be firmly soldered to the slug or the pedestal while the pins are soldered to the respective pads on the front side of the PWB without causing any stress on the pins. Remove flux completely if used for soldering.

## Performance Data



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