FAIRCHILD SEMICONDUCTOR TM

May 1998

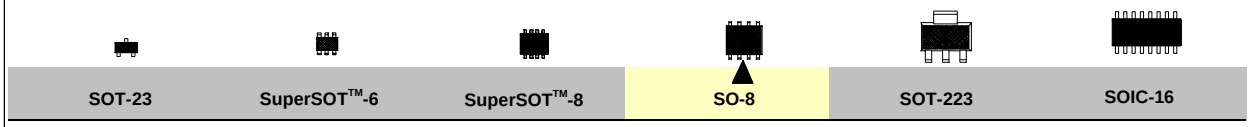
# NDS9955
# Dual N-Channel Enhancement Mode Field Effect Transistor

## General Description

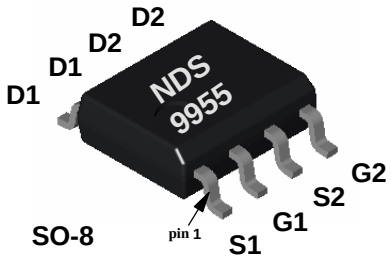
SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to provide superior switching performance and minimize on-state resistance. These devices are particularly suited for low voltage applications such as disk drive motor control, battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

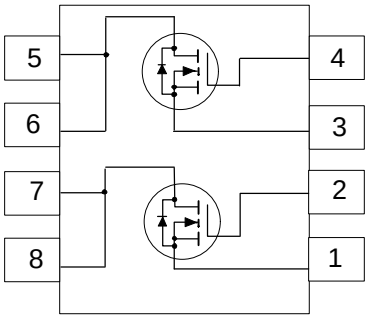
## Features

- 3.0 A, 50 V. $R_{DS(ON)}$ = 0.130 Ω @ $V_{GS}$ = 10 V,
  $R_{DS(ON)}$ = 0.200 Ω @ $V_{GS}$ = 4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16




## Absolute Maximum Ratings $T_A$ = 25°C unless other wise noted

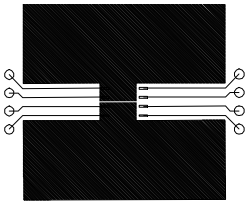
| Symbol | Parameter | | NDS9955 | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 50 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 3 | A |
| | - Pulsed | | 10 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | |
| | | (Note 1b) | 1 | |
| | | (Note 1c) | 0.9 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Electrical Characteristics ($T_A$ = 25 °C unless otherwise noted )

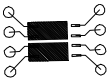
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 50 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | 60 | | mV/ °C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | | | 2 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.7 | 3 | V |
| | | $T_J$ =125°C | 0.7 | | 2.2 | |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 3 A | | 0.076 | 0.13 | Ω |
| | | $T_J$ =125°C | | 0.124 | 0.2 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 1.5 A | | 0.103 | 0.2 | |
| | | $T_J$ =125°C | | 0.166 | 0.3 | |
| $I_{D(ON)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | 10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3 A | | 5.3 | | S |
| **DYNAMIC CH ARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 345 | | pF |
| $C_{oss}$ | Output Capacitance | | | 110 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 25 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DS}$ = 25 V, $I_D$ = 1 A | | 5 | 20 | ns |
| $t_r$ | Turn - On Rise Time | $V_{GS}$ = 10 V , $R_{GEN}$ = 6 Ω | | 7.5 | 20 | |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 20 | 70 | |
| $t_f$ | Turn - Off Fall Time | | | 7 | 5 | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 25 V, $I_D$ = 2 A, $V_{GS}$ = 10 V | | 12.9 | 30 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 1.7 | | |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.2 | | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | | 0.8 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_F$ = 1.3 A, $dI_F/dt$ = 100 A/µs | | 40 | | ns |
| $I_{rr}$ | Reverse Recovery Current | | | 1.5 | | A |

Notes:

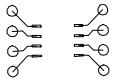
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

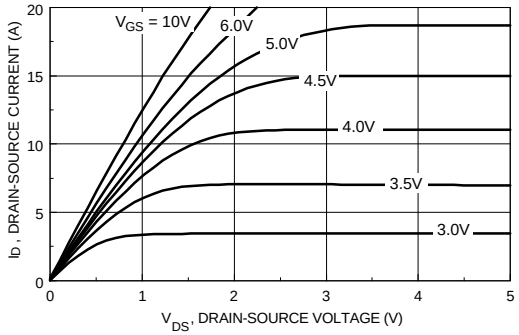



**Figure 1. On-Region Characteristics.**

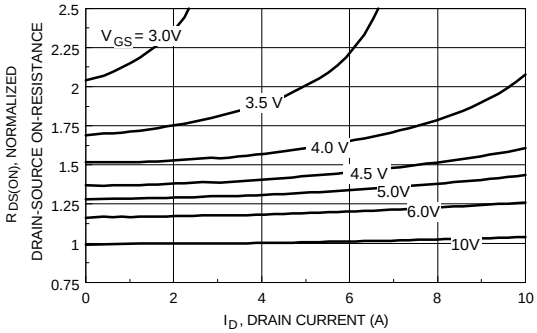



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

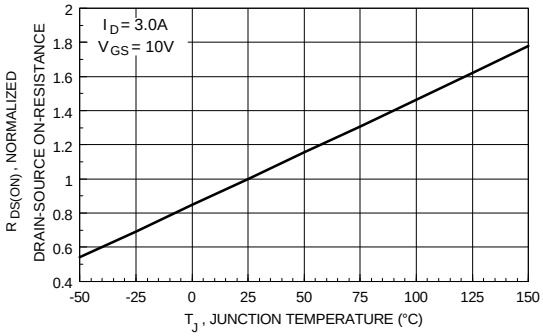



**Figure 3. On-Resistance Variation With Temperature.**

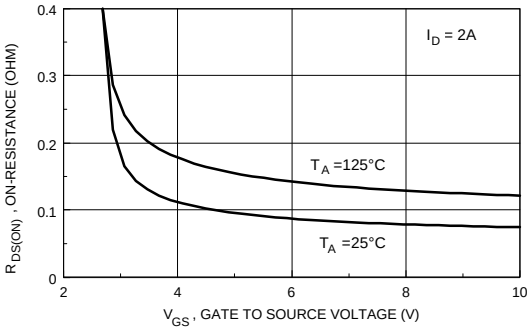



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

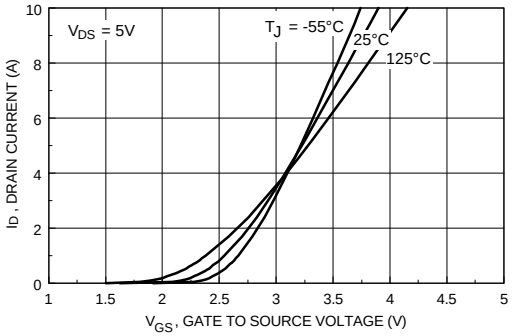



**Figure 5 . Transfer Characteristics.**

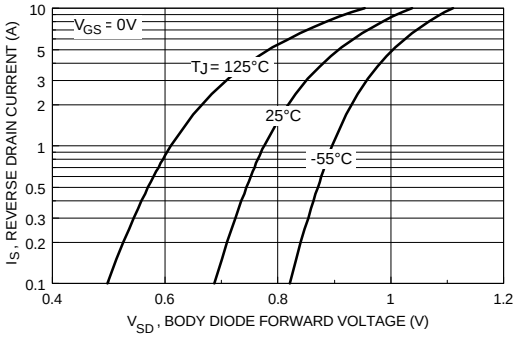



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical Characteristics (continued)

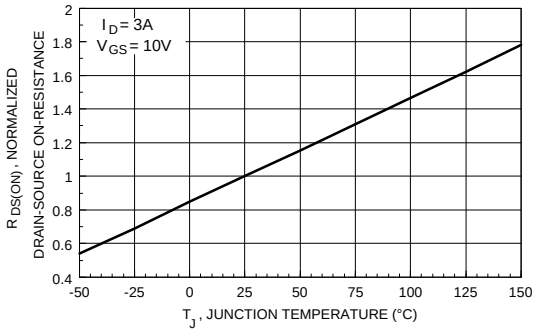



**Figure 7. Gate Charge Characteristics.**

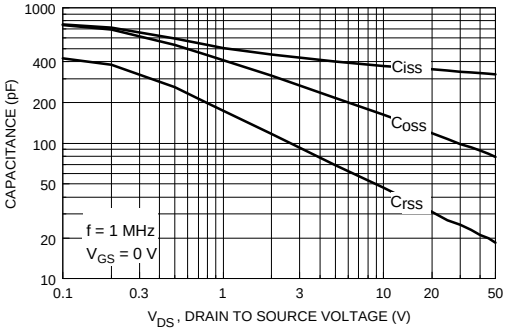



**Figure 8. Capacitance Characteristics.**

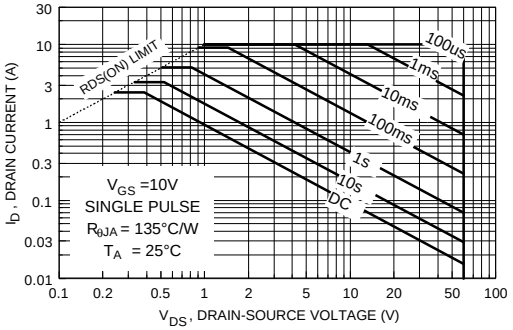



**Figure 9. Maximum Safe Operating Area.**

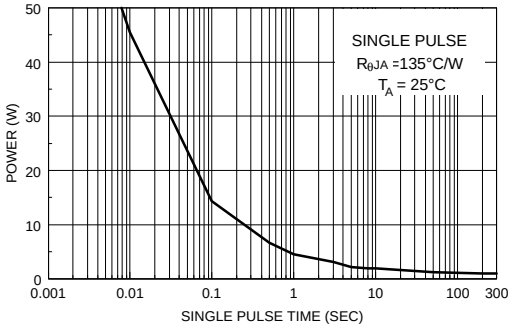



**Figure 10. Single Pulse Maximum Power Dissipation.**

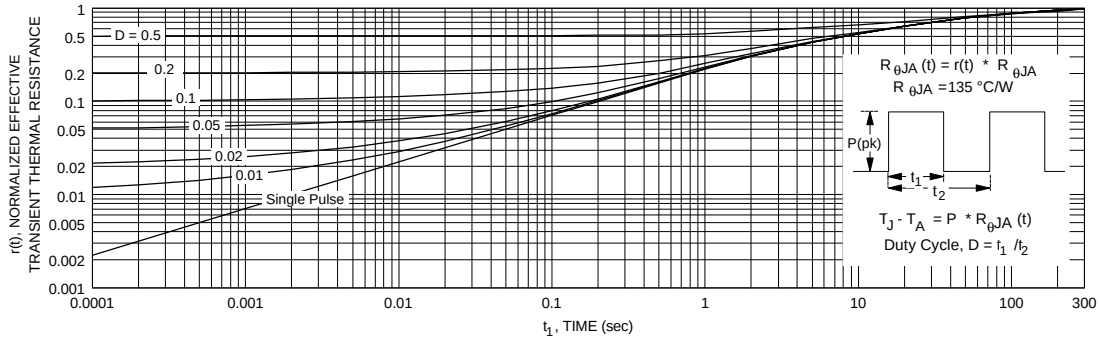


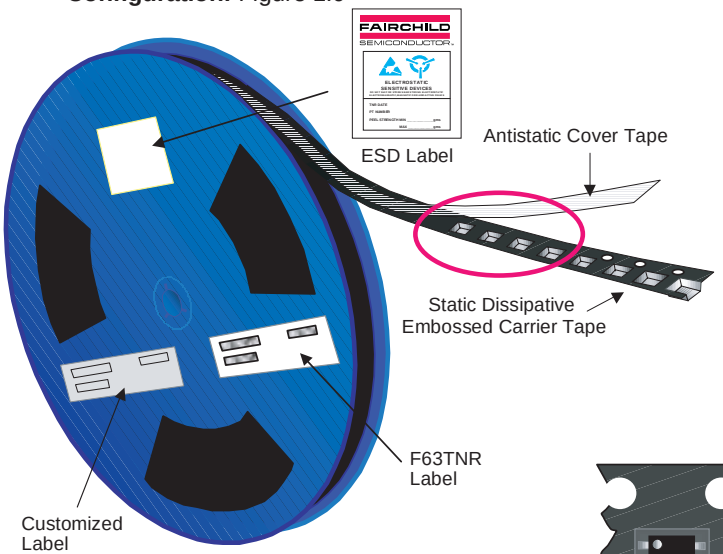

**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

# SO-8 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

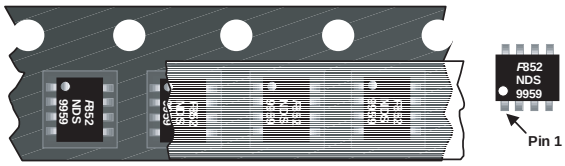
## SOIC(8lds) Packaging Configuration: Figure 1.0




**Packaging Description:**

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

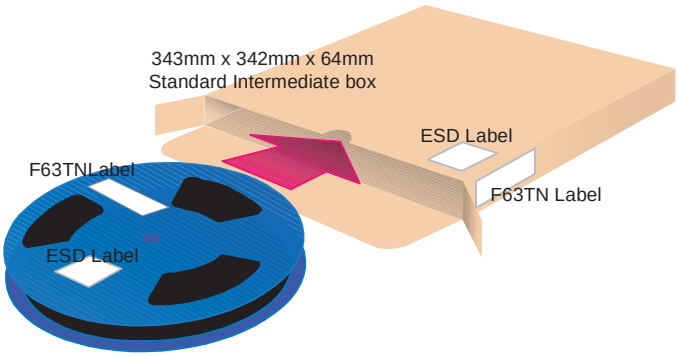



**SOIC-8 Unit Orientation**

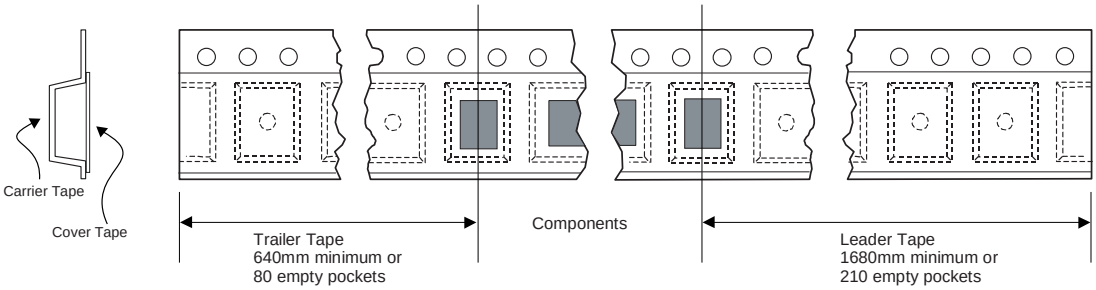
| SOIC (8lds) Packaging Information | | | | |
|---|---|---|---|---|
| **Packaging Option** | Standard (no flow code) | L86Z | F011 | D84Z |
| **Packaging type** | TNR | Rail/Tube | TNR | TNR |
| **Qty per Reel/Tube/Bag** | 2,500 | 95 | 4,000 | 500 |
| **Reel Size** | 13" Dia | - | 13" Dia | 7" Dia |
| **Box Dimension (mm)** | 343x64x343 | 530x130x83 | 343x64x343 | 184x187x47 |
| **Max qty per Box** | 5,000 | 30,000 | 8,000 | 1,000 |
| **Weight per unit (gm)** | 0.0774 | 0.0774 | 0.0774 | 0.0774 |
| **Weight per Reel (kg)** | 0.6060 | - | 0.9696 | 0.1182 |
| **Note/Comments** | | | | |

F63TNR Label sample

LOT: CBVK741B019 QTY: 2500
FSID: FDS9953A SPEC:
D/C1: D9842 QTY1: SPEC REV:
D/C2: QTY2: CPN:
N/F: F (F63TNR)3

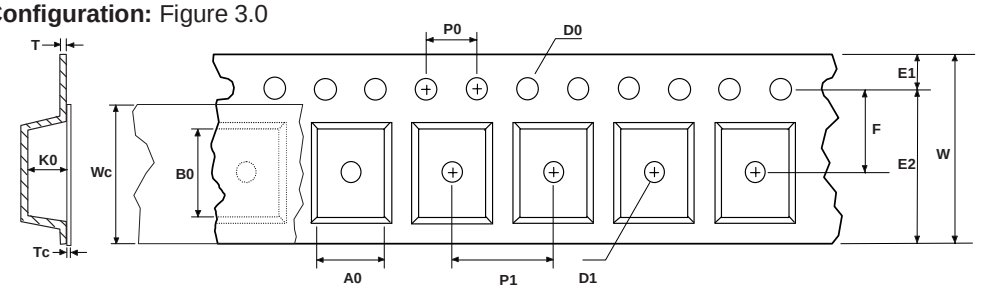



## SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



# SO-8 Tape and Reel Data and Package Dimensions, continued

## SOIC(8lds) Embossed Carrier Tape
**Configuration:** Figure 3.0

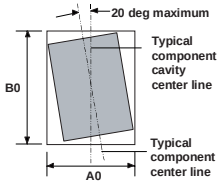



**User Direction of Feed**

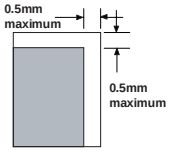
| Dimensions are in millimeter | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg type** | **A0** | **B0** | **W** | **D0** | **D1** | **E1** | **E2** | **F** | **P1** | **P0** | **K0** | **T** | **Wc** | **Tc** |
| **SOIC**(8lds) (12mm) | 6.50 +/-0.10 | 5.30 +/-0.10 | 12.0 +/-0.3 | 1.55 +/-0.05 | 1.60 +/-0.10 | 1.75 +/-0.10 | 10.25 min | 5.50 +/-0.05 | 8.0 +/-0.1 | 4.0 +/-0.1 | 2.1 +/-0.10 | 0.450 +/- 0.150 | 9.2 +/-0.3 | 0.06 +/-0.02 |

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).


Sketch A (Side or Front Sectional View)
**Component Rotation**

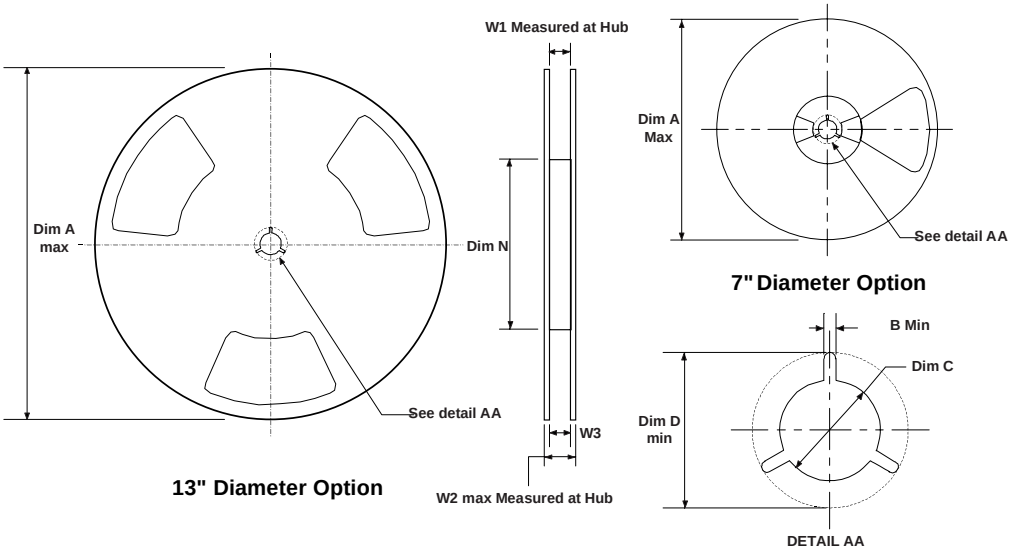



Sketch B (Top View)
**Component Rotation**




Sketch C (Top View)
**Component lateral movement**

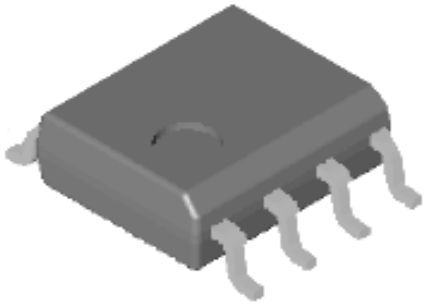
## SOIC(8lds) Reel Configuration: Figure 4.0

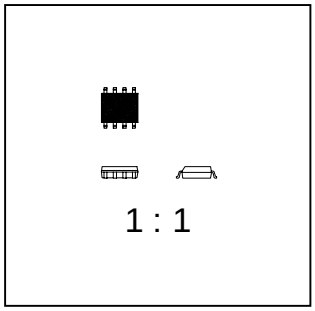



| Dimensions are in inches and millimeters | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Tape Size** | **Reel Option** | **Dim A** | **Dim B** | **Dim C** | **Dim D** | **Dim N** | **Dim W1** | **Dim W2** | **Dim W3 (LSL-USL)** |
| 12mm | 7" Dia | 7.00 177.8 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 2.165 55 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |
| 12mm | 13" Dia | 13.00 330 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 7.00 178 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |

## SO-8 Tape and Reel Data and Package Dimensions, continued

# SOIC-8 (FS PKG Code S1)

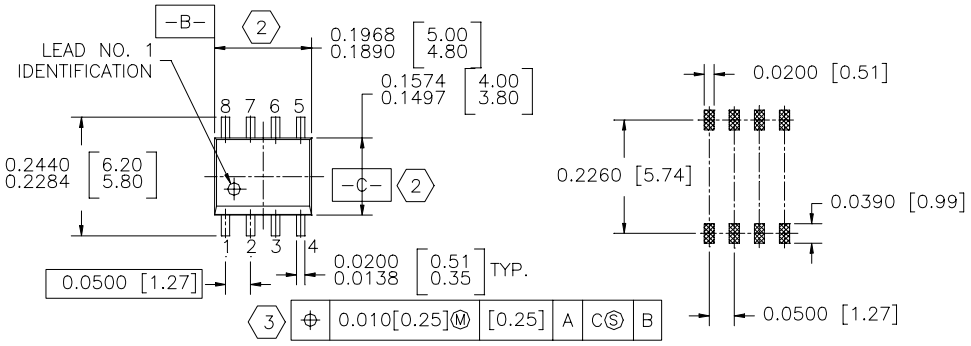


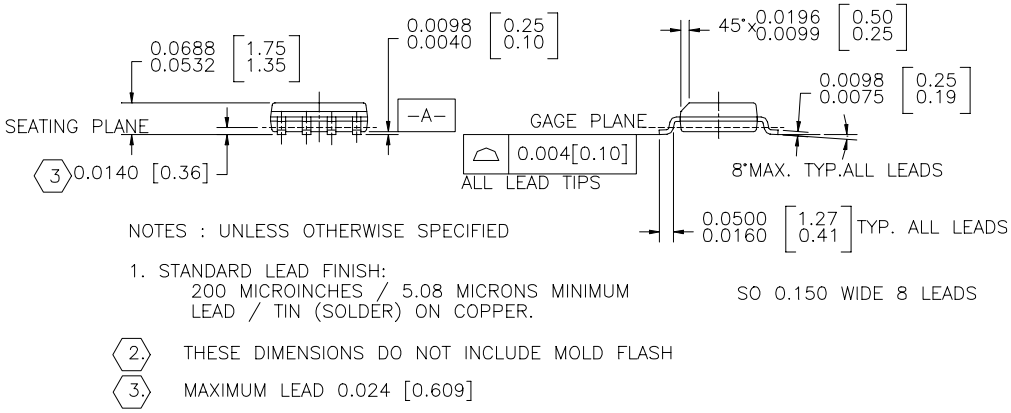



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774




NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES / 5.08 MICRONS MINIMUM
   LEAD / TIN (SOLDER) ON COPPER.

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |