AN-9729

LED Application Design Guide Using Half-Bridge LLC Resonant Converter for 100W Street Lighting

Introduction

This application note describes the LED driving system using a half-bridge LLC resonant converter for high power LED lighting applications, such as outdoor or street lighting. Due to the existence of the non-isolation DC-DC converter to control the LED current and the light intensity, the conventional PWM DC-DC converter has the problem of low-power conversion efficiency. The half-bridge LLC converter can perform the LED current control and the efficiency can be significantly improved. Moreover, the cost and the volume of the whole LED driving system can be reduced.

Consideration of LED Drive

LED lighting is rapidly replacing conventional lighting sources like incandescent bulbs, fluorescent tubes, and halogens because LED lighting reduces energy consumption. LED lighting has greater longevity, contains no toxic materials, and emits no harmful UV rays, which are 5 ~ 20 times longer than fluorescent tubes and incandescent bulbs. All metal halide and fluorescent lamps, including CFLs, n contain mercury.

The amount of current through an LED determines the light it emits. The LED characteristics determine the forward voltage necessary to achieve the required level of current. Due to the variation in LED voltage versus current characteristics, controlling only the voltage across the LED leads to variability in light output. Therefore, most LED drivers use current regulation to support brightness control. Brightness can be controlled directly by changing the LED current.

Consideration of LLC Resonant Converter

The attempt to obtain ever-increasing power density of switched-mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters; however, switching losses have been an obstacle to high-frequency operation. To reduce switching losses and allow high-frequency operation, resonant switching techniques have been developed. These techniques process power in a sinusoidal manner and the switching devices are softly commutated. Therefore, the switching losses and noise can be dramatically reduced[1-7].

Among various kinds of resonant converters, the simplest and most popular is the LC series resonant converter, where the rectifier-load network is placed in series with the L-C resonant network, as depicted in Figure 1[2-4]. In this configuration, the resonant network and the load act as a voltage divider. By changing the frequency of driving voltage V_d, the impedance of the resonant network changes. The input voltage is split between this impedance and the reflected load. Since it is a voltage divider, the DC gain of a LC series resonant converter is always <1. At light-load condition, the impedance of the load is large compared to the impedance of the resonant network; all the input voltage is imposed on the load. This makes it difficult to regulate the output at light load. Theoretically, frequency should be infinite to regulate the output at no load.
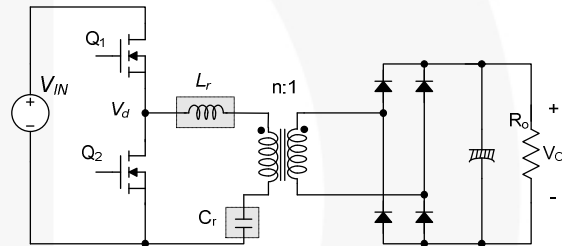

Figure 1. Half-Bridge, LC Series Resonant Converter

To overcome the limitation of series resonant converters, the LLC resonant converter has been proposed[8-12]. The LLC resonant converter is a modified LC series resonant converter implemented by placing a shunt inductor across the transformer primary winding, as depicted in Figure 2. When this topology was first presented, it did not receive much attention due to the counterintuitive concept that increasing the circulating current in the primary side with a shunt inductor can be beneficial to circuit operation. However, it can be very effective in improving efficiency for high-input voltage applications where the switching loss is more dominant than the conduction loss.

In most practical designs, this shunt inductor is realized using the magnetizing inductance of the transformer. The circuit diagram of LLC resonant converter looks much the same as the LC series resonant converter: the only difference is the value of the magnetizing inductor. While the series resonant converter has a magnetizing inductance larger than the LC series resonant inductor (L_r), the magnetizing inductance in an LLC resonant converter is just 3~8 times L_r, which is usually implemented by introducing an air gap in the transformer.
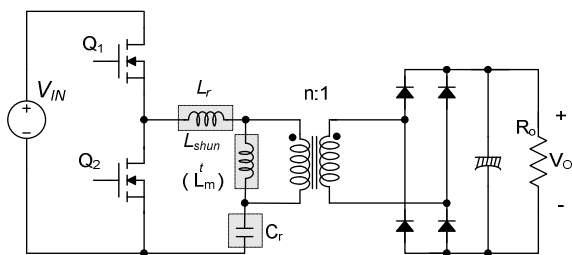
Figure 2.　Half-Bridge LLC Resonant Converter

An LLC resonant converter has many advantages over a series resonant converter. It can regulate the output over wide line and load variations with a relatively small variation of switching frequency. It can achieve zero voltage switching (ZVS) over the entire operating range. All essential parasitic elements, including junction capacitances of all semiconductor devices and the leakage inductance and magnetizing inductance of the transformer, are utilized to achieve soft switching.

This application note presents design considerations of an LLC resonant half-bridge converter employing Fairchild's FLS-XS series. It includes explanation of the LLC resonant converter operation principles, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure, explained with a design example, helps design the LLC resonant converter.

LLC Resonant Converter and Fundamental Approximation

Figure 3 shows a simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Figure 4 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is same as the resonance frequency, determined by the resonance between L_r and C_r. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is sum of the magnetizing current and the secondary-side current referred to the primary.

In general, the LLC resonant topology consists of three stages shown in Figure 3; square-wave generator, resonant network, and rectifier network.

- The square-wave generator produces a square-wave voltage, V_d, by driving switches Q_1 and Q_2 alternately with 50% duty cycle for each switch. A small dead time is usually introduced between the consecutive transitions. The square-wave generator stage can be built as a full-bridge or half-bridge type.

- The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current is allowed to flow through the resonant

network even though a square-wave voltage is applied to the resonant network. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square-wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As shown in Figure 4, the MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.

- The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and a capacitor. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration with capacitive output filter.
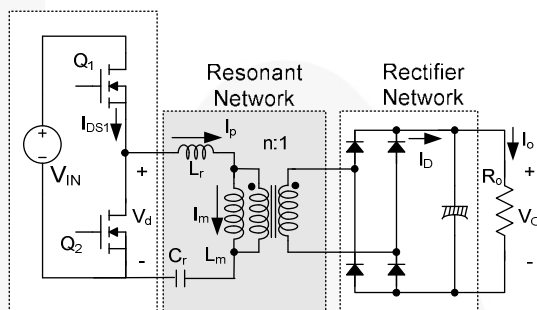

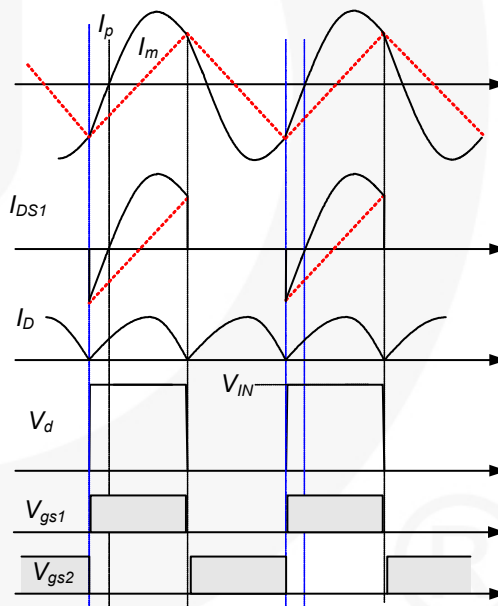**Figure 3.　Schematic of Half-Bridge LLC Resonant Converter**

Figure 4.　Typical Waveforms of Half-Bridge LLC Resonant Converter

The filtering action of the resonant network allows use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 5 shows how this equivalent load resistance is derived. The

primary-side circuit is replaced by a sinusoidal current source, I_{ac}, and a square wave of voltage, V_{RI}, appears at the input to the rectifier. Since the average of $|I_{ac}|$ is the output current, I_o, I_{ac}, is obtained as:

$$I_{ac} = \frac{\pi \cdot I_o}{2} \sin(\omega t) \tag{1}$$

and V_{RI} is given as:

$$\begin{aligned} V_{RI} &= +V_o \quad if \sin(\omega t) > 0 \\ V_{RI} &= -V_o \quad if \sin(\omega t) < 0 \end{aligned} \tag{2}$$

where V_o is the output voltage.

The fundamental component of V_{RI} is given as:

$$V_{RI}{}^F = \frac{4V_o}{\pi} \sin(\omega t) \tag{3}$$

Since harmonic components of V_{RI} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{RI}{}^F$ by I_{ac} as:

$$R_{ac} = \frac{V_{RI}{}^F}{I_{ac}} = \frac{8}{\pi^2} \frac{V_o}{I_o} = \frac{8}{\pi^2} R_o \tag{4}$$

Considering the transformer turns ratio (n=N_p/N_s), the equivalent load resistance shown in the primary side is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2} R_o \tag{5}$$

By using the equivalent load resistance, the AC equivalent circuit is obtained, as illustrated in Figure 6, where $V_d{}^F$ and $V_{RO}{}^F$ are the fundamental components of the driving voltage, V_d, and reflected output voltage, V_{RO} (nV_{RI}), respectively.
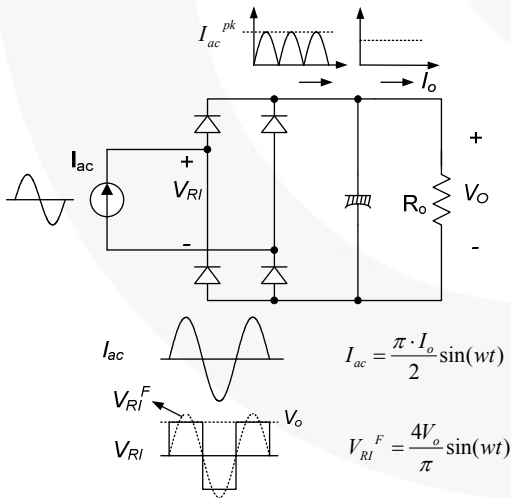

Figure 5. Derivation of Equivalent Load Resistance R_{ac}

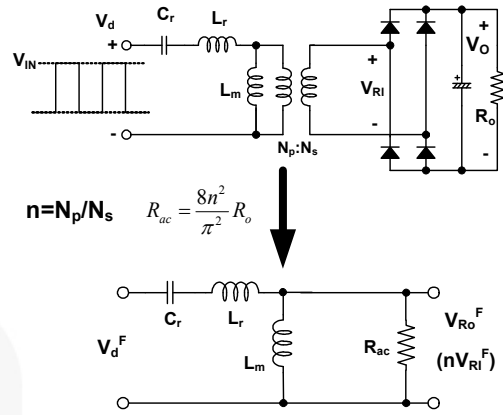$$n=N_p/N_s \quad R_{ac} = \frac{8n^2}{\pi^2} R_o$$

Figure 6. AC Equivalent Circuit for LLC Resonant Converter

With the equivalent load resistance obtained in Equation 5, the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Figure 6, the voltage gain, M, is obtained as:

$$M = \frac{V_{RO}{}^F}{V_d{}^F} = \frac{n \cdot V_{RI}{}^F}{V_d{}^F} = \frac{\frac{4n \cdot V_o}{\pi} \sin(\omega t)}{\frac{4}{\pi} \frac{V_{in}}{2} \sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}}$$

$$= \left| \frac{(\frac{\omega}{\omega_o})^2 (m-1)}{(\frac{\omega^2}{\omega_p{}^2} - 1) + j \frac{\omega}{\omega_o} (\frac{\omega^2}{\omega_o{}^2} - 1)(m-1)Q} \right| \tag{6}$$

where:

$$L_p = L_m + L_r \;, \; R_{ac} = \frac{8n^2}{\pi^2} R_o \;, \; m = \frac{L_p}{L_r}$$

$$Q = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}} \;, \; \omega_o = \frac{1}{\sqrt{L_r C_r}} \;, \; \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As can be seen in Equation (6), there are two resonant frequencies. One is determined by L_r and C_r, while the other is determined by L_p and C_r.

Equation (6) shows the gain is unity at resonant frequency (ω_o), regardless of the load variation, which is given as:

$$M = \frac{2n \cdot V_o}{V_{in}} = \frac{(m-1) \cdot \omega_p{}^2}{\omega_o{}^2 - \omega_p{}^2} = 1 \quad at \, \omega = \omega_o \tag{7}$$

The gain of Equation (6) is plotted in Figure 7 for different Q values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 7, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, f_o. This is a distinct advantage of LLC-type resonant converter over the conventional series resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.

The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with '*' in Figure 7. Note that the peak voltage gain does not occur at f_o or f_p. The peak gain frequency where the peak gain is obtained exists between

f_p and f_o, as shown in Figure 7. As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o and the peak gain drops; the full load condition should be worst case for the resonant network design.
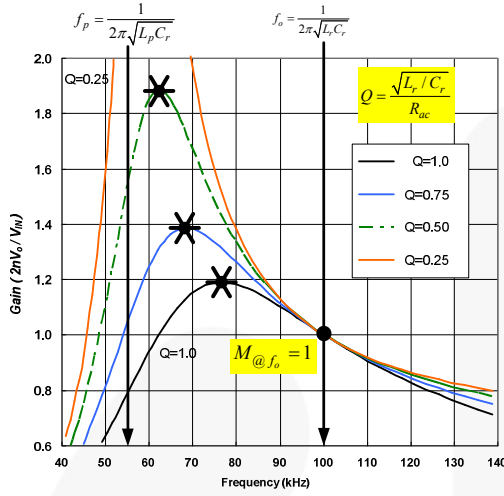

Figure 7.   Typical Gain Curves of LLC Resonant Converter (*m*=3)

Consideration for Integrated Transformer

For practical design, it is common to implement the magnetic components (series inductor and shunt inductor) using an integrated transformer; where the leakage inductance is used as a series inductor, while the magnetizing inductor is used as a shunt inductor. When building the magnetizing components in this way, the equivalent circuit in Figure 6 should be modified as shown in Figure 8 because leakage inductance exists, not only in the primary side, but also in the secondary side. Not considering the leakage inductance in the transformer secondary side generally results in an ineffective design.
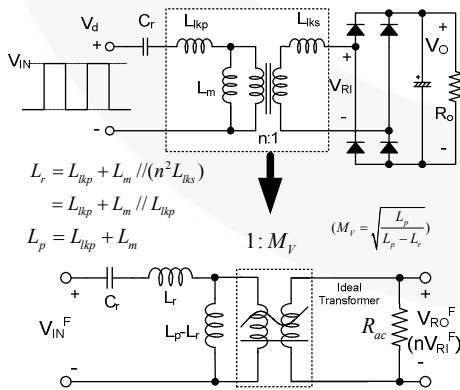

Figure 8.   Modified Equivalent Circuit to Accommodate the Secondary-Side Leakage Inductance

In Figure 8, the effective series inductor (L_p) and shunt inductor (L_p-L_r) are obtained by assuming $n^2 L_{lks} = L_{lkp}$ and referring the secondary-side leakage inductance to the primary side as:

$$L_p = L_m + L_{lkp}$$

$$L_r = L_{lkp} + L_m // (n^2 L_{lks}) = L_{lkp} + L_m // L_{lkp} \tag{8}$$

When handling an actual transformer, equivalent circuit with L_p and L_r is preferred since these values can be measured with a given transformer. In an actual transformer, L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively.

In Figure 9, notice that a virtual gain M_V is introduced, which is caused by the secondary-side leakage inductance. By adjusting the gain equation of Equation (6) using the modified equivalent circuit of Figure 9, the gain equation for integrated transformer is obtained by:

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega}{\omega_o})^2 \cdot (m-1) \cdot M_V}{(\frac{\omega^2}{\omega_p^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o^2} - 1) \cdot (m-1)Q^e} \right|$$

$$= \left| \frac{(\frac{\omega^2}{\omega_o^2})\sqrt{m(m-1)}}{(\frac{\omega^2}{\omega_p^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o^2} - 1) \cdot (m-1) \cdot Q^e} \right|$$

where: (9)

$$R_{ac}^{\ e} = \frac{8n^2}{\pi^2} \frac{R_o}{M_V^{\ 2}}, \ m = \frac{L_p}{L_r}$$

$$Q^e = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}^{\ e}}, \ \omega_o = \frac{1}{\sqrt{L_r C_r}}, \ \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

The gain at the resonant frequency (ω_o) is fixed regardless of the load variation, which is given as:

$$M = M_V = \sqrt{\frac{L_p}{L_p - L_r}} = \sqrt{\frac{m}{m-1}} \quad at \, \omega = \omega_o \tag{10}$$

The gain at the resonant frequency (ω_o) is unity when using individual core for series inductor, as shown in Equation 7. However, when implementing the magnetic components with integrated transformer, the gain at the resonant frequency (ω_o) is larger than unity due to the virtual gain caused by the leakage inductance in the transformer secondary side.

The gain of Equation (9) is plotted in Figure 10 for different Q^e values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 9, the LLC resonant converter shows gain characteristics almost independent of the load when the switching frequency is around the resonant frequency, f_o.
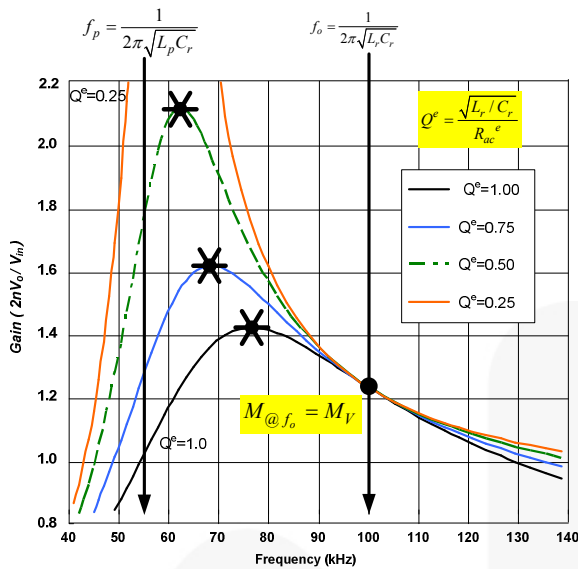
Figure 9.   Typical Gain Curves of LLC Resonant Converter (*m*=3) Using an Integrated Transformer

Consideration of Operation Mode and Attainable Maximum Gain

Operation Mode

The LLC resonant converter can operate at frequency below or above the resonance frequency (f_o), as illustrated in Figure 10. Figure 11 shows the waveforms of the currents in the transformer primary side and secondary side for each operation mode. Operation below the resonant frequency (case I) allows the soft commutation of the rectifier diodes in the secondary side, while the circulating current is relatively large. The circulating current increases more as the operation frequency moves downward from the resonant frequency. Meanwhile, operation above the resonant frequency (case II) allows the circulating current to be minimized, but the rectifier diodes are not softly commutated. Below-resonance operation is preferred for high output voltage applications, such as street LED lighting systems where the reverse-recovery loss in the rectifier diode is severe. Below-resonance operation has a narrow frequency range with respect to the load variation since the frequency is limited below the resonance frequency even at no-load condition.

On the other hand, above-resonance operation has less conduction loss than the below-resonance operation. It can show better efficiency for low output voltage applications, such as Liquid Crystal Display (LCD) TV or laptop adaptor, where Schottky diodes are available for the secondary-side rectifiers and reverse-recovery problems are insignificant. However, operation above the resonant frequency may cause too much frequency increase at light-load condition. Above-frequency operation requires frequency skipping to prevent too much increase of the switching frequency.
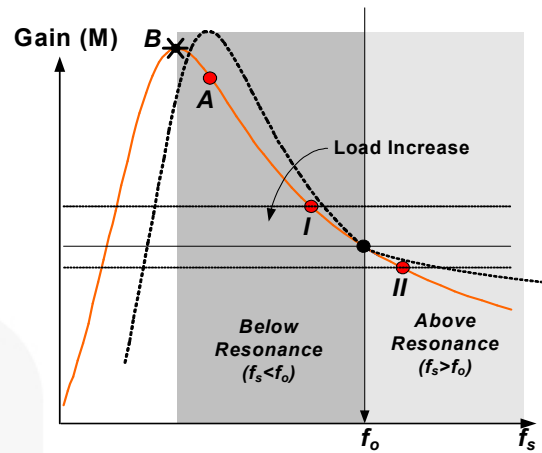

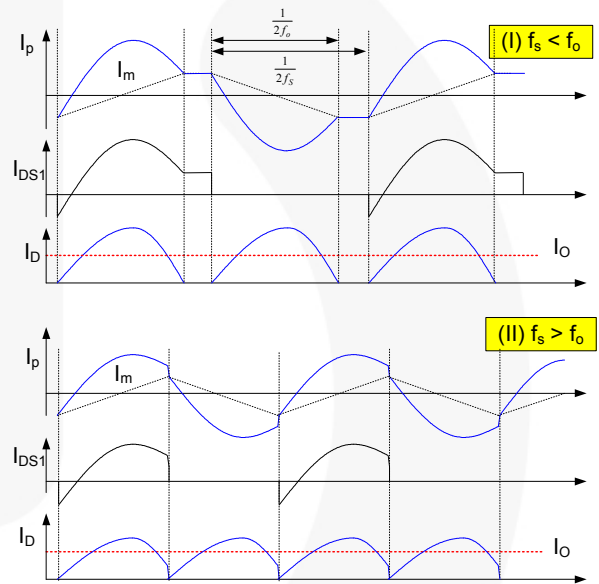**Figure 10. Operation Modes According to the Operation Frequency**

Figure 11. Waveforms of Each Operation Mode

Required Maximum Gain and Peak Gain

Above the peak gain frequency, the input impedance of the resonant network is inductive and the input current of the resonant network (I_p) lags the voltage applied to the resonant network (V_d). This permits the MOSFETs to turn on with zero voltage (ZVS), as illustrated in Figure 12. Meanwhile, the input impedance of the resonant network becomes capacitive and I_p leads V_d below the peak gain frequency. When operating in capacitive region, the MOSFET body diode is reverse recovered during the switching transition, which results in severe noise. Another problem of entering the capacitive region is that the output voltage becomes out of control since the slope of the gain is reversed. The minimum switching frequency should be limited above the peak gain frequency.
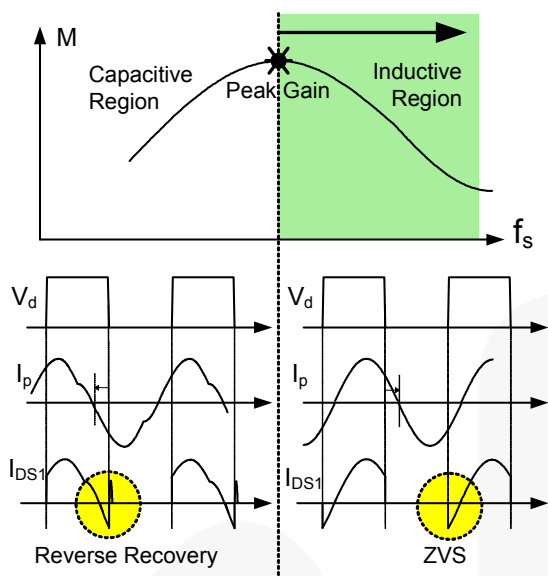
Figure 12. Operation Waveforms for Capacitive and Inductive Regions

The available input voltage range of the LLC resonant converter is determined by the peak voltage gain. Thus, the resonant network should be designed so that the gain curve has an enough peak gain to cover the input voltage range. However, ZVS condition is lost below the peak gain point, as depicted in Figure 12. Therefore, some margin is required when determining the maximum gain to guarantee stable ZVS operation during the load transient and startup. Typically 10~20% of the maximum gain is used as a margin, as shown in Figure 13.
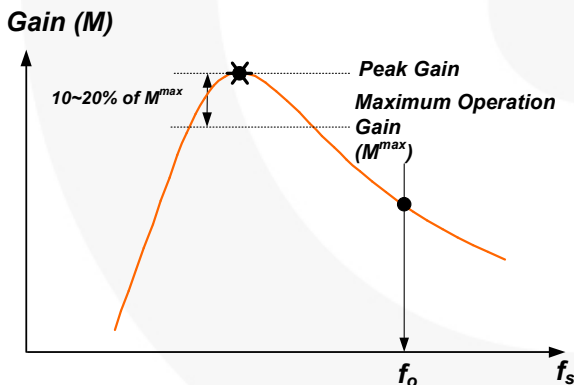
Figure 13. Determining the Maximum Gain

Even though the peak gain at a given condition can be obtained using the gain in Equation (6), it is difficult to express the peak gain in explicit form. To simplify the analysis and design, the peak gains are obtained using simulation tools and depicted in Figure 14, which shows how the peak gain (attainable maximum gain) varies with Q for different m values. It appears that higher peak gain can be obtained by reducing m or Q values. With a given resonant frequency (f_o) and Q value, decreasing m means reducing the magnetizing inductance, which results in increased circulating current. There is a trade-off between the available gain range and conduction loss.
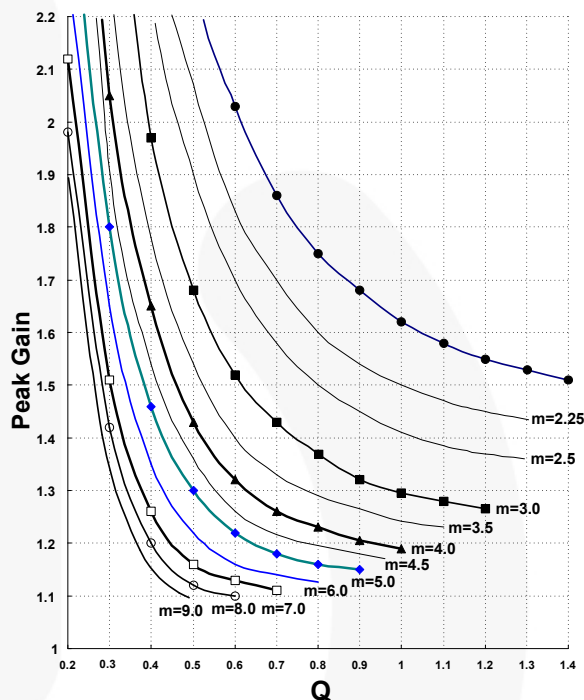

Figure 14. Peak Gain (Attainable Maximum Gain) vs. Q for Different m Values

Features of FLS-XS Series

FLS-XS series is an integrated Pulse Frequency Modulation (PFM) controller and MOSFETs specifically designed for Zero Voltage Switching (ZVS) half-bridge converters with minimal external components. The internal controller includes an under-voltage lockout, optimized high-side / low-side gate driver, temperature-compensated precise current controlled oscillator, and self-protection circuitry. Compared with discrete MOSFET and PWM controller solutions, FLS-XS series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability.
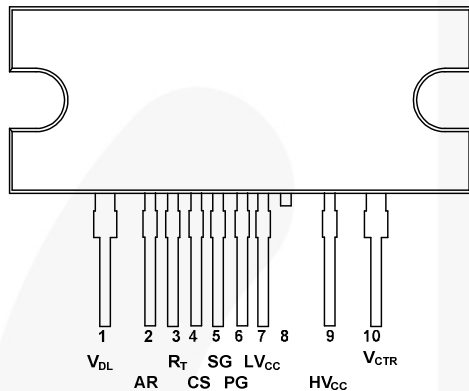
Table 1.   Pin Description

Pin#	Name	Description
1	V_{DL}	This pin is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	AR	This pin is for discharging the external soft-start capacitor when any protections are triggered. When the voltage of this pin drops to 0.2V, all protections are reset and the controller starts to operate again.
3	R_T	This pin is to program the switching frequency. Typically, opto-coupler and resistor are connected to this pin to regulate the output voltage.
4	CS	This pin is to sense the current flowing through the low-side MOSFET. Typically negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LV_{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HV_{CC}	This pin is the supply voltage of the high-side drive circuit.
10	V_{CTR}	This pin is the drain of the low-side MOSFET. Typically transformer is connected to this pin.

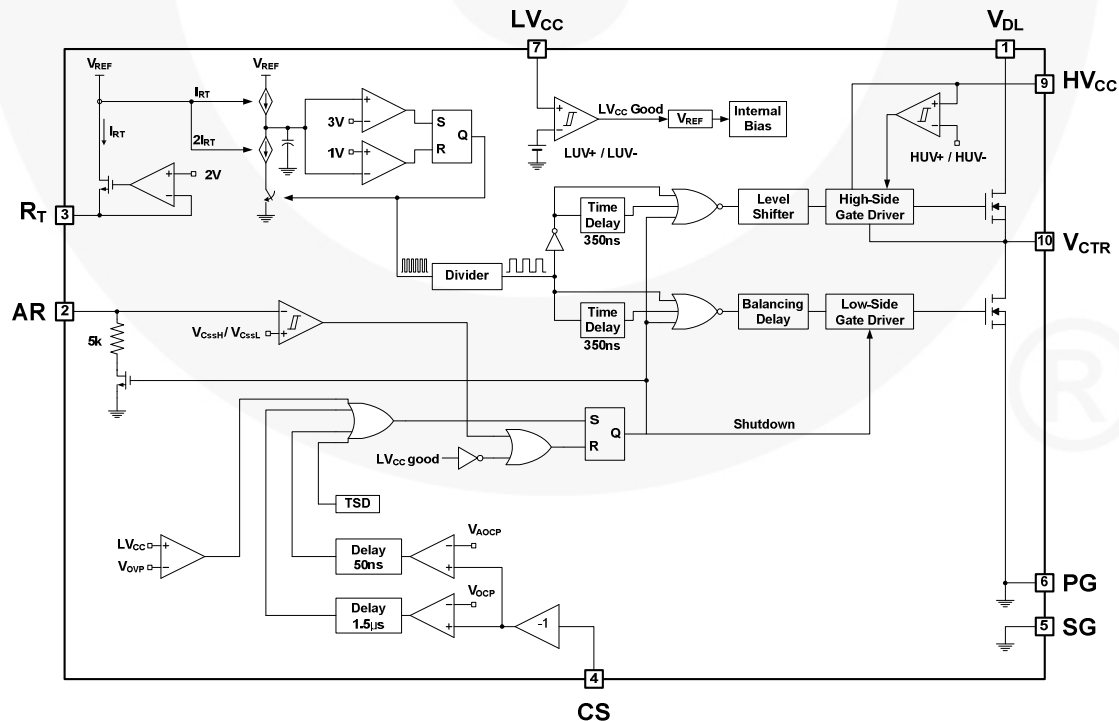**Figure 15. Package Diagram**

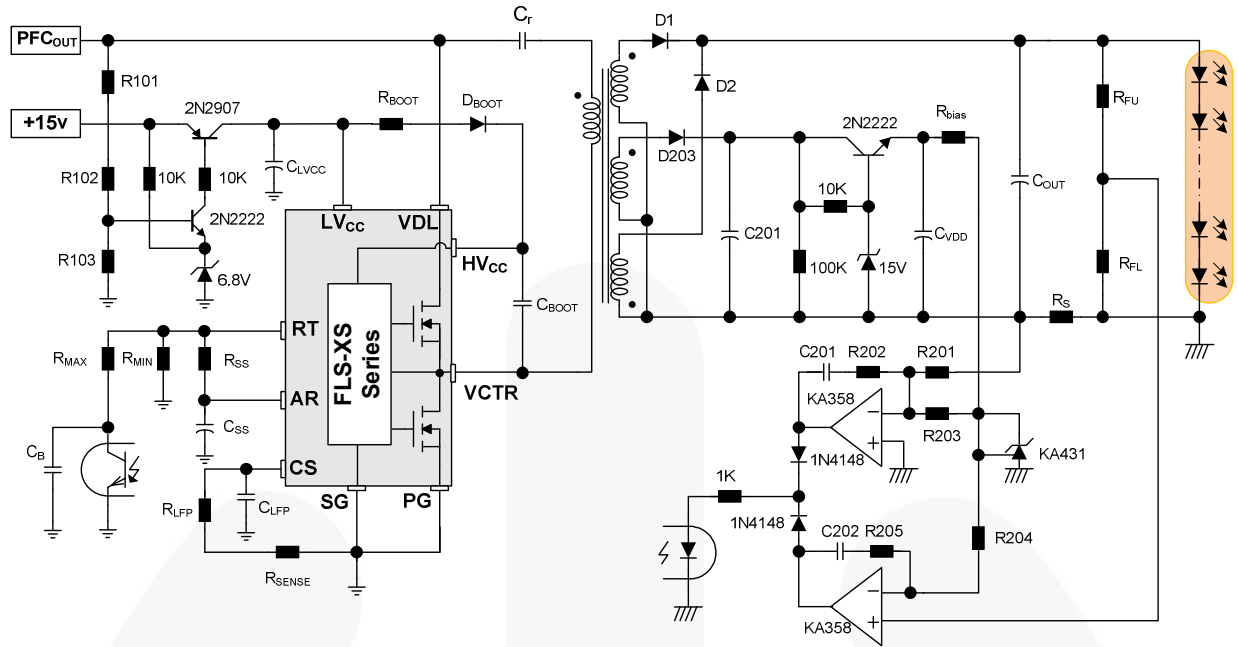**Figure 16. Functional Block Diagram of FSFR-Series**

Figure 17. Reference Circuit for Design Example of LLC Resonant Half-Bridge Converter

Design Procedure

In this section, a design procedure is presented using the schematic in Figure 17 as a reference. An integrated transformer with center tap, secondary side is used and input is supplied from Power Factor Correction (PFC) pre-regulator. A DC-DC converter with 100W/100V output has been selected as a design example. The design specifications are as follows:

- Nominal input voltage: $400V_{DC}$ (output of PFC stage)
- Output: 100V/1A (100W)
- Hold-up time requirement: 30ms (50Hz line freq.)
- DC link capacitor of PFC output: 240μF

[STEP-1] Define System Specifications

Estimated Efficiency (E_{ff}): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use E_{ff} = 0.88~0.92 for low-voltage output applications and E_{ff} = 0.92~0.96 for high-voltage output applications. With the estimated efficiency, the maximum input power is given as:

$$P_{in} = \frac{P_o}{E_{ff}} \tag{11}$$

Input Voltage Range (V_{in}^{min} and V_{in}^{max}): The maximum input voltage would be the nominal PFC output voltage as:

$$V_{in}^{max} = V_{O.PFC} \tag{12}$$

Even though the input voltage is regulated as constant by PFC pre-regulator, it drops during the hold-up time. The minimum input voltage considering the hold-up time requirement is given as:

$$V_{in}^{min} = \sqrt{V_{O.PFC}^2 - \frac{2P_{in}T_{HU}}{C_{DL}}} \tag{13}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, T_{HU} is a hold-up time, and C_{DL} is the DC link bulk capacitor.

(Design Example) Assuming the efficiency is 92%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{100}{0.92} = 109W$$

$$V_{in}^{max} = V_{O.PFC} = 400V$$

$$V_{in}^{min} = \sqrt{V_{O.PFC}^2 - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

$$= \sqrt{400^2 - \frac{2 \cdot 109 \cdot 30 \times 10^{-3}}{240 \times 10^{-6}}} = 364V$$

[STEP-2] Determine Maximum and Minimum Voltage Gains of the Resonant Network

As discussed in the previous section, it is typical to operate the LLC resonant converter around the resonant frequency (f_o) to minimize switching frequency variation. Since the input of the LLC resonant converter is supplied from PFC output voltage, the converter should be designed to operate at f_o for the nominal PFC output voltage.

As observed in Equation (10), the gain at f_o is a function of m ($m=L_p/L_r$). The gain at f_o is determined by choosing that value of m. While a higher peak gain can be obtained with a small m value, too small m value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set m to be 3~7, which results in a voltage gain of 1.1~1.2 at the resonant frequency (f_o).

With the chosen m value, the voltage gain for the nominal PFC output voltage is obtained as:

$$M^{\min} = \sqrt{\frac{m}{m-1}} \quad @f=f_o \tag{14}$$

which would be the minimum gain because the nominal PFC output voltage is the maximum input voltage (V_{in}^{max}).

The maximum voltage gain is given as:

$$M^{\max} = \frac{V_{in}^{max}}{V_{in}^{min}} M^{\min} \tag{15}$$

(Design Example) The ratio (m) between L_p and L_r is chosen as 5. The minimum and maximum gains are obtained as:

$$M^{\min} = \frac{V_{RO}}{V_{in}^{max}/2} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{5}{5-1}} = 1.12$$

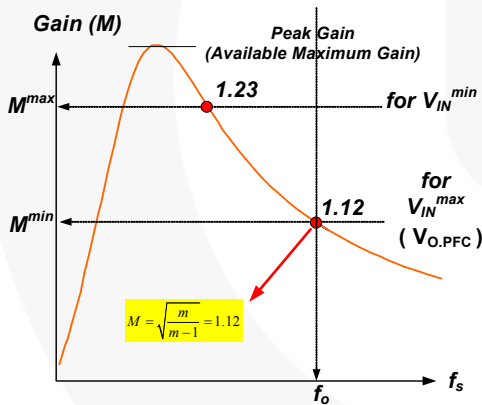$$M^{\max} = \frac{V_{in}^{max}}{V_{in}^{min}} m^{\min} = \frac{400}{364} \cdot 1.12 = 1.23$$

Figure 18. Maximum Gain / Minimum Gain

[STEP-3] Determine the Transformer Turns Ratio (n=N$_p$/N$_s$)

With the minimum gain (M^{min}) obtained in STEP-2, the transformer turns ratio is given as:

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{max}}{2(V_o + V_F)} \cdot M^{\min} \tag{16}$$

where V_F is the secondary-side rectifier diode voltage drop.

(Design Example) assuming V_F is 0.9V,

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{max}}{2(V_O + V_F)} \cdot M_{\min} = \frac{400}{2(100 + 0.9)} \cdot 1.12 = 2.22$$

[STEP-4] Calculate Equivalent Load Resistance

With the transformer turns ratio obtained from Equation (16), the equivalent load resistance is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} \tag{17}$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{(V_o + V_F)^2}{P_o} = \frac{8 \cdot 2.22^2 \cdot 100.9^2}{\pi^2 \cdot 100} = 405\Omega$$

[STEP-5] Design the Resonant Network

With m value chosen in STEP-2, read proper Q value from the peak gain curves in Figure 14 that allows enough peak gain. Considering the load transient and stable zero-voltage-switching (ZVS) operation, 10~20% margin should be introduced on the maximum gain when determining the peak gain. Once the Q value is determined, the resonant parameters are obtained as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} \tag{18}$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} \tag{19}$$

$$L_p = m \cdot L_r \tag{20}$$

(Design Example)
From STEP-2, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{in}^{min}) is 1.23. With 15% margin, a peak gain of 1.41 is required. m has been chosen as 5 in STEP-2 and Q is obtained as 0.42 from the peak gain curves in Figure 19. By selecting the resonant frequency as 100kHz, the resonant components are determined as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = \frac{1}{2\pi \cdot 0.42 \cdot 100 \times 10^3 \cdot 405} = 9.35nF$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \times 100 \times 10^3)^2 \cdot 9.35 \times 10^{-9}} = 271\mu H$$
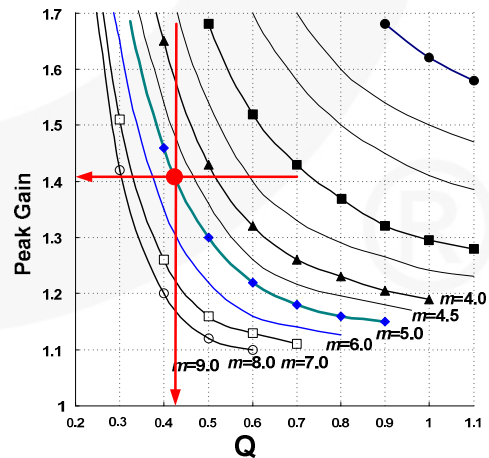
$$L_p = m \cdot L_r = 1355\mu H$$

Figure 19. Resonant Network Design Using the Peak Gain (Attainable Maximum Gain) Curve for m=5

[STEP-6] Design the Transformer

The worst case for the transformer design is the minimum switching frequency condition, which occurs at the minimum input voltage and full-load condition. To obtain the minimum switching frequency, plot the gain curve using gain Equation 9 and read the minimum switching frequency. The minimum number of turns for the transformer primary-side is obtained as:

$$N_p^{\ min} = \frac{n(V_o + V_F)}{2f_s^{\ min} \cdot M_V \cdot \Delta B \cdot A_e} \qquad (21)$$

where A_e is the cross-sectional area of the transformer core in m^2 and ΔB is the maximum flux density swing in Tesla, as shown in Figure 20. If there is no reference data, use ΔB =0.3~0.4 T.
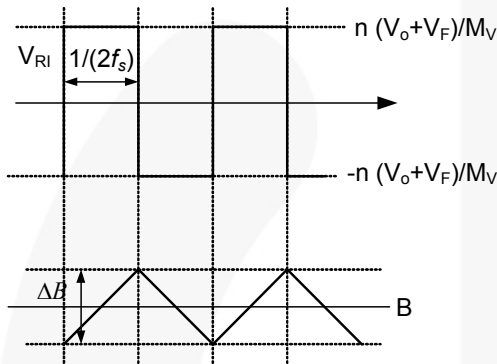
Figure 20. Flux Density Swing

Choose the proper number of turns for the secondary side that results in primary-side turns larger than N$_p$^{min} as:

$$N_p = n \cdot N_s > N_p^{\ min} \qquad (22)$$

(Design Example) EER3542 core (A$_e$=107mm^2) is selected for the transformer. From the gain curve of Figure 21, the minimum switching frequency is obtained as 70KHz. The minimum primary-side turns of the transformer is given as:

$$N_p^{\ min} = \frac{n(V_o + V_F)}{2f_s^{\ min}\Delta B \cdot 1.11 \cdot A_e}$$

$$= \frac{2.22 \times 100.9}{2 \times 80 \times 10^3 \cdot 0.4 \cdot 1.11 \cdot 107 \times 10^{-6}} = 30\ turns$$

Choose N$_s$ so that the resultant N$_p$ is larger than N$_p$^{min}:

$$N_p = n \cdot N_s = 2.22 \times 13 = 29 < N_p^{\ min}$$

$$N_p = n \cdot N_s = 2.22 \times 14 = 31 > N_p^{\ min}$$

$$N_p = n \cdot N_s = 2.22 \times 15 = 33 > N_p^{\ min}$$

$$N_p = n \cdot N_s = 2.22 \times 16 = 36 > N_p^{\ min}$$

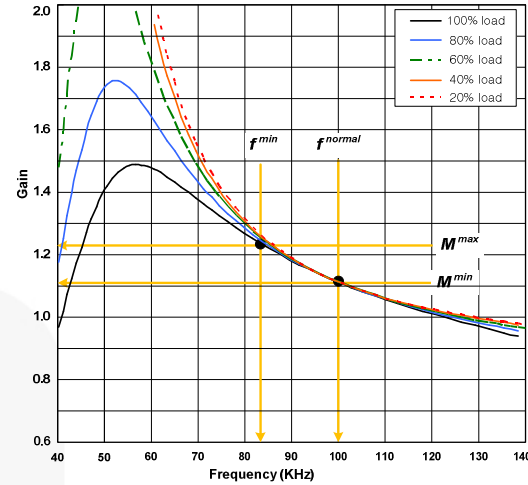$$N_p = n \cdot N_s = 2.22 \times 17 = 38 > N_p^{\ min}$$

Figure 21. Gain Curve

[STEP-7] Transformer Construction

Parameters L_p and L_r of the transformer were determined in STEP-5. L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively. Since LLC converter design requires a relatively large L_r, a sectional bobbin is typically used, as shown in Figure 22, to obtain the desired L_r value. For a sectional bobbin, the number of turns and winding configuration are the major factors determining the value of L_r, while the gap length of the core does not affect L_r much. L_p can be controlled by adjusting the gap length. Table 2 shows measured L_p and L_r values with different gap lengths. A gap length of 0.05mm obtains values for L_p and L_r closest to the designed parameters.
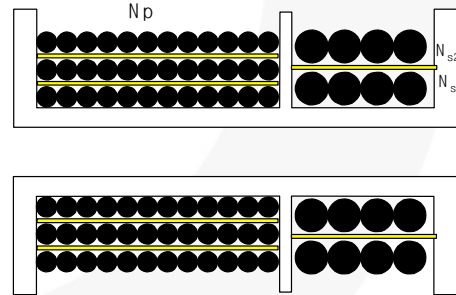
Figure 22. Sectional Bobbin

**Table 2. Measured L$_r$ and L$_r$ with Different Gap Lengths**

Gap Length	Lp	Lr
0.0mm	2,295μH	123μH
0.05mm	943μH	122μH
0.10mm	**630μH**	**118μH**
0.15mm	488μH	117μH
0.20mm	419μH	115μH
0.25mm	366μH	114μH

(Design Example)

Final Resonant Network Design

Even though the integrated transformer approach in LLC resonant converter design can implement the magnetic components in a single core and save one magnetic component, the value of L_r is not easy to control in real transformer design. Resonant network design sometimes requires iteration with a resultant L_r value after the transformer is built. The resonant capacitor value is also changed since it should be selected among off-the-shelf capacitors. The final resonant network design is summarized in Table 3 and the new gain curves are shown in Figure 23.

Table 3. Final Resonant Network Design Parameters

Parameters	Initial Design	Final Design
L_p	1365μH	**850μH**
L_r	273H	**170μH**
C_r	9.3nF	**15nF**
f_o	100kHz	**99.7kHz**
m	5	**5**
Q	0.42	**0.26**
M@f_o	1.12	**1.12**
Minimum Frequency	80kHz	**80kHz**
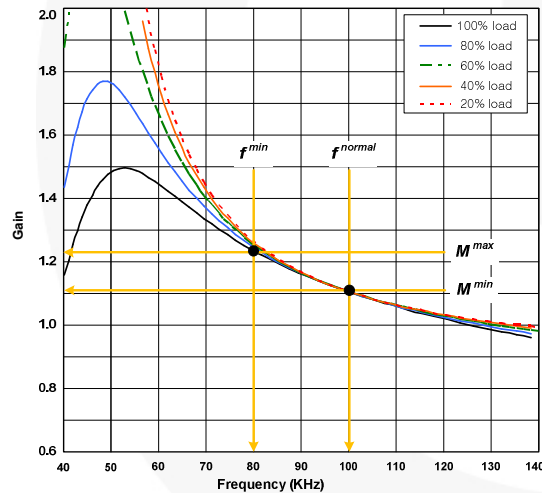
Figure 23. Gain Curve of the Final Resonant Network Design

[STEP-8] Select the Resonant Capacitor

When choosing the resonant capacitor, the current rating should be considered because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor is given as:

$$I_{C_r}{}^{RMS} \cong \frac{1}{E_{ff}} \sqrt{[\frac{\pi I_o}{2\sqrt{2}n}]^2 + [\frac{n(V_o + V_F)}{4\sqrt{2}f_o M_V (L_p - L_r)}]^2} \quad (23)$$

The nominal voltage of the resonant capacitor in normal operation is given as:

$$V_{C_r}{}^{nom} \cong \frac{V_{in}{}^{max}}{2} + \frac{\sqrt{2} \cdot I_{Cr}{}^{RMS}}{2 \cdot \pi \cdot f_o \cdot C_r} \quad (24)$$

However, the resonant capacitor voltage increases much higher at overload condition or load transient. Actual capacitor selection should be based on the Over-Current Protection (OCP) trip point. With the OCP level, I_{OCP}, the maximum resonant capacitor voltage is obtained as:

$$V_{C_r}{}^{nom} \cong \frac{V_{in}{}^{max}}{2} + \frac{I_{OCP}}{2 \cdot \pi \cdot f_o \cdot C_r} \quad (25)$$

(Design Example)

$$I_{C_r}{}^{RMS} \cong \frac{1}{E_{ff}} \sqrt{[\frac{\pi I_O}{2\sqrt{2}n}]^2 + [\frac{n(V_o + V_F)}{4\sqrt{2}f_o M_v (L_p - L_r)}]^2}$$

$$= \frac{1}{0.92} \sqrt{[\frac{\pi \cdot 1}{2\sqrt{2} \cdot 2.22}]^2 + [\frac{2.22(100 + 0.9)}{4\sqrt{2} \cdot 99 \times 10^3 \cdot 1.12 \cdot 680 \times 10^{-6}}]^2}$$

$$= 0.78A$$

The peak current in the primary side in normal operation is:
$$I_{C_r}{}^{peak} = \sqrt{2} \cdot I_{C_r}{}^{rms} = 1.103A$$

OCP level is set to 1.75A with 50% margin on $I_{Cr}{}^{peak}$:

$$V_{C_r}{}^{nom} \cong \frac{V_{in}{}^{max}}{2} + \frac{\sqrt{2} \cdot I_{C_r}{}^{RMS}}{2 \cdot \pi \cdot f_o \cdot C_r}$$

$$= \frac{400}{2} + \frac{\sqrt{2} \cdot 0.78}{2 \cdot \pi \cdot 99 \times 10^3 \cdot 15 \times 10^{-9}} = 318V$$

$$V_{C_r}{}^{max} \cong \frac{V_{in}{}^{max}}{2} + \frac{I_{OCP}}{2 \cdot \pi \cdot f_o \cdot C_r}$$

$$= \frac{400}{2} + \frac{1.75}{2 \cdot \pi \cdot 99 \times 10^3 \cdot 15 \times 10^{-9}} = 387.7V$$

A 630V rated low-ESR film capacitor is selected for the resonant capacitor.

[STEP-9] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice of the output voltage expressed as:

$$V_D = 2(V_o + V_F) \quad (26)$$

The RMS value of the current flowing through each rectifier diode is given as:

$$I_D{}^{RMS} = \frac{\pi}{4} I_o \quad (27)$$

Meanwhile, the ripple current flowing through output capacitor is given as:

$$I_{Co}{}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o{}^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o \quad (28)$$

The voltage ripple of the output capacitor is:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C \tag{29}$$

where R_C is the effective series resistance (ESR) of the output capacitor and the power dissipation is the output capacitor is:

$$P_{Loss.Co} = (I_{Co}{}^{RMS})^2 \cdot R_C \tag{30}$$

(Design Example) The voltage stress and current stress of the rectifier diode are:

$$V_D = 2(V_o + V_F) = 2(100 + 0.9) = 201.8V$$

$$I_D{}^{RMS} = \frac{\pi}{4} I_o = 0.785A$$

The 600V/8A Ultra fast recovery diode is selected for the rectifier, considering the voltage overshoot caused by the stray inductance.

The RMS current of the output capacitor is:

$$I_{C_o}{}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o{}^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 0.48A$$

When two electrolytic capacitors with ESR of 100mΩ are used in parallel, the output voltage ripple is given as:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C = \frac{\pi}{2} \cdot 1 \cdot (\frac{0.1}{2}) = 0.079V$$

The loss in electrolytic capacitors is:

$$P_{Loss,C_o} = (I_{C_o}{}^{RMS})^2 \cdot R_C = 0.48^2 \cdot 0.05 == 0.01W$$

[STEP-10] Control Circuit Configuration

Figure 24 shows the typical circuit configuration for the RT pin of FLS-XS series, where the opto-coupler transistor is connected to the RT pin to control the switching frequency. The minimum switching frequency occurs when the opto-coupler transistor is fully tuned off, which is given as:

$$f_{min} = \frac{5.2k\Omega}{R_{min}} \times 100 (kHz) \tag{31}$$

Assuming the saturation voltage of the opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f_{max} = (\frac{5.2k\Omega}{R_{min}} + \frac{4.68k\Omega}{R_{max}}) \times 100 (kHz) \tag{32}$$
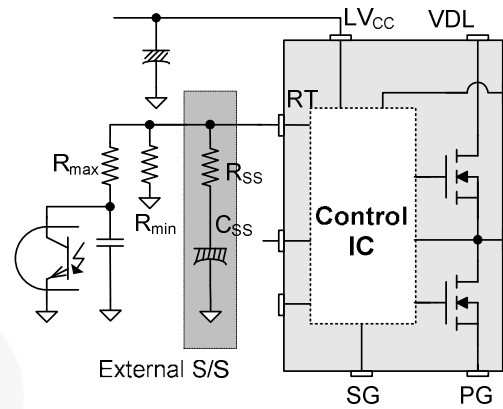

Figure 24. Typical Circuit Configuration for RT Pin

Soft-Start To prevent excessive inrush current and overshoot of output voltage during startup, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is reversely proportional to the switching frequency, soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established, as illustrated in Figure 25. The soft-start circuit is made by connecting RC series network on the RT pin as shown in Figure 24. FLS-XS series also has an internal soft-start for 3ms to reduce the current overshoot during the initial cycles, which adds 40KHz to the initial frequency of the external soft-start circuit, as shown in Figure 25. The actual initial frequency of the soft-start is given as:

$$f^{ISS} = (\frac{5.2k\Omega}{R_{min}} + \frac{5.2k\Omega}{R_{SS}}) \times 100 + 40 \ (kHz) \tag{33}$$

It is typical to set the initial frequency of soft-start (f^{ISS}) as 2~3 times of the resonant frequency (f_o).

The soft-start time is determined by the RC time constant:

$$T_{SS} = 3 \sim 4 \ times \ of \ R_{SS} \cdot C_{SS} \tag{34}$$
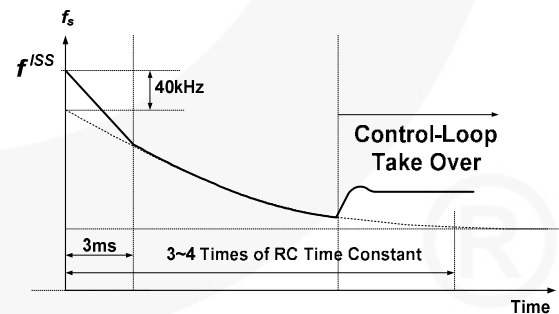

Figure 25. Frequency Sweep of the Soft-Start

(Design Example) The minimum frequency is 80kHz in STEP-6. R_{min} is determined as:

$$R_{min} = \frac{100KHz}{f_{min}} \times 5.2K\Omega = 6.5K\Omega$$

Considering the output voltage overshoot during transient (10%) and the controllability of the feedback loop, the maximum frequency is set as 140kHz. R_{max} is determined as:

$$R_{max} = \frac{4.68K\Omega}{(\frac{f_o \times 1.40}{100KHz} - \frac{5.2K\Omega}{R_{min}})}$$

$$= \frac{4.68K\Omega}{(\frac{99KHz \times 1.40}{100KHz} - \frac{5.2K\Omega}{6.5K\Omega})} = 7.8K\Omega$$

Setting the initial frequency of soft-start as 250kHz (2.5 times of the resonant frequency), the soft-start resistor R_{SS} is given as:

$$R_{SS} = \frac{5.2K\Omega}{(\frac{f_{ISS} - 40KHz}{100KHz} - \frac{5.2K\Omega}{R_{min}})}$$

$$= \frac{5.2K\Omega}{(\frac{250KHz - 40KHz}{100KHz} - \frac{5.2K\Omega}{6.5K\Omega})} = 4K\Omega$$

[STEP-11] Current Sensing and Protection

FLS-XS series senses low-side MOSFET drain current as a negative voltage, as shown in Figure 26 and Figure 27. Half-wave sensing allows low-power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal. Typically, RC low-pass filter is used to filter out the switching noise in the sensing signal. The RC time constant of the low-pass filter should be 1/100~1/20 of the switching period.
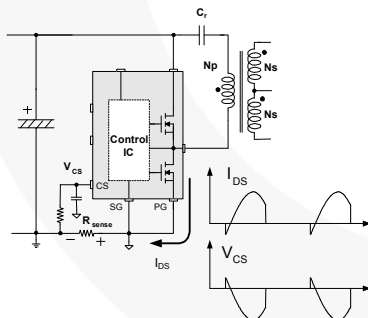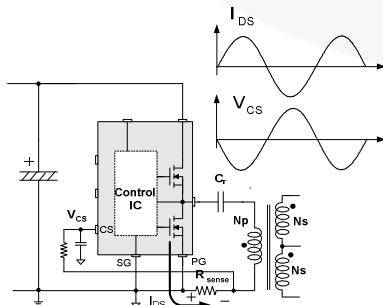

Figure 26. Half-Wave Sensing

Figure 27. Full-Wave Sensing

(Design Example) Since the OCP level is determined as 1.75A in STEP-8 and the OCP threshold voltage is -0.6V, a sensing resistor of 0.33Ω is used. The RC time constant is set to 100ns (1/100 of switching period) with 1kΩ resistor and 100pF capacitor.

[STEP-12] Voltage and Current Feedback

Power supplies for LED lighting must be controlled by Constant Current (CC) Mode as well as a Constant Voltage (CV) Mode. Because the forward-voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged. Figure 28 shows an example of a CC and CV Mode feedback circuit for single output LED power supply. During normal operation, CC Mode is dominant and CV control circuit does not activate as long as the feedback voltage is lower than reference voltage, which means that CV control circuit only acts as OVP for abnormal modes.

(Design Example) The output voltage (V_O) is 100V in design target. V_O is determined as:

$$V_o = 2.5(1 + \frac{R_{FU}}{R_{FL}})$$

Set the upper-side feedback resistance (R_{FU}) as 330KΩ. R_{FL} is determined as:

$$R_{FL} = \frac{2.5 \times R_{FU}}{(V_o - 2.5)} = \frac{2.5 \times 330K\Omega}{(100 - 2.5)} = 8.46K\Omega$$

The output voltage of op-amp is given as:

$$0 = \frac{\frac{V_{sense}}{R201} + \frac{V_{REF}}{R203} + sC201 \cdot V_{OC}}{\frac{1}{R201} + \frac{1}{R203} + sC201}$$

$$V_{OC} = -\frac{1}{sC201}(\frac{V_{sense}}{R201} + \frac{V_{REF}}{R203})$$

Actually, the V_{sense} has a negative value and assume all resistors have the same value for simplification;

$$V_{OC} = -\frac{1}{sC201 \times R}(V_{sense} - V_{REF})$$

The output voltage of the op-amp for CC control keeps zero voltage as long as the sensing voltages are lower than the reference voltage.

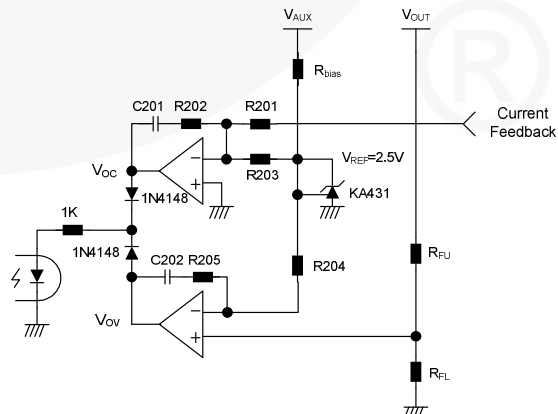**Figure 28. Example of CC and CV Feedback Circuit**

Figure 29 shows another example of a CC and Over-Voltage Regulation (OVR) Mode feedback circuit for multi-output LED power supply. The FAN7346 is a LED current-balance controller that controls four LED arrays to maintain equal LED current. To prevent LED driving voltage being over the withstanding voltage of component, the FAN7346 controls LED driving voltage. The OVR control circuit activates when the ENA pin is in HIGH state. If OVR pin voltage is lower than 1.5V, the Feedback Control (FB) pin voltage follows headroom control to maintain minimum voltage of drain voltages as 1V. If OVR pin voltage is higher than 1.5V, the FAN7346 controls FB (FB is pulled LOW) through FB regulation so the OVR pin voltage is not over 1.5V.

LED current is controlled by FBx pin voltage. The external current balance switch is operating in linear region to control LED current. Sensed voltage at the FBx pin is compared with internal reference voltage and controller signals the gate (or base) for external current balance switch. Internal reference voltage is made from ADIM voltage. The LED current is determined as:

$$I_{LED} = \frac{V_{ADIM}}{10 \times R_{SENSE}} \quad (35)$$

ADIM voltage is clamped internally from 0.5V to 4V. The protections; such as open LED Protection (OLP), Short LED Protection (SLP), and Over-Current Protection (OCP); which increase system reliability, are applied in individual string protection method.

To sense a short LED condition, the FAN7346 senses drain voltage level. If LEDs are shorted, the LED forward voltage is lower than other LED strings, so its drain voltage of external balance switch is higher than other drain voltage. The SLP condition detection threshold voltage can be programmed by SLPR voltage. The internal short LED protection reference is determined as:

$$V_{SLP\_TH} = 10 \times V_{SLPR} \quad (36)$$

Minimum SLP threshold voltage is 0V and maximum SLP threshold voltage is 45V. If any string is in SLP condition, SLP string is turned off and other string is operated normally. If the sensed drain voltage (CHx voltage) is higher than the programmed threshold voltage for 20µs, CHx goes to short LED protection. As soon as encountering SLP, the corresponding channel is forced off.

To sense an open LED condition, the FAN7346 senses drain voltage level. If LED string is opened, its drain voltage of external balance switch is grounded, so the FAN7346 detects the open-LED condition. The detection threshold voltage is 0.3V. If CHx voltage is lower than 0.3V for 20µs, its drain voltage feedback is pulled up to 5V. This means the opened LED string is eliminated from drain feedback loop. Without OLP, minimum drain voltage is 0V, so drain voltage feedback forces the FB signal to increase output power. This can cause SLP or thermal

stress problems in the other channel. OLP function has auto-recovery: As soon as drain voltage is higher than 0.3V, OLP is finished and drain voltage feedback system is restored.

To sense over-current condition, the FAN7346 monitors FBx pin voltage. If FBx voltage is higher than 1V for 20µs, CHx is considered in over-current condition. After sensing OCP condition, individual channel switch is latched off. So, even if a channel is in OCP condition, other channels keep operating. Any OCP channel is restarted after UVLO is reset.

(Design Example) The output voltage (V_O) is 100V in design target. V_O is determined as:

$$V_o = 1.5(1 + \frac{R8}{R10})$$

Set the upper-side feedback resistance (R8) as 1MΩ. R10 is determined as:

$$R10 = \frac{1.5 \times R8}{(V_o - 1.5)} = \frac{1.5 \times 1M\Omega}{(100 - 1.5)} = 15.23K\Omega$$

The output channel current (I_{LED}) is 250mA in design target. Setting the V_{ADIM} is above 4V, the current sense R_{SENSE} is determined as:

$$R_{SENSE} = \frac{V_{ADIM}}{10 \times I_{LED}} = \frac{4V}{10 \times 250mA} = 1.6\Omega$$

Choose the sense resistor (R29, R30, R31, and R32) is 1.5 Ω, the OCP level is determined as:

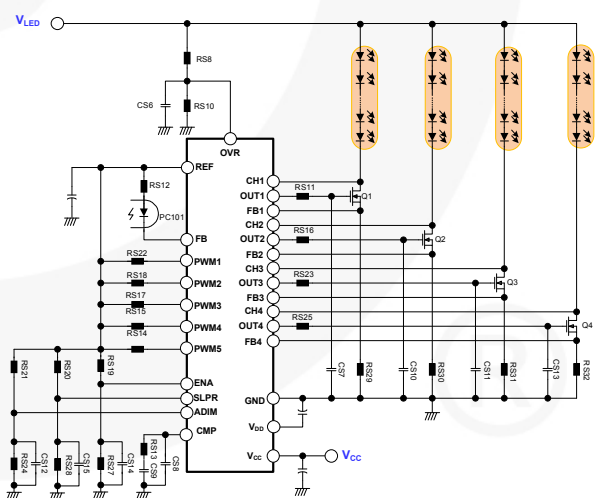$$I_{OCP} = \frac{V_{OCP\_TH}}{R_{SENSE}} = \frac{1V}{1.5\Omega} = 666mA$$

Figure 29. Example of CC and OVR Feedback Circuit

Design Summary

Figure 30 and Figure 31 show the final schematic of the LLC resonant half-bridge converter for LED lighting design example. EER3543 core with sectional bobbin is used for the transformer. Efficiency at full-load is around 94%.
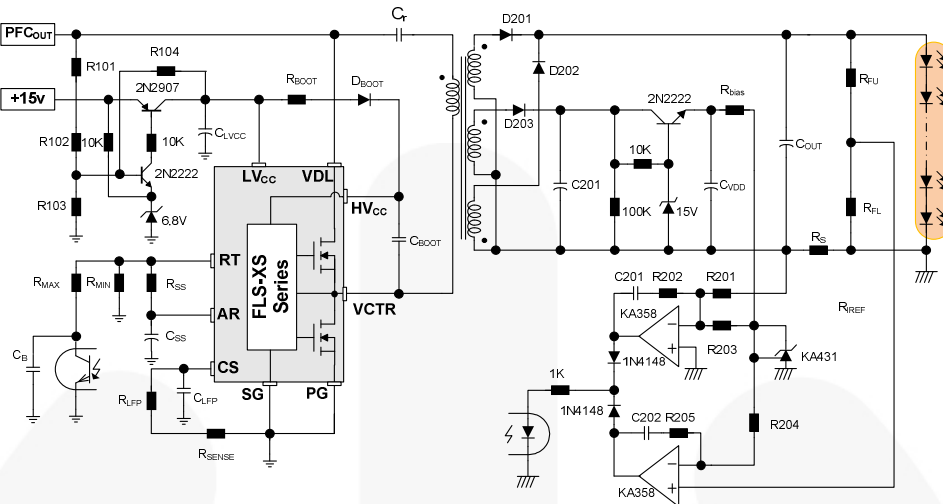

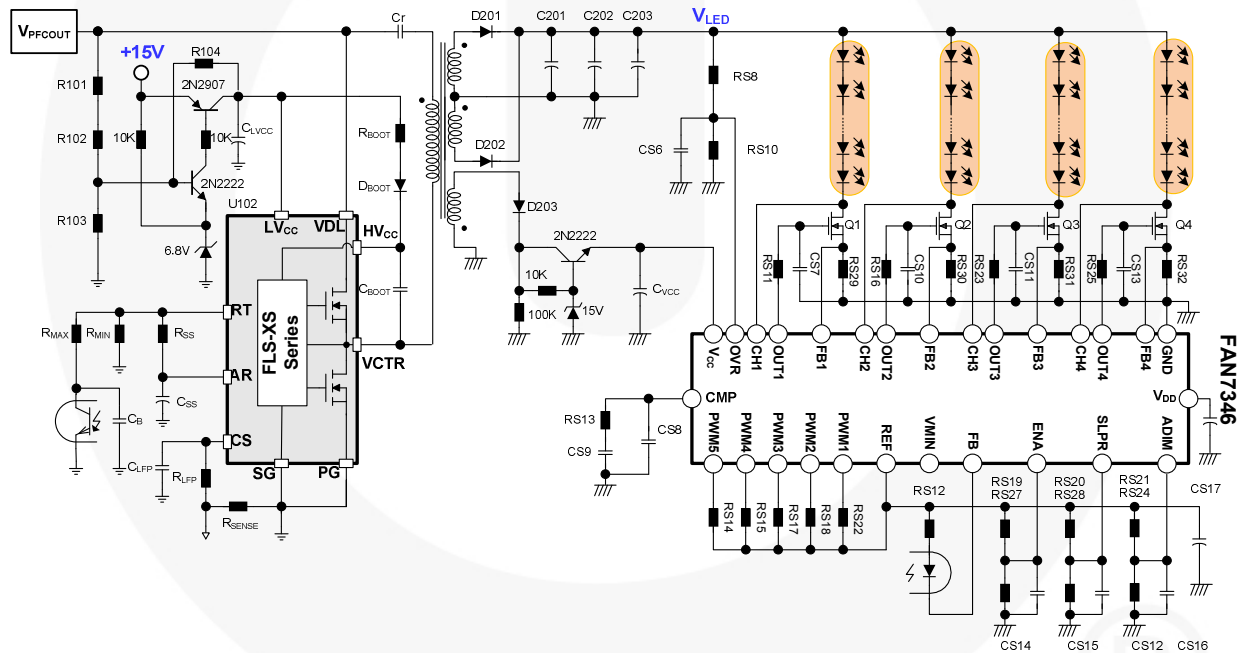**Figure 30. Final Schematic of Half-Bridge LLC Resonant Converter for Single Channel**

Figure 31. Final Schematic of Half-Bridge LLC Resonant Converter for Multi Channel

Experimental Verification

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are used as designed in the design example.

Figure 32 and Figure 33 show the operation waveforms at full-load and no-load conditions for nominal input voltage. As observed, the MOSFET drain-to-source voltage (V_{DS}) drops to zero by resonance before the MOSFET is turned on and zero voltage switching is achieved.

Figure 34 shows the waveforms of the resonant capacitor voltage and primary-side current at full-load condition. The peak values of the resonant capacitor voltage and primary-side current are 300V and 1.1A, respectively, which are well matched with the calculated values in STEP-8 of design procedure section.

Figure 35 shows the rectifier diode voltage and current waveforms at full-load condition. Due to the voltage overshoot caused by stray inductance, the voltage stress is a little bit higher than the value calculated in STEP-9.

Figure 36 shows the output load current and output voltage of op-amp waveforms for constant-current control when output load is step changed from 140mA to 1000mA at t_0.

Figure 37 shows the operation waveform when LED string is opened and restored condition
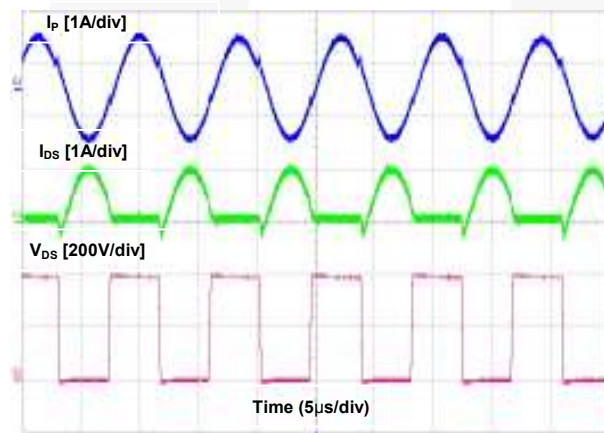
Figure 32. Operation Waveforms at Full-Load Condition
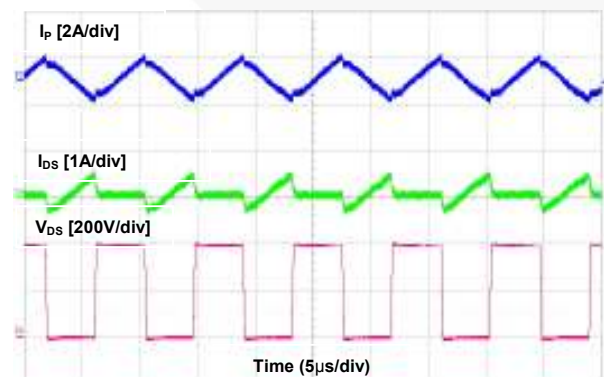
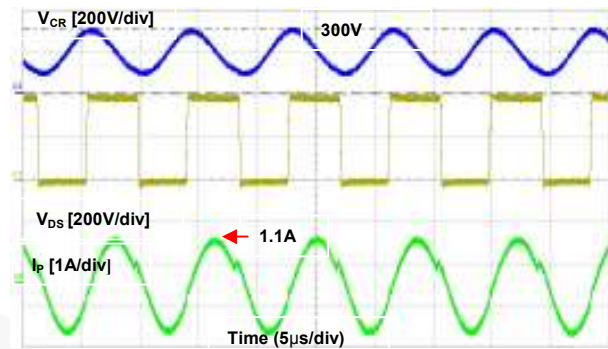**Figure 33. Operation Waveforms at No-Load Condition**

Figure 34. Resonant Capacitor Voltage and Primary-Side Current Waveforms at Full-Load Condition
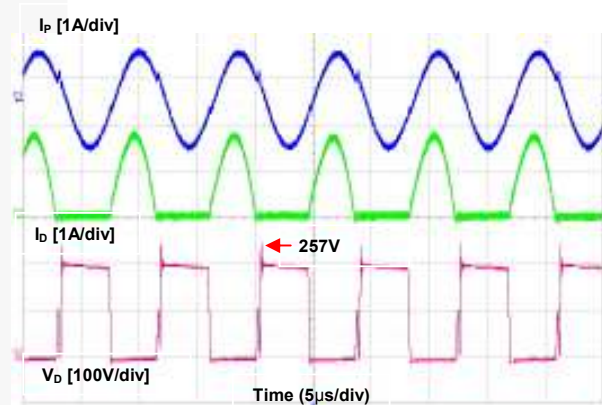

Figure 35. Rectifier Diode Voltage and Current Waveforms at Full-Load Condition
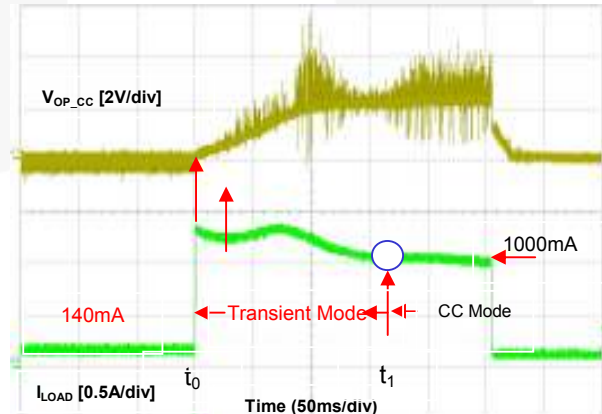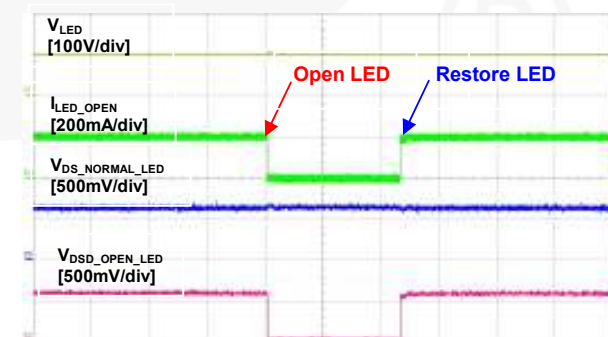

Figure 36. Soft-Start Waveforms

Figure 37. Open LED Protection Operation

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This application note written based on Fairchild Semiconductor Application Note AN-4137.

Related Datasheets

FLS1800XS — Half-Bridge LLC Resonant Control IC for Lighting

FLS2100XS — Half-Bridge LLC Resonant Control IC for Lighting

FAN7346 — 4-Channel LED Current Balance Control IC