

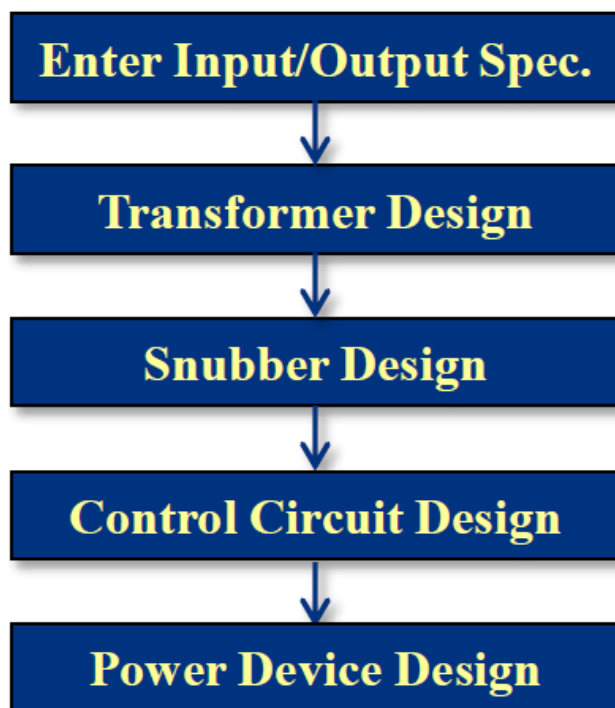


AN-7732

FL7732 Design Tool Flow (Flyback)

Overview

This document is intended to provide in-depth guidance to using the Fairchild Design Tool for FL7732. Use the Design Tool with the product datasheet.



Flyback Design

Figure 1. Design Flow

Step 1 — Enter Input Output Specification

Input
Output

Blue box is input from user.
Red box is calculated output.

Input Spec			
Min. Vin	90	Vac	
Max. Vin	140	Vac	
Output Spec			
Vout	22	V	
Max. Vout	28	V	
Iout	380	mA	
Pout	8.36	W	

Max. Vout is OVP level.

Step 2 — Transformer Design

Transformer Design		
Max. Duty	39	%
Max. Ton	6.500	us
Switching freq.	60	kHz
Max. Vcs	0.5	V
Efficiency	80	%
Ae	36.6	mm ²
Bmax	0.3	
Lm	0.982	mH
Nps	3.223	
Nas	0.821	
Nap	0.255	
Np.min	75.347	T
Np	76	T
Ns	23.578	T
Na	19.368	T
Llk	10	uH

Max. duty is generally between 20 ~ 50%.

High max. duty = · Low conduction loss, Suitable for low-line

Low max. duty = · More Bmax margin, Suitable for high-line

Max. Ton should be less than 10us.

This switching frequency is the operating frequency at the rated Vout condition.

The switching frequency should be less than 65kHz.

Max. Vcs is max. peak CS voltage.

Enter Max. Vcs less than 0.67V because pulse by pulse CS voltage limit is 0.67V.

Higher Nps makes higher max. Vcs in the primary side CC regulation.

So, when max. Vcs is highly set, Nps becomes higher.

Enter Np over Np.min.

If Np is too big to fit in transformer window, reduce Max. Duty.

Make transformer according to the above spec.

Then, enter Llk (Leakage inductance) after measuring.

Step 3 — Snubber Design

Snubber Design		
V _{sn}	200	V
ΔV _{sn}	5	V
R _{sn}	242.7247	kohm
C _{sn}	2.746596	nF

V_{sn} is snubber voltage.

V_{sn} is generally set as 2~2.5 times N_{ps}·V_o.

ΔV_{sn} is generally set as 5% ripple of V_{sn}.

Step 4 — Control Circuit Design

Control Circuit Design		
R _{sense}	0.593767	ohm
R _{cc}	100	ohm
V _{in.bnk}	50	V
V _f	0.5	V
R _{vs1}	165.2367	kohm
R _{vs2}	19.75502	kohm
C _{vs}	10	pF
C _{comi}	1	uF
C _{vdd}	33	uF
D _{vdd} V _{max}	73.95584	V
R _{str}	155.8442	kohm

R_{cc} is line CC compensation resistor.

When I_{out} becomes higher at higher input voltage, increase R_{cc}.

R_{cc} should be limited less than 500ohm.

Large R_{cc} can make CS noise, inducing V_{cs} peak detection error.

V_{in.bnk} is VS blanking level.

VS blanking : VS voltage detection is disabled.

V_{in.bnk} is generally set as 30~70V.

V_f is secondary diode forward voltage.

C_{vs} is VS filter capacitor, generally set as 10~30pF.

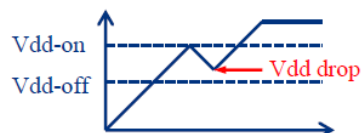
C_{comi} capacitor is generally 0.68~3.3uF.

Check output voltage overshoot at startup in max. V_{in} condition.

If output voltage overshoot is too big, increase C_{comi}.

V_{dd} capacitor is generally in 10~47uF.

If V_{dd} drops too close to V_{dd-off} at startup, increase C_{vdd}.



Step 5 — Power Device Design

Power Device Design		
MOSFET V _{max}	397.9899	V
MOSFET I _{pk}	0.842082	A
Diode V _{max}	89.4245	V
Diode I _{pk}	2.714286	A

V_{max} is MOSFET drain-source maximum voltage.

I_{pk} is MOSFET peak current.

V_{max} is maximum reverse voltage of secondary diode.

I_{pk} is peak current of secondary diode.

Related Resources

Locate the Design Tool at:

http://www.fairchildsemi.com/design_tools/led-driver-design-tool/

Consult the product datasheet at:

[*FL7732 —Single-Stage PFC Primary-Side-Regulation Offline LED Driver*](#)

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