Application Note AN6032

FAN4800 Combo Controller Applications

General Description

This application note shows the step-by-step process to design a high-performance supply. The equations shown in this document can also be used for different output voltages and total power.

The complete power supply circuits shown in Figures 6 and 7 demonstrate the FAN4800's ability to manage high output power while complying with international requirements regarding AC line quality. The PFC section provides $380V_{DC}$ to a dual-transistor current-mode forward converter. The output of the converter delivers +12V at up to 8.4 amps. The circuit operates from 85 to $265V_{AC}$ with both power sections switching at 100kHz.

The PFC Stage

Powering the FAN4800

The FAN4800 is initialized once C_{12} is charged to 13V through R_{27} and R_{28}. PFC switching action boosts the voltage on C_5 to 380V via L_1's inductance. T_2 then supplies a well-regulated 13V for the FAN4800 from its secondary winding. T_2's primary-to-secondary turns ratio (N_{PRI} / N_{SEC}) is 18.8:1. For proper circuit operation, high-frequency bypassing with low-ESR ceramic or film capacitors on V_{CC} and V_{REF} is provided. Orderly PFC operation upon start-up is achieved when D_2 quick charges the boost capacitor to the peak AC line voltage before the boost switch Q_1 is turned on. This ensures the boost inductor current is zero before

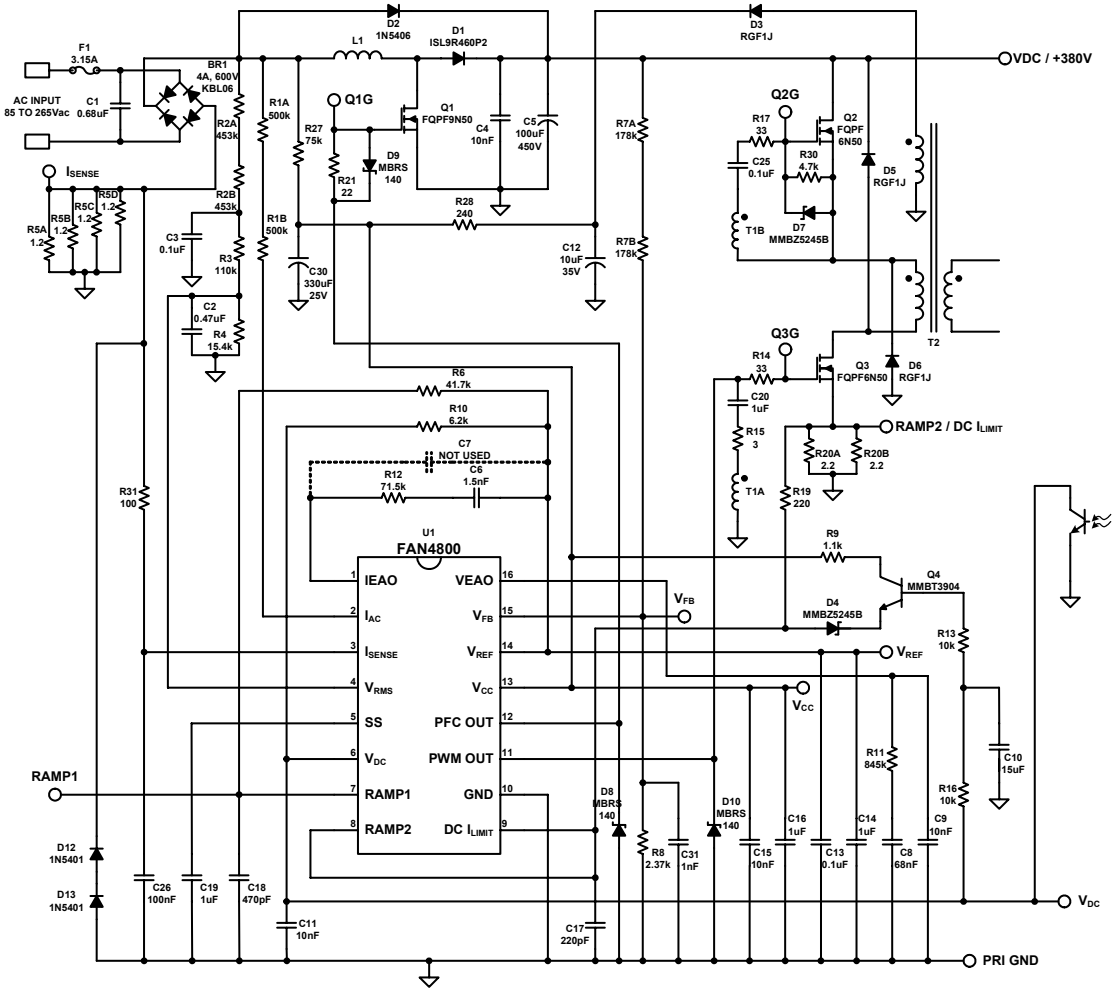

Figure 1. The PFC Stage

PFC action begins. The value of the regulated voltage on C_5 must always be greater than the peak value of the maximum line voltage delivered to the supply.

$$\begin{aligned} &V_{C5} > \sqrt{2}V_{in(\,rms\_max)} \\ &V_{C5} > (1.414)\times(265) \\ &V_{C5} > 375V \qquad use\ 380V \end{aligned} \tag{1}$$

Because the FAN4800 uses transconductance amplifiers, the loop compensation networks are returned to ground (see the FAN4800 datasheet for the error amplifier characteristics/ advantages). This eliminates the interaction of the resistive divider network with the loop compensation capacitors, permitting a wide choice of divider values chosen to minimize amplifier offset voltages due to input bias currents. For reliable operation, R_{7A} and R_{7B} must have a voltage rating of at least 400 volts.

Calculate the divider ratio $(R_{7A}+R_{7B})/R_8$ by:

$$\begin{aligned} &\frac{R_{7A}+R_{7B}}{R_8} = \frac{V_{C5}}{2.5} - 1 \\ &\frac{R_{7A}+R_{7B}}{R_8} = \frac{380}{2.5} - 1 \\ &\frac{R_{7A}+R_{7B}}{R_8} = 151 \end{aligned} \tag{2}$$

Selecting the Power Components

The FAN4800 PFC section operates with continuous inductor current to minimize peak current and to maximize available power. The boost inductor value found by setting ΔI, the peak-to-peak value of high-frequency current, is typically 10% to 20% of the peak value of the maximum line current.

$$I_{in(\,peak\_max)} = \frac{\sqrt{2}P_{in(max)}}{V_{in(\,rms\_min)}} \tag{3}$$

$$P_{in(max)} = \frac{P_{O(max)}}{\eta} \tag{4}$$

where $I_{in(peak\_max)}$ is a peak value of input current occurred at low line, $V_{in(rms\_min)}$ is RMS value of minimum line voltage, $P_{O(max)}$ is the maximum output power, and η is efficiency. Value $I_{in(peak\_max)}$ defines value of ΔI, where dI is the specified percentage rate. $I_{L(max)}$ is the inductor maximum current.

$$\Delta I = dI \times I_{in(\,peak\_max)} \tag{5}$$

$$I_{L(max)} = I_{in(\,peak\_max)} + \frac{\Delta I}{2}$$

Duty cycle D and switching frequency f_S influence inductor selection.

$$D = \frac{V_O - \sqrt{2}V_{in(\,rms\_min)}}{V_O} \tag{6}$$

$$\begin{aligned} L_1 &= \frac{D\times\sqrt{2}V_{in(\,rms\_min)}}{f_S\times\Delta I} \\ &= \frac{\left(V_O - \sqrt{2}V_{in(\,rms\_min)}\right)\cdot V_{in(\,rms\_min)}^{\,2}\cdot\eta}{V_O\cdot f_S\cdot dI\cdot P_{O(max)}} \\ &= \frac{\{380-(1.414)\cdot(85)\}\cdot(85)^2\cdot(0.95)}{(380)\cdot(1\times10^5)\cdot(0.15)\cdot(100)} \\ &= 3.128mH \qquad use\ 3.0mH \end{aligned} \tag{7}$$

The boost diode D_1 and switch Q_1 are chosen with a reverse voltage rating of 500V to safely withstand the 380V boost potential. The maximum Q_1 RMS current is obtained by Equation 8 and the maximum Q_1 peak current is calculated by Equation 9.

$$\begin{aligned} I_{Q1rms} &= \sqrt{2}I_{in(\,rms\_max)}\sqrt{\frac{1}{2} - \frac{4\sqrt{2}V_{in(\,rms\_min)}}{3\pi V_O}} \\ &= \frac{\sqrt{2}P_{O(max)}}{\eta V_{in(\,rms\_min)}}\sqrt{\frac{1}{2} - \frac{4\sqrt{2}V_{in(\,rms\_min)}}{3\pi V_O}} \\ &= \frac{(1.414)\cdot(100)}{(0.95)\cdot(85)}\sqrt{\frac{1}{2} - \frac{4\cdot(1.414)\cdot(85)}{3\cdot(3.1416)\cdot(380)}} \\ &= 1.06A \end{aligned} \tag{8}$$

$$\begin{aligned} I_{Q1peak} &= I_{in(\,peak\_max)} + \frac{\Delta I}{2} \\ &= \frac{\sqrt{2}P_{O(max)}}{\eta V_{in(\,rms\_min)}} + \frac{\left(V_O - \sqrt{2}V_{in(\,rms\_min)}\right)\cdot\sqrt{2}V_{in(\,rms\_min)}}{V_O\cdot f_S\cdot L_1} \\ &= \frac{(1.414)\cdot(100)}{(0.95)\cdot(85)} + \frac{\{380-(1.414)\cdot(85)\}\cdot(1.414)\cdot(85)}{(380)\cdot(1\times10^5)\cdot(3\times10^{-3})} \\ &= 2.025A \end{aligned} \tag{9}$$

The boost diode average current can be calculated by:

$$\begin{aligned} I_{D1avg} &= I_{O(max)} \\ &= \frac{P_{O(max)}}{V_O} \\ &= \frac{100}{380} = 0.26A \end{aligned} \tag{10}$$

The boost capacitor value is chosen to permit a given output voltage hold-up time in the event the line voltage is suddenly removed.

$$C_5 \geq \frac{2P_{O(max)}t_{HLD}}{V_{C5(NOM)}^{\,2} - V_{C5(MIN)}^{\,2}} \tag{11}$$

where:

t_{HLD} = hold-up time (sec)

$V_{C5(min)}$ = minimum voltage on C_5 at which the PWM stage can still deliver full output power

A key advantage of using leading/trailing-edge modulation is that a large portion of the inductor current is "dumped" directly into the load (PWM stage transformer) and not the boost capacitor. This relaxes the ESR requirement of the boost capacitor. For reference, Equation 12 should be used as a starting point when choosing C_5's maximum ripple current rating (at 120Hz).

$$I_{C5\_rms} = \frac{I_{O(C5)}}{\sqrt{2}} \quad (12)$$

$$\left(I_{peak} = \sqrt{2} \cdot I_{C5\_rms}\right) \quad (12a)$$

Selecting the Power Setting Components

The maximum average power delivered by the PFC stage is set using the following procedure:

1. Find the resistive divider ratio that results in the voltage at the V_{RMS} pin being equal to 1.14V at the lowest line voltage. The voltage at this pin must be well filtered, yet able to respond well to transient line voltage changes.

$$\frac{R_4}{R_{TOT}} = \frac{1.14 \cdot \pi}{2\sqrt{2}V_{in(rms\_min)}} \quad (13)$$

The resistor and capacitor values in the typical example were found empirically to offer the lowest ripple voltage and still respond well to line voltage changes. Should a ratio be required that is greatly different from that found in Equation 13, adjust the filter capacitor values according to Equations 14 and 15.

$$C_3 = \frac{R_{TOT}}{2\pi f_1 \cdot (R_{2A} + R_{2B}) \cdot (R_3 + R_4)} \quad (14)$$

$$C_2 = \frac{\left(1 + \frac{R_4 \cdot R_{TOT}}{(R_{2A} + R_{2B}) \cdot (R_3 + R_4)}\right)}{2\pi f_2 \cdot R_4} \quad (15)$$

where:

f_1 = 15Hz, f_2 = 23Hz

$R_{TOT} = R_{2A} + R_{2B} + R_3 + R_4$

2. Find the constant of proportionality k_M of the multiplier gain k in Equation 16a. To obtain "brownout" action below the lowest input voltage, the maximum gain of the multiplier must be used when finding k_M. The maximum gain (0.35) occurs when the V_{RMS} input of the multiplier is 1.14V. Equation 16 is the general expression for the multiplier gain versus the line voltage.

$$k = \frac{k_M}{V_{rms}^2} \quad (16)$$

$$k_M = kV_{in(rms\_min)}^2 \quad (16a)$$

$$= (0.35) \cdot (85)^2$$

$$= 2528.75 \approx 2529$$

3. Select the value of (R_{1A}+R_{1B}) that permits the greatest multiplier output current without saturating the output. The maximum output current of the multiplier is 228.57µA.

$$(R_{1A} + R_{1B}) \geq \frac{k\sqrt{2}V_{in(rms\_min)}\left(V_{EAO(max)} - 0.625\right)}{228.57 \times 10^{-6}}$$

$$(R_{1A} + R_{1B}) \geq \frac{(0.35) \cdot (1.414) \cdot (85)(6 - 0.625)}{228.57 \times 10^{-6}} \quad (17)$$

$$(R_{1A} + R_{1B}) \geq 989.38k\Omega \qquad use\ 1M\Omega$$

4. Select the value of the current sense resistor to complete the calculations for the power setting components.

$$R_{5A} \,||\, R_{5B} \,||\, R_{5C} \,||\, R_{5D} \leq \frac{R_{MULO} \cdot k_M \left(V_{EAO(max)} - 0.625\right) \cdot \eta}{P_{O(max)} (R_{1A} + R_{1B})} \quad (18)$$

$$R_{5A} \,||\, R_{5B} \,||\, R_{5C} \,||\, R_{5D} \leq \frac{\left(3.5 \times 10^3\right) \cdot (2529)(6 - 0.625) \cdot (0.95)}{(100)\left(1 \times 10^6\right)}$$

$$R_{5A} \,||\, R_{5B} \,||\, R_{5C} \,||\, R_{5D} \leq 0.452\Omega \qquad use\ 0.3\Omega$$

where:

R_{MULO} = multiplier output termination resistance (3.5kΩ).

Voltage Loop Compensation

Maximum transient response of the PFC section, without instability, is obtained when the open-loop crossover frequency is one-half the line frequency. For this application, the compensation components (pole/zero pair) are chosen so that the closed loop response decreases at 20dB/decade, crossing unity gain at 30Hz, then immediately decreasing at 40dB/decade. The error amplifier pole is placed at 30Hz and an effective zero at one-tenth this frequency, or 3Hz. Find the crossover frequency (G_{PS} = 1) of the power stage. For reference, Equation 20 finds the power stage pole and Equation 21 finds the power stage DC gain.

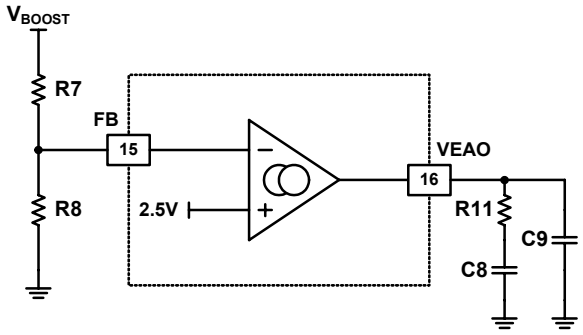

Figure 2. Voltage Amp Compensation

$$f_C = \frac{P_{in(max)}}{2\pi V_O\left(V_{EAO(max)} - 0.625\right)C_5} = \frac{P_{O(max)}}{2\pi\eta V_O\left(V_{EAO(max)} - 0.625\right)C_5} \quad (19)$$
$$= \frac{100}{(2)\cdot(3.1416)\cdot(0.95)\cdot(380)\cdot(6-0.625)\cdot\left(100\times10^{-6}\right)}$$
$$= 82.02Hz$$

$$f_P = \frac{1}{\pi R_L C_5} \quad (20)$$
$$= \frac{1}{(3.1416)\cdot(1444)\cdot\left(100\times10^{-6}\right)}$$
$$= 2.20Hz$$

where:

$$R_L = \frac{V_O{}^2}{P_{O(max)}}$$

$$G_{PS(DC)} = \frac{\sqrt{2}f_C}{f_P} = \frac{(1.414)\cdot(82.02)}{2.20} = 52.72 \quad (34.44dB) \quad (21)$$

The gain of the power stage at 30Hz is calculated by:

$$G_{PS(30Hz)} = \frac{f_C}{30} = \frac{82.02}{30} = 2.734 \quad (8.736dB) \quad (22)$$

The power stage gain is attenuated by the resistive divider $(R_{7A}+R_{7B})/R_8$ according to Equation 23:

$$G_{RDIV} = \frac{R_8}{R_{7A}+R_{7B}+R_8} = \frac{2.37}{178+178+2.37} = 6.613\times10^{-3} \quad (-43.59dB) \quad (23)$$

The amount of error amplifier gain required to bring the open-loop gain to unity at 30Hz is the negative of the sum of the power stage, plus divider stage gain (attenuation):

$$G_{EA} = -\left(G_{PS(30Hz)} + G_{RDIV}\right) = -\left(8.736 + (-43.59)\right) = 34.854dB \quad (55.29V/V) \quad (24)$$

The value of R_{11}, which sets the high-frequency gain of the error amplifier, can be determined by:

$$R_{11} = \frac{G_{EA}}{g_M} = \frac{55.29}{70\times10^{-6}} = 789.8k\Omega \qquad use\ 845k\Omega \quad (25)$$

Calculate C_8; which, together with R_{11}, sets the zero frequency at 3Hz.

$$C_8 = \frac{1}{2\pi R_{11} f_Z} = \frac{1}{(2)\cdot(3.1416)\cdot\left(845\times10^3\right)\cdot(3)} = 62.8nF \qquad use\ 68nF \quad (26)$$

Since the pole frequency is ten times the zero frequency, the pole capacitor C_9 is one-tenth the value of C_8.

$$C_9 = \frac{C_8}{10} = \frac{68\times10^{-9}}{10} = 6.8nF \qquad use\ 10nF \quad (27)$$

Current Loop Compensation

The current loop is compensated like the voltage loop, except the choice of the open-loop crossover frequency. To prevent interaction with the voltage loop, the current loop bandwidth should be greater than ten times the voltage loop crossover frequency, but no more than one sixth the switching frequency, or 16.7kHz. The power stage crossover frequency is calculated by Equation 28, the pole frequency by Equation 29, and the power stage DC gain by Equation 30.

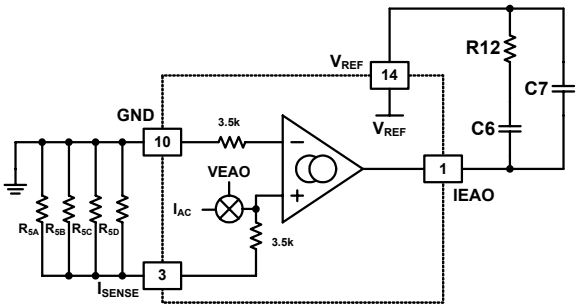

Figure 3. Current Amp Compensation

$$f_C = \frac{(R_{5A} \,||\, R_{5B} \,||\, R_{5C} \,||\, R_{5D})V_O}{2\pi L_1 V_{RAMP_{(P-P)}}} \quad (28)$$
$$= \frac{(0.3)(380)}{(2)\cdot(3.1416)\cdot(3\times10^{-3})\cdot(2.75)}$$
$$= 2.2kHz$$

$$f_P = \frac{1}{\pi R_L C_5} \quad (29)$$
$$= \frac{1}{(3.1416)\cdot(1444)\cdot(100\times10^{-6})}$$
$$= 2.20Hz \qquad same\ as\ (20)$$

$$G_{PS(DC)} = \frac{\sqrt{2}f_C}{f_P} \quad (30)$$
$$= \frac{(1.414)\cdot(2.20\times10^{3})}{2.20}$$
$$= 1414 \quad (63.0dB)$$

Find the gain of the power stage at 16.7kHz.

$$G_{PS(16.7kHz)} = \frac{f_C}{16.7\times10^{3}} \quad (31)$$
$$= \frac{2.20\times10^{3}}{16.7\times10^{3}}$$
$$= 1.32\times10^{-1} \quad (-17.60dB)$$

The current loop contains no attenuating resistors, so find the error amplifier gain with:

$$G_{EA} = -(-G_{PS(16.7kHz)}) \quad (32)$$
$$= -(-17.60)$$
$$= 17.60dB \quad (7.58V/V)$$

Determine the value of the current error amplifier setting resistor R_{12}.

$$R_{12} = \frac{G_{EA}}{g_{M(CE)}} \quad (33)$$
$$= \frac{7.58}{85\times10^{-6}}$$
$$= 89.2k\Omega \qquad use\ 71.5k\Omega$$

Calculate the value of C_6 to form the zero at 1.67kHz.

$$C_6 = \frac{1}{2\pi R_{12} f_Z} \quad (34)$$
$$= \frac{1}{(2)\cdot(3.1416)\cdot(71.5\times10^{3})\cdot(1.67\times10^{3})}$$
$$= 1.33nF \qquad use\ 1.5nF$$

The pole capacitor C_7 is one-tenth the value of C_6.

$$C_7 = \frac{C_6}{10} \quad (35)$$
$$= \frac{1.5\times10^{-9}}{10}$$
$$= 150pF$$

The PWM Stage

Soft-Starting the PWM Stage

The FAN4800 features a dedicated soft-start pin for controlling the rate of rise of the output voltage and preventing overshoot during power on. The controller does not initiate soft-start action until the PFC voltage reaches its nominal value, thereby preventing stalling of the output voltage due to excessive PFC currents. PWM action is terminated in the event the FAN4800 loses power or if the PFC boost voltage falls below $228V_{DC}$. The soft-start capacitor value (C_{19}) for 50ms of delay is found by Equation 36.

$$C_{19} = (t_{SS})\cdot\left(\frac{20\times10^{-6}}{0.95}\right) \quad (36)$$
$$= (0.05)\cdot\left(\frac{20\times10^{-6}}{0.95}\right)$$
$$= 1\mu F$$

Setting the Oscillator Frequency

There is one version of the FAN4800. The FAN4800IN is where the PFC and PWM run at the same frequency.

FAN4800IN

In general, it is best to choose a small-valued capacitor C_{18} to maximize the oscillator duty cycle (minimize the C_{18} discharge time). Too small a value capacitor can increase the oscillator's sensitivity to phase modulation caused by stray field voltage induction into this node. For the practical

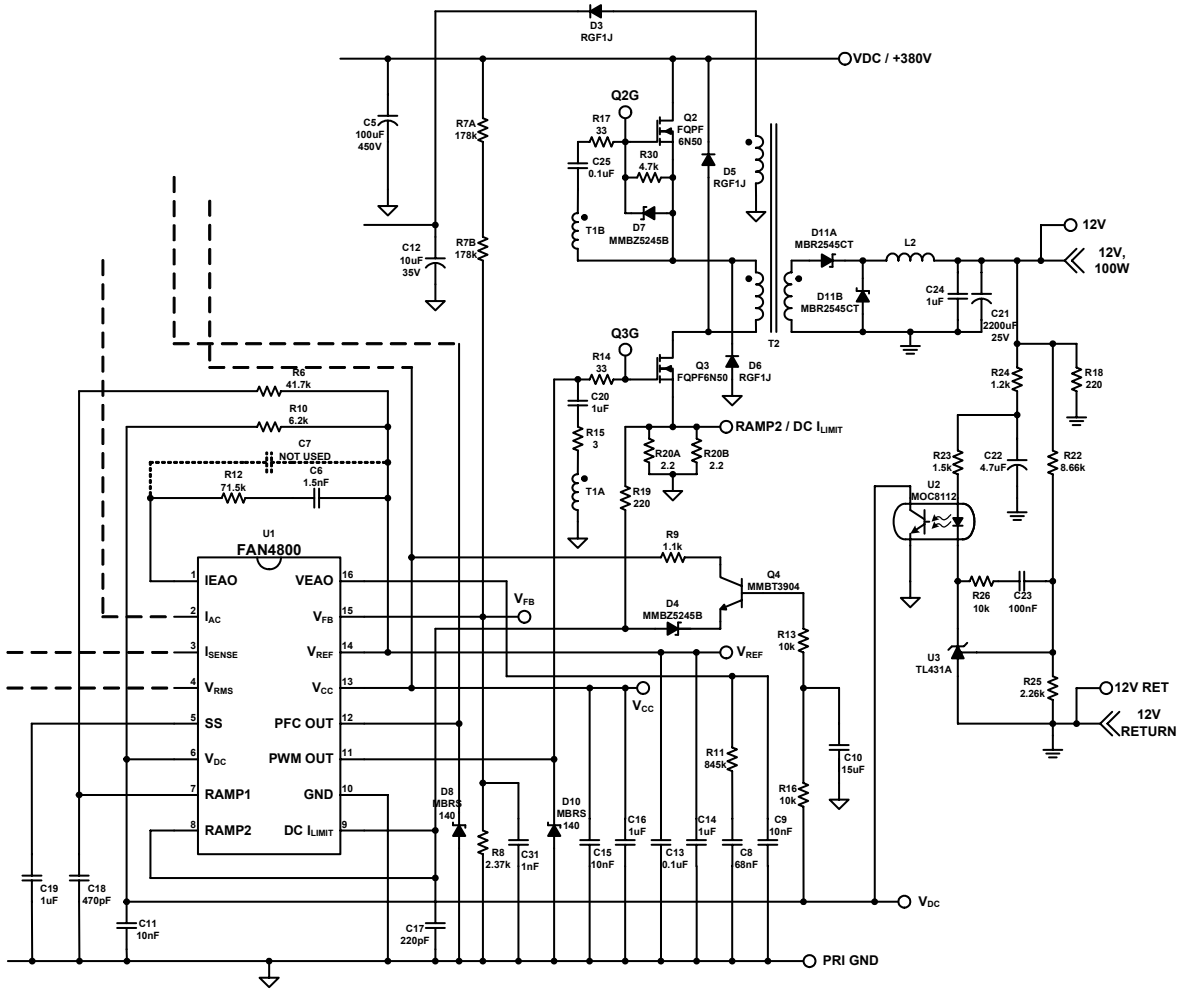

Figure 4. The PWM Stage

example, a 470pF capacitor is chosen for C_{18}. Equation 37 is accurate with values of R_6 greater than 10k.

$$R_6 \cong \frac{1}{0.51 \cdot f_{SW} C_{18}} \quad (37)$$
$$\cong \frac{1}{(0.51) \cdot (1 \times 10^5) \cdot (470 \times 10^{-12})}$$
$$\cong 41.7k\Omega$$

Current Limit

The PWM power stage operates in current mode using R_{20A} and R_{20B} to generate the voltage ramp for duty cycle control. The FAN4800 limits the maximum primary current via an internal 1V comparator; which, when exceeded, terminates the drive to the external power MOSFETs. Maximum primary current is:

$$I_{PRI(MAX)} = \frac{1}{R_{20A} \,||\, R_{20B}} \quad (38)$$
$$= \frac{2.2 + 2.2}{2.2 \times 2.2}$$
$$= 0.91Amps$$

Voltage Mode (Feedforward)

Should voltage mode control be used, it is necessary to know C_5's peak voltage to choose the correct ramp generating components. Equation 39 finds the worst-case peak-to-peak ripple voltage across C_5. To find the peak voltage, divide the ripple voltage by two and add it to the regulated boost voltage. Remember that since the FAN4800 employs leading/trailing modulation, the actual peak-to-peak ripple voltage is generally much less than the calculated value.

$$V_{R(C5)} = I_{OUT(C5)} \sqrt{\left(\frac{1}{4\pi f_L C_5}\right)^2 + ESR(C_5)^2} \quad (39)$$

where:

f_L = line frequency.

Solve Equation 40 for the ramp resistor value. The ramp capacitor value should be in the range of 470pF ~ 10nF. Choose a resistor with an adequate voltage rating to withstand the boost voltage.

$$R_{RAMP} = \frac{\sigma_{(MAX)}}{C_{RAMP} f_{SW} \ln\left(1 - \frac{V_{REF}}{V_O + 0.5V_R}\right)} \quad (40)$$

where:

$\sigma_{(MAX)}$ = maximum PWM duty cycle (0.45 for the FAN4800)

V_R = peak-to-peak boost capacitor ripple voltage for Equation 39.

The Power Transformer Turns Ratio

The minimum output voltage at the secondary of T_2 is found in Equation 41. The secondary voltage is chosen to be 30 volts to increase the output voltage hold-up time.

$$V_{SEC(MIN)} = \frac{V_{OUT}}{\sigma_{(MAX)}} + V_F \quad (41)$$
$$= \frac{12}{0.45} + 1.0$$
$$= 27.7 Volts$$

The transformer turns ratio is derived from Equation 42:

$$\frac{N_{PRI}}{N_{SEC}} = \frac{V_O}{V_{SEC(MIN)}} \quad (42)$$
$$= \frac{380}{30}$$
$$N_{PRI} : N_{SEC} = 38 : 3$$

The maximum secondary current with the output shorted is limited by Equation 43:

$$I_{SEC(MAX)} = \frac{I_{PRI(MAX)} N_{PRI}}{N_{SEC}} \quad (43)$$
$$= \frac{(0.91)\cdot(38)}{3}$$
$$= 11.5 Amps$$

The output inductor and rectifier are chosen with maximum current rating larger than the maximum secondary current.

Output Filter Component Filter Selection

L_2's value is chosen to efficiently minimize output ripple current, thereby easing the ESR requirement of the filter capacitor. C_{21}'s ESR value is the dominant contributor to the output ripple. The maximum ESR value required is found in Equation 44:

$$ESR_{(C21)} \le \frac{V_R L_2 f_{SW}}{V_{SEC} \sigma_{(MAX)}} \quad (44)$$

where:

V_R = peak-to-peak output ripple voltage.

Output Voltage Compensation

A TL431 shunt regulator U_3 and opto-isolator U_2 perform output voltage setting and regulation. The opto crosses the primary-to-secondary safety boundary, varying the voltage on the V_{DC} pin to keep the output voltage constant against line and load changes. Using current-mode control simplifies loop compensation, leaving only a single pole and zero in the output stage. The pole is created from the output capacitor and equivalent load resistance. The zero is formed from the filter capacitor and its ESR. In this example, the action of the zero occurs well after the closed-loop response has crossed unity, so it was not compensated with a pole. The output pole is canceled, increasing the overall bandwidth by the addition of R_{26} and C_{23}, which form a zero with TL431. For more information on using the TL431, including gain/phase versus frequency characteristics, refer to the Fairchild Semiconductor datasheet for the **TL431**.

3.3V Output Design Changes

The latest microprocessors and support circuitry require a 3.3V supply for proper operation. The FAN4800 is ideal for these applications, including the energy-efficient, ecologically friendly "Green" PC. If the total output power required varies greatly from 100 watts, it is necessary to re-select certain components, beginning with the PFC stage. T_2's turn ratio must be adjusted according to Equation 42 and another low-current secondary winding added using the same turns ratio as originally found for the +12 volts. This second winding is necessary to power the TL431/opto circuit because the 3.3V output is not adequate to fully bias the feedback circuitry. C_{21} may be increased to reduce the output ripple voltage. Figure 5 displays a 3.3V output stage capable of supplying 16 amps.

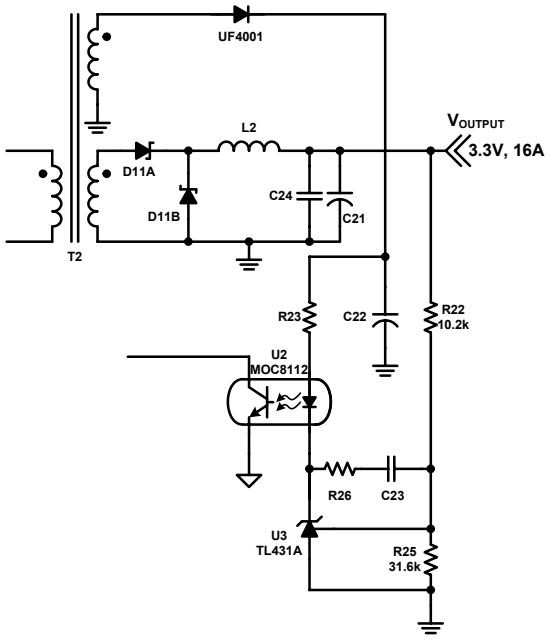

Figure 5. 3.3V Output Stage

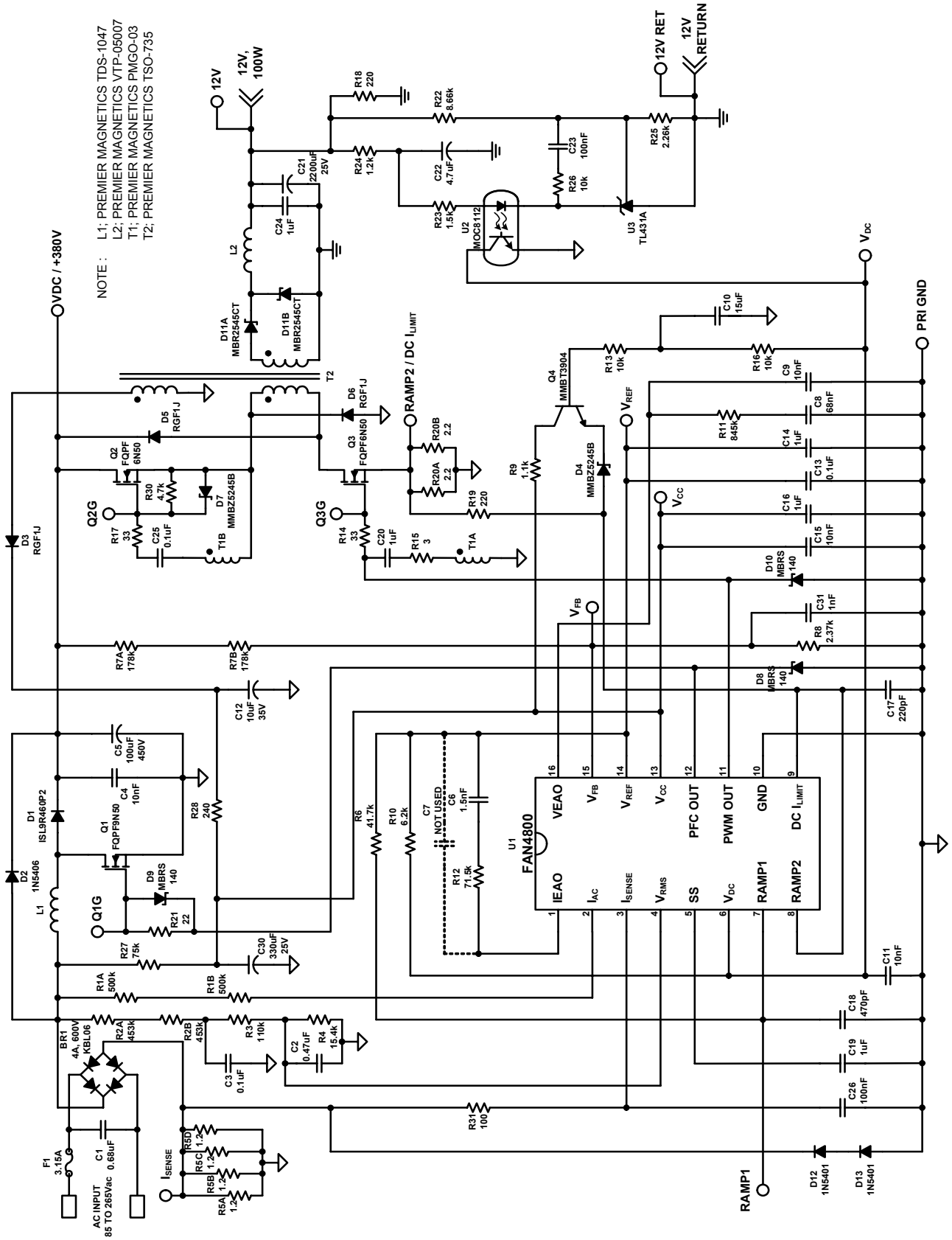

Figure 6. Complete 100W Circuit (Current Mode)

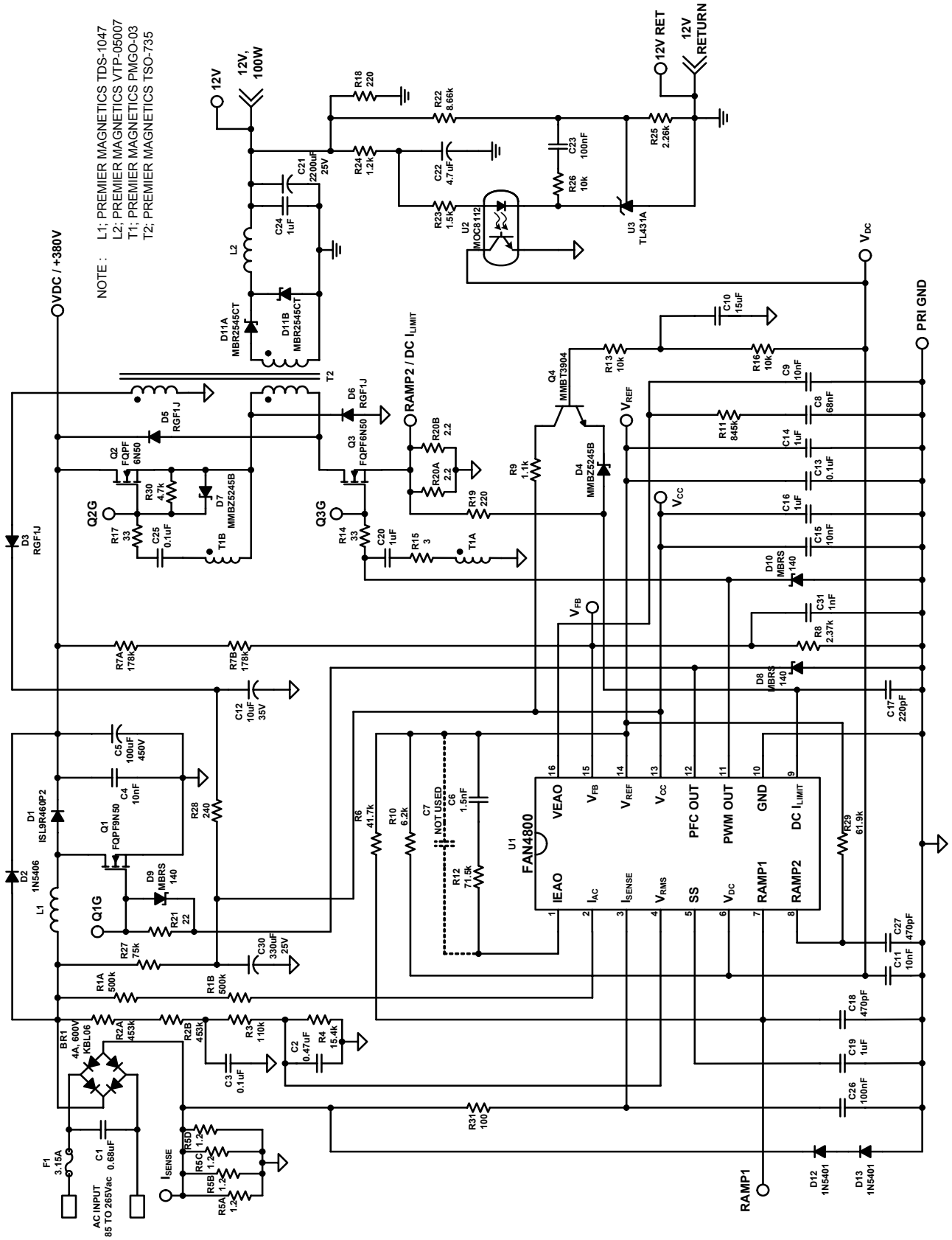

Figure 7. Complete 100W Circuit (Voltage Mode)