AN-9752

Design Guidelines for New-Generation FPS™ FSB-Series

1. Introduction

The FSB-series is a next-generation Green-Mode Fairchild Power Switch (FPS™) incorporating Fairchild's innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling conformance to worldwide standby efficiency guidelines. It integrates advanced current-mode pulse-width modulator (PWM) and an avalanche-rugged 700V SenseFET in a single package; allowing auxiliary power designs with higher standby energy efficiency, reduced size, improved reliability, and lower system cost than previous solutions. The typical application circuit is shown in Figure 1.

This application note focuses on design consideration of two unique functions of FSB-series: AX-CAP™ discharge and adjustable peak current limit. It introduces AX-CAP operation principle and provides the equations of discharge time for worst-case scenarios. Then it shows how to achieve the constant power limit and how to design the IPK pin level for appropriate Over-Power Protection (OPP) level.

The design consideration for applying FSB-series to a standby auxiliary power supply with single output is well described in Fairchild application note AN-8024. It covers designing the transformer, selecting the components, feedback loop design, and design tips to maximize efficiency. For multi-output applications, refer to Fairchild application note AN-4137.

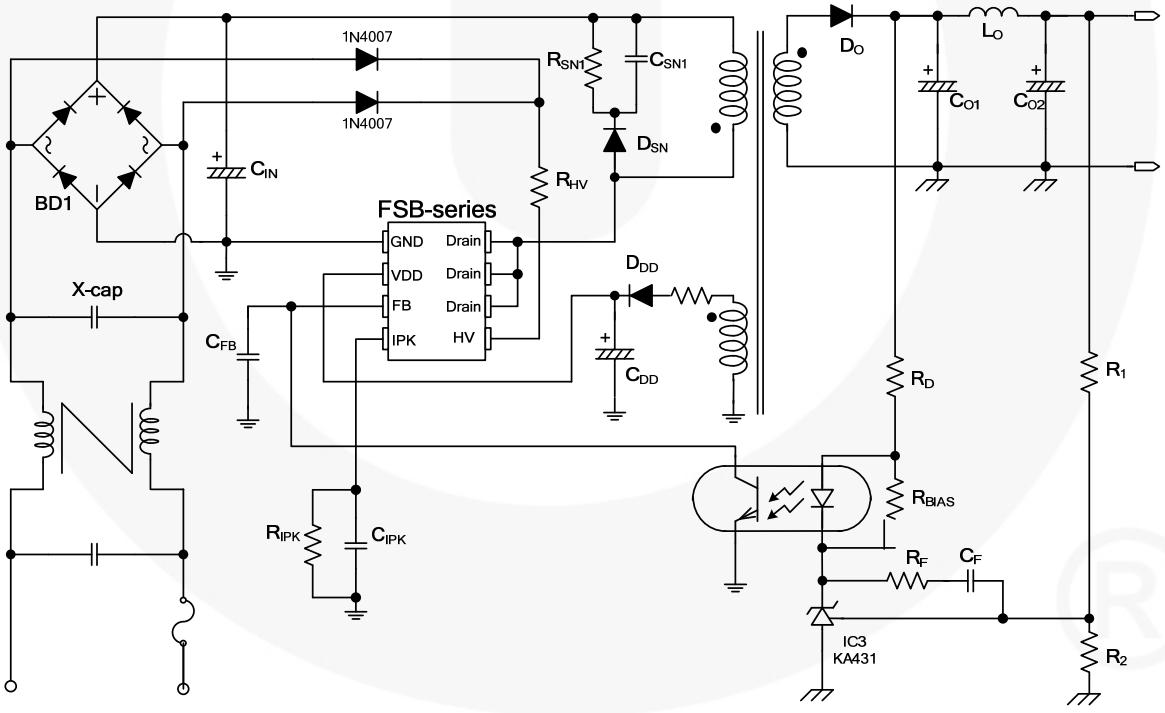

Figure 1. Typical Application Circuit

2. AX-CAP™ Technology

The AX-CAP™ discharge function is one of Fairchild Semiconductor's mWSaver™ technologies offering best-in-class minimum power consumption in no-load and light-load conditions to meet the latest ENERGY STAR specifications and 2013 ErP Standby Power Regulation (less than 0.5W consumption with 0.25W load for ATX power and LCD TV power).

The EMI filter in the front end of the Switched-Mode Power Supply (SMPS) typically includes a capacitor across the AC line connector, as shown in Figure 2. Most of the safety regulations, such as UL 1950 and IEC61010-1, require the capacitor to be discharged to a safe level within a given time after the power supply is unplugged from the power outlet.

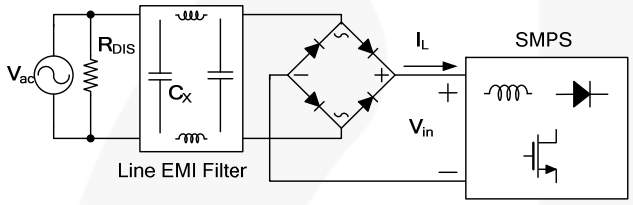

Figure 2. Typical Circuit of Line EMI Filter

- UL1950: voltage across a capacitance greater than 0.1μF must decay to 37% of the AC input peak voltage in one second for type-A equipment and 10 seconds for type-B equipment.
- IEC61010-1: The pins must not be hazardous (live) at five seconds after disconnection from the supply.

The discharge resistor must comply with Equation (1) to meet the discharge time of less than one second. The power loss of discharge resistor paralleled with X-cap is shown in Equation (2):

$$\tau_{DIS} = C_X \times R_{DIS} \le 1s \quad (1)$$

$$P_{Loss} = \frac{V_{AC\,(RMS)}^{2}}{R_{DIS}} \quad (2)$$

Table 1 shows the relationship between rated output power, typical effective X capacitor value, and power dissipation of the discharge resistor. As the power level increases, the EMI filter capacitor tends to increase and, therefore, requires a smaller discharge resistor to maintain the same discharge time. This typically results in more power dissipation in high-power applications. Power dissipation in the discharge resistor is a major cause of standby power consumption in high-power applications.

Table 1. Power Dissipation in Discharge Resistor for Different Rated Power System

Effective X-CAP	Typical Rated Output Power	Discharge Resistor	Power Dissipation in Discharge Resistor at $240V_{AC}$ for t_{DIS}=1s
250nF	20~50W	4MΩ	14.4mW
500nF	50W~100W	2MΩ	28.8mW
1μF	100W~200W	1MΩ	57.6mW
2μF	200W~400W	500kΩ	115.2mW
4μF	400W~800W	250kΩ	230.4mW
8μF	800W~1,600W	125kΩ	460.8mW

The innovative AX-CAP discharge method, a proprietary mWSaver technology of Fairchild Semiconductor, was developed to eliminate X-cap discharge resistors while meeting safety requirements.

2.1 Proposed Solution

Figure 3 shows the typical application circuit and internal blocks for AX-CAP™ technology. It intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the AX-CAP discharge circuit is disabled in normal operation, the power loss in the EMI filter can be virtually removed. In normal operation, the line voltage is detected by sensing X capacitor voltage with a switched voltage divider composed of external high-voltage resistor (R_{HV}) and internal resistor (R_{LS}). The switched voltage divider is driven with a very narrow pulse such that the power consumption of the voltage divider can be minimized.

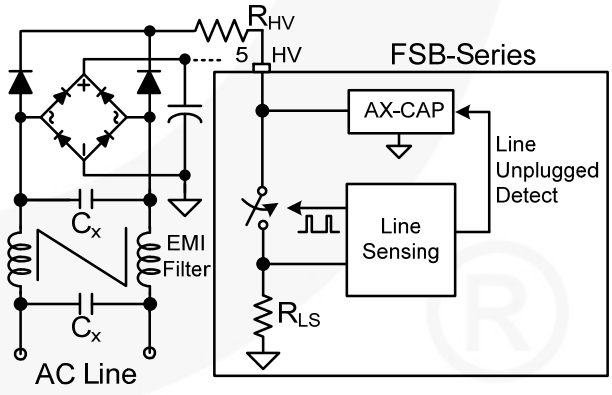

Figure 3. AX-CAP™ Circuit Connection of FSB-Series

AX-CAP™ detects the line disconnection by checking the zero crossing of X capacitor voltage. In normal operation, X capacitor voltage drops down to zero repetitively as long as it is connected to the line. Once the power supply is disconnected from power outlet, the bridge rectifier is reverse biased and the only discharge path for the X capacitor is through the switched voltage divider. Then, the

X capacitor is slowly discharged, as seen in Figure 4. If the X capacitor voltage is higher than half of line peak voltage for longer than debounce time, the FSB-series enters Discharge Mode, where the switched voltage divider is kept on to provide the discharge path.

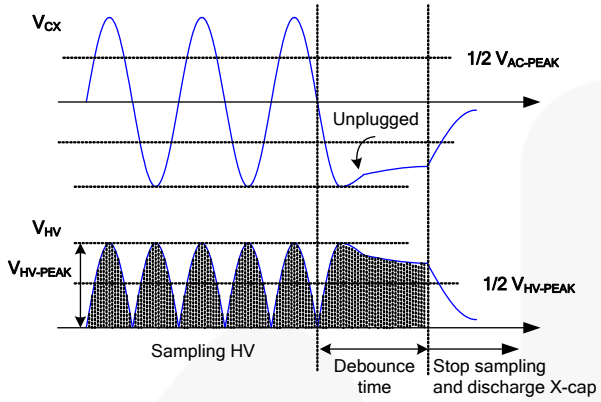

Figure 4. Behavior of HV Pin as Unplugged from the Power Outlet

2.2 Worst-Case Analysis

The discharge time after pulling out the plug can be calculated by Equations (3) and (4):

$$V_{DIS-ST} = V_{CX} \cdot e^{-\frac{t_{AC-OFF}}{R_{HV} \cdot C_X} \cdot \frac{t_{S-TIME}}{t_{S-CYCLE}}} \quad (3)$$

$$t_{DIS} = t_{AC-OFF} + R_{HV} \cdot C_X \cdot \ln \frac{V_{DIS-ST}}{V_{DIS-EN}} \quad (4)$$

where:

V_{DIS-ST} the voltage level of X-cap entering Discharge Mode;

V_{DIS-EN} the voltage level of X-cap meeting safety requirements (37% of AC peak voltage);

t_{AC-OFF} the debounce time of AX-CAP™ detecting line voltage;

t_{S-TIME} HV pin sampling period; and

$t_{S-CYCLE}$ HV pin sampling rate.

The discharge time of FSB-series for worst-case V_{CX}=373V is calculated as shown in Table 2, such that V_{DIS-EN}=138V. Here t_{AC-OFF} is 160ms, t_{S-TIME} is 20µs, and $t_{S-CYCLE}$ is 960µs. R_{HV} is determined by different AC input range; therefore, the worst case can be analyzed as shown in Figure 5.

Table 2. Worst-Case Discharge Times of Different AX-CAP™ in 264V_{AC} Input

X-Cap (µF)	0.10	0.22	0.47	0.68	1.00	2.20	3.30	4.70
Full Range (85V_{AC} ~ 264V_{AC}) – R_{HV}=200kΩ								
t_{DIS} (s)	0.18	0.20	0.25	0.29	0.36	0.59	0.81	1.09
High-Voltage Single Range (170V_{AC} ~ 264V_{AC}) – R_{HV}=400kΩ								
t_{DIS} (s)	0.20	0.24	0.34	0.43	0.55	1.03	1.47	2.03

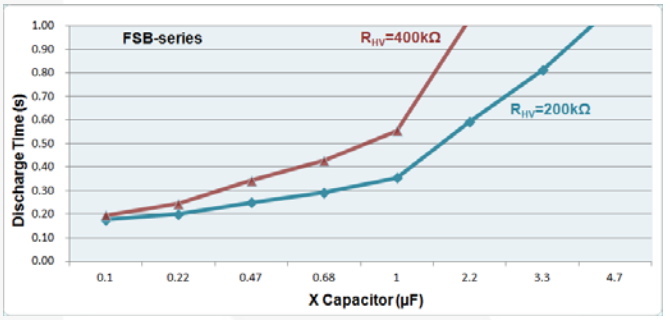

Figure 5. Worst-Case Analysis of Discharge Time for FSB-Series

3. Adjustable Peak Current Limit

3.1 Constant Power Limit

To make the limited output power constant regardless of the line voltage condition, a special current-limit profile with sample and hold is used. The current-limit level is sampled from the current-limit profile and held at the falling edge of the gate drive signal, as shown in Figure 6. Then, the sampled current-limit level is used for the next switching cycle. The sample-and-hold function is used to prevent sub-harmonic oscillation in current-mode control.

The current-limit level increases as the duty cycle increases, which reduces the current-limit level as duty cycle decreases. This allows lower current-limit level for high line voltage condition where the duty cycle is smaller than that of low line. Therefore, the limited maximum output power can remain constant even for a wide input-voltage range.

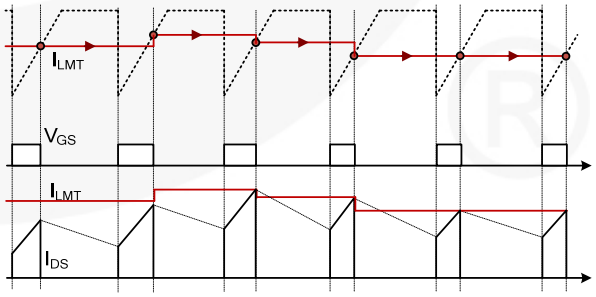

Figure 6. Current Limit Variation with Duty Cycle

3.2 Adjustable Current Limit

The peak current limit is programmable using a resistor on the IPK pin. There is an internal current source of 50μA for the IPK pin, which generates voltage drop across the resistor. The voltage of the IPK pin determines the current limit level. Since the upper and lower clamping voltages of IPK pin are 3V and 1.5V, respectively; the suggested resistor value for the IPK pin is from 30kΩ to 60kΩ.

Figure 7 shows the relationship between the peak current limit I_{LMT} and PWM turn-on time. The peak current threshold level is summarized in Table 3. The current limit plateau, I_{LMT-FL}, and I_{LMT-VA} can be determined by the following equations:

$$I_{LMT-FL} = \frac{1}{1.5}[(V_{IPK} - 1.5) \cdot I_{LMT-FL-H} + (3 - V_{IPK}) \cdot I_{LMT-FL-L}] \quad (5)$$

$$I_{LMT-VA} = \frac{1}{1.5}[(V_{IPK} - 1.5) \cdot I_{LMT-VA-H} + (3 - V_{IPK}) \cdot I_{LMT-VA-L}] \quad (6)$$

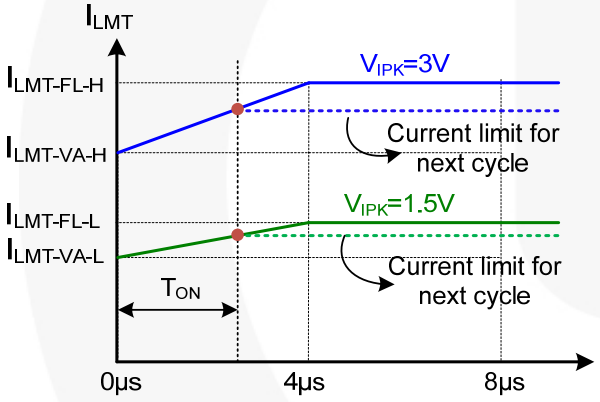

Figure 7. I_{LMT} vs. PWM Turn-On Time

Table 3. I_{LMT} Threshold Level

$I_{LMT-FL-H}$	FSB117H	0.80A
	FSB127H	1.00A
	FSB147H	1.50A
$I_{LMT-VA-H}$	FSB117H	0.60A
	FSB127H	0.75A
	FSB147H	1.13A
$I_{LMT-FL-L}$	FSB117H	0.40A
	FSB127H	0.50A
	FSB147H	0.75A
$I_{LMT-VA-L}$	FSB117H	0.30A
	FSB127H	0.38A
	FSB147H	0.57A

3.3 Over-Power Protection Level

To determine the IPK pin level, the output over-power protection level, P_o, should be given first as:

$$P_o = \left(I_{LMT} \cdot V_{bulk} \cdot t_{on} - \frac{1}{2} \frac{(V_{bulk} \cdot t_{on})^2}{L_m} \right) \cdot f_s \cdot \eta \quad (7)$$

where V_{Bulk} is the input bulk voltage, t_{on} is PWM turn-on time, L_m is the primary-side inductance of the transformer, f_S is the switching frequency, and η is estimated efficiency for OPP level.

Therefore, the peak current limit I_{LMT} can be obtained as:

$$I_{LMT} = \frac{P_o}{V_{Bulk} \cdot t_{on} \cdot F_s \cdot \eta} + \frac{V_{Bulk} \cdot t_{on}}{2L_m} \quad (8)$$

With a given transformer specification, the PWM turn-on time can be determined as (refer to AN-8024):

$$t_{on} = \left(\frac{V_o \cdot N_p}{V_o \cdot N_p + V_{Bulk} \cdot N_s} \right) \cdot \frac{1}{F_s} \quad (9)$$

where N_p and N_s are the number of turns for the primary and secondary side, respectively, and V_o is the output voltage.

Then I_{LMT} can be expressed as:

$$I_{LMT} = \frac{I_{LMT-FL} \cdot t_{on} + I_{LMT-VA} \cdot (4\mu - t_{on})}{4\mu} \quad (10)$$

Notice that t_{on} should be smaller than 4μs to meet Equation 10. V_{IPK} can be obtained as:

$$V_{IPK} = \frac{6\mu \cdot I_{LMT}}{t_{on} \cdot (A - C) + (4\mu - t_{on}) \cdot (B - D)} \quad (11)$$

where A is $I_{LMT-FL-H}$, B is $I_{LMT-VA-H}$, C is $I_{LMT-FL-L}$, and D is $I_{LMT-VA-L}$ that can be found in Table 3.

Therefore, the resistance of the IPK pin is determined as:

$$R_{IPK} = \frac{V_{IPK}}{50\mu} \quad (12)$$

Although the upper and lower clamping voltage of the IPK pin are 3V and 1.5V, respectively; R_{IPK} is recommended from 30kΩ to 60kΩ.

Appendix: Design Example for Peak Current Limit of FSB-Series

Application	Device	Output Power	Input Voltage	Output Voltage	Over-Power Protection (OPP)
ATX Standby	FSB127H	10W	85 ~ 265V_{AC}	5V	15W

1. System Specification

Output Voltage (V_o)	**5**	V
Over Power Protection (OPP)	**15**	W
Switching Frequency (F_s)	**100**	kHz
Estimated Efficiency (η)	**75**	%

2. Transformer Specification

Primary Turns (N_p)	**106**	T
Secondary Turns (N_s)	**8**	T
Primary Side Inductance (L_m)	**1.2**	mH
PWM Turn-on Time as 85V_{AC} (t_{on})	**3.55**	**μs**
Peak Current Limit (I_{LMT})	**0.646**	**A**

3. Threshold Level of Current Limit

Flat Level for V_{IPK}=3V ($I_{LMT-FL-H}$)	**1.00**	A
Valley Level for V_{IPK}=3V ($I_{LMT-VA-H}$)	**0.75**	A
Flat Level for V_{IPK}=1.5V ($I_{LMT-FL-L}$)	**0.50**	A
Valley Level for V_{IPK}=1.5V ($I_{LMT-VA-L}$)	**0.38**	A
IPK Pin Level (V_{IPK})	**1.997**	**V**
Flat Level of Current Limit (I_{LMT-FL})	**0.666**	**A**
Valley Level of Current Limit (I_{LMT-VA})	**0.503**	**A**

4. Over-Power Protection of FSB127H

AC Input (V_{AC})	90	115	132	180	230	264	V
Over Power Protection (P_o)	**15.1**	**15.0**	**14.9**	**14.5**	**14.1**	**13.9**	**W**

References

AN-4137 — Design Guidelines for Offline Flyback Converters Using FPS™

AN-8024 — Applying Fairchild Power Switch (FPS™) FSBH-Series to Standby Auxiliary Power Supply

FSB127H / FSB147H — mWSaver™ Fairchild Power Switch (FPS™) Datasheet, Fairchild Semiconductor