FAIRCHILD SEMICONDUCTOR®

February 1998
Revised April 2003

# Family Characteristics
# TinyLogic® HS/HST and UHS Series

## Characteristics HS/HST Series

- High Speed performance
  HS propagation delays comparable to HC
  HST propagation delays comparable to HCT
- High noise immunity
  HS $V_{NIH} = V_{NIL} = 28\%$ of $V_{CC}$ (CMOS compatible inputs)
  HST $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ (TTL compatible inputs)
- Low noise generation
  Output edge rates comparable to HC/HCT
  One half the output current drive of HC/HCT
  Single output switching
- Balanced output current drive
  $|I_{OH}| = I_{OL} = 2$ mA @ $V_{CC} = 4.5V$
- Low quiescent power consumption
  $I_{CC} < 1$ µA @ 25°C
- Broad $V_{CC}$ operating range
  HS 2V to 6V with 2V, 3V, 4.5V and 6V specs
  HST 4.5V to 5.5V for standard 5V operation
- Dual rail ESD protection for input and output
- Industry standard single-gate functions and pin out
- Space saving SMT packaging in SOT23 and SC70

## DC Comparison Table (NC7S00/ST00 vs. HC00/HCT00)

DC Electrical Characteristics @ $T_A = -40$ to +85°C (unless otherwise noted)

| Parameter | $V_{CC}$ (V) | NC7S00 | HC00 | $V_{CC}$ (V) | NC7ST00 | HCT00 | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ /$I_{OL}$ | 6.0 | –2.6/2.6 | –5.2/5.2 | | | | mA |
| $I_{OH}$ /$I_{OL}$ | 4.5 | –2/2 | –4/4 | 4.5 | –2/2 | –4/4 | mA |
| $I_{OH}$ /$I_{OL}$ | 3.0 | –1.3/1.3 | Not spec'd | | | | mA |
| $V_{OL}$ @ $I_{OL}$ (Max) | 6.0 | 0.33 | 0.33 | | | | V |
| $V_{OL}$ @ $I_{OL}$ (Max) | 4.5 | 0.33 | 0.33 | 4.5 | 0.33 | 0.33 | V |
| $V_{OL}$ @ $I_{OL}$ (Max) | 3.0 | 0.33 | Not spec'd | | | | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 6.0 | 5.63 | 5.34 | | | | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 4.5 | 4.13 | 3.84 | 4.5 | 4.13 | 3.84 | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 3.0 | 2.63 | Not spec'd | | | | V |
| $V_{IH}$ (Min) | 4.5 to 6.0 | 0.7•$V_{CC}$ | 0.7•$V_{CC}$ | 4.5 to 5.5 | 2.0 | 2.0 | V |
| $V_{IL}$ (Max) | 4.5 to 6.0 | 0.3•$V_{CC}$ | 0.3•$V_{CC}$ | 4.5 to 5.5 | 0.8 | 0.8 | V |
| $V_{IH}$ (Min) | 3.0 to 4.5 | 0.7•$V_{CC}$ | Not spec'd | | | | V |
| $V_{IL}$ (Max) | 3.0 to 4.5 | 0.3•$V_{CC}$ | Not spec'd | | | | V |
| $I_{IN}$ (Max) | 6.0 | ±1.0 | ±1.0 | 5.5 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ (Max) | 6.0 | 10.0 | 20.0 | 5.5 | 10.0 | 20.0 | µA |

## DC Performance HS/HST Series

The HS/HST series are designed and fabricated to have performance similar to the standard HC/HCT logic families. The DC Comparison Table compares the DC specifications for HS/HST vs. HC/HCT for the "00" NAND gate function. Noteworthy differences are in the reduced $I_{OL}/I_{OH}$ output drive current specification and the improved $V_{OH}$ and $I_{CC}$ specifications for HS/HST vs. HC/HCT. Also, the HS series is fully specified for 3V $V_{CC}$ operation.

Typical output current drive characteristics for the NC7S00 device are shown in *Figure 1* and *Figure 2* at room temperature and over the recommended $V_{CC}$ operating range. All devices in the HS/HST series use the identical output stage and share these characteristics. The drive current decreases with decreasing $V_{CC}$. The low current drive nature of the HS/HST series is consistent with their low noise generation, low dynamic power consumption, and relatively slow output edge rate characteristics. This low current drive does not permit incident-wave switching of transmission lines.

The typical output current drive characteristics over the recommended operating temperature range and operating at 3V and 4.5V $V_{CC}$ is shown in *Figure 3, Figure 4, Figure 5* and *Figure 6*. An increase in operating temperature will reduce the current drive and increase the on-resistance of CMOS transistors.

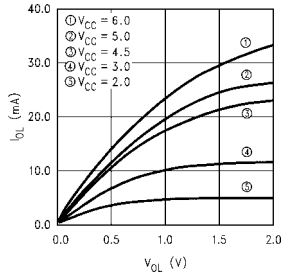


**FIGURE 1. NC7S00 Typical $I_{OL}$ vs. $V_{OL}$ @ $T_A$ = 25°C**

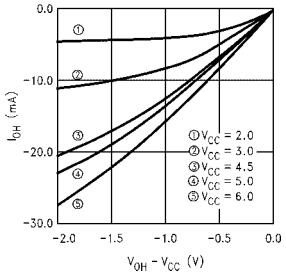


**FIGURE 2. NC7S00 Typical $I_{OH}$ vs. $V_{OH}$ @ $T_A$ = 25°C**

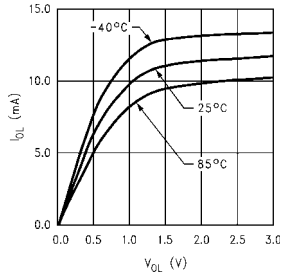


**FIGURE 3. NC7S00 Typical $I_{OL}$ vs. $V_{OL}$ @ $V_{CC}$ = 3V**

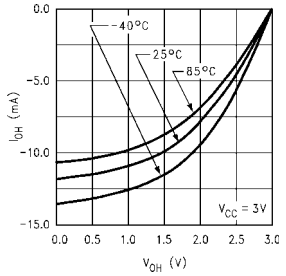


**FIGURE 4. NC7S00 Typical $I_{OH}$ vs. $V_{OH}$ @ $V_{CC}$ = 3V**

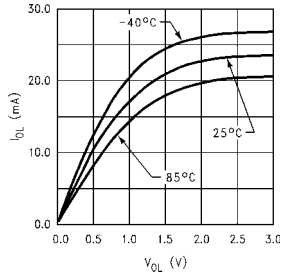


**FIGURE 5. NC7S00 Typical $I_{OL}$ vs. $V_{OL}$ @ $V_{CC}$ = 4.5V**

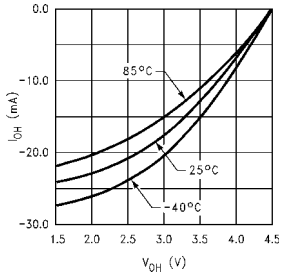


**FIGURE 6. NC7S00 Typical $I_{OH}$ vs. $V_{OH}$ @ $V_{CC}$ = 4.5V**

## Input-Output Voltage Transfer Characteristics HS/HST Series

The Input-Output voltage transfer characteristics are device and circuit design dependent. The HS series is based on designs that utilize a CMOS compatible input structure. The basic CMOS compatible input stage is designed to be in its most active region (switching states) at an input voltage approximately one half of the circuit operating $V_{CC}$. Adding hysteresis circuitry to the basic CMOS compatible input stage will add offset voltage with a directional dependence to increase noise immunity of the stage. Implementation of a standard logic gate contains the input stage, a logic circuitry stage and the output stage.

*Figure 7* shows the typical input-output voltage transfer characteristic for the NC7S04 device. This is representative of inverting logic functions implemented with no hysteresis circuitry. The transfer has sharp corners, high transfer rate, no evidence of hysteresis, and the input transition voltage is centered on a voltage approximately one half of $V_{CC}$ indicating CMOS input compatibility. The sharp corners and high transfer rate results from the cascading of 3 distinct stages of logic circuitry, i.e. 3 stages of gain.

The only device in the HS series implemented with input hysteresis (Schmitt Trigger Input) is the NC7S14. *Figure 8* shows the typical input-output voltage transfer characteristics for the NC7S14 device. Hysteresis is clearly evident as the positive going input transfer voltage is significantly shifted above the $0.5 \bullet V_{CC}$ point while the negative going input transfer voltage has significantly shifted below the $0.5 \bullet V_{CC}$ point.

A special purpose function in the HS series is the NC7SU04 Unbuffered Inverter. This device consists of only one stage of circuitry, the output stage. The NC7SU04 is intended for special use such as in oscillator or AC coupled inverting amplifier analog type applications. *Figure 9* shows the typical input-output voltage transfer characteristic for the NC7SU04 device. The soft corners and gradual transfer rate are indicative of the single stage of circuitry.

The HST series is based on designs that utilize a TTL compatible input structure. The TTL compatible input stage is designed to be in its most active region (switching states) at an input voltage approximately one third of the circuit operating $V_{CC}$. This results in a family of devices which is specified to interface with TTL output swings, operate nominally at standard TTL $V_{CC}$ of 5V ± 10%, and be specified with the TTL compatible input logic levels of $V_{IL}$ = 0.8V maximum and $V_{IH}$ = 2.0V minimum. *Figure 10* shows the typical input-output voltage transfer characteristic for the NC7ST04 device. The input transition voltage is at approximately one third of $V_{CC}$ indicating TTL input compatibility. The transfer has sharp corners, high transfer rate, and no evidence of hysteresis indicating standard logic implementation. No devices in the HST series are implemented as unbuffered or with hysteresis circuitry.

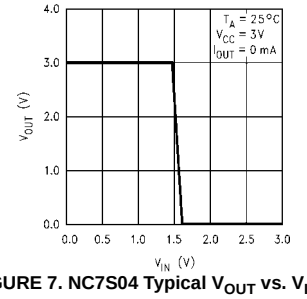


**FIGURE 7. NC7S04 Typical $V_{OUT}$ vs. $V_{IN}$**

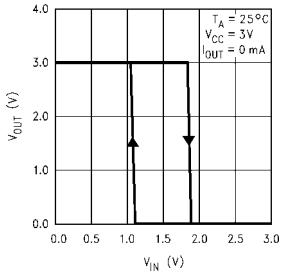


**FIGURE 8. NC7S14 Typical $V_{OUT}$ vs. $V_{IN}$**

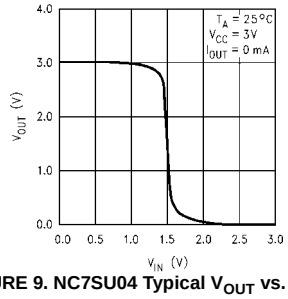


**FIGURE 9. NC7SU04 Typical $V_{OUT}$ vs. $V_{IN}$**

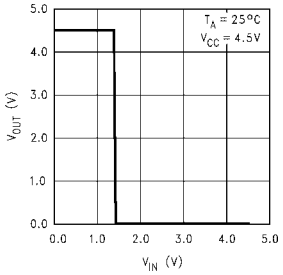


**FIGURE 10. NC7ST04 Typical $V_{OUT}$ vs. $V_{IN}$ @ $I_{OUT}$ = 0mA**

## Input and Output ESD Protection HS/HST Series

All devices in the HS/HST series are implemented with input and output ESD protection diodes with respect to both power rails. Therefore voltages applied to inputs or outputs should not exceed 0.5V above the $V_{CC}$ rail potential or 0.5V below the Ground rail potential unless properly current limited.

## AC Comparison Table (NC7S00/ST00 vs. HC00/HCT00)

AC Electrical Characteristics @ $T_A$= −40 to +85°C; $C_L$ = 50pF; $t_r = t_f$ = 6ns (unless otherwise noted)

| Parameter | $V_{CC}$ (V) | NC7S00 | HC00 | $V_{CC}$ (V) | NC7ST00 | HCT00 | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ (Max) | 6.0 | 21 | 19 | | | | ns |
| $t_{PLH}$ (Max) | 4.5 | 25 | 23 | 4.5 | 20 | 29 | ns |
| $t_{PHL}$ (Max) | 4.5 | 25 | 23 | 4.5 | 31 | 29 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 3.0 | 35 | Not spec'd | | | | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 2.0 | 125 | 113 | | | | ns |
| $t_{TLH}$, $t_{THL}$ (Max) | 6.0 | 26 | 16 | | | | ns |
| $t_{TLH}$, $t_{THL}$ (Max) | 4.5 | 31 | 19 | 4.5 | 31 | 19 | ns |
| $t_{TLH}$, $t_{THL}$ (Max) | 3.0 | 45 | Not spec'd | | | | ns |
| $t_{TLH}$, $t_{THL}$ (Max) | 2.0 | 155 | 95 | | | | ns |
| $C_{PD}$ (Typ @ 25°C) | 5.0 | 6 | | 5.0 | 6 | | pF |
| | 6.0 | | 20 | 5.5 | | 30 | pF |
| $C_{IN}$ (Typ/Max @25°C) | | 2/10 | 5/10 | | 2/10 | 5/10 | pF |

## AC Performance HS/HST Series

The HS/HST series are fabricated on a 2 micron advanced CMOS process which enables AC switching performance comparable to the standard HC/HCT logic families. However, HS/HST series have reduced output drive which yields significantly lower dynamic power consumption than HC/HCT.

The AC Comparison Table compares the AC specifications for HS/HST vs. HC/HCT series for the “00” NAND gate function. Note that HS series is fully specified for 3V $V_{CC}$ operation.

Typical switching performance for the NC7S00 device is shown in *Figure 11, Figure 12*, *Figure 13* and *Figure 14* for the recommended $V_{CC}$ operating range and temperature range. Characteristic of CMOS designs, $t_{PLH}$ vs. $t_{PHL}$ is well balanced as is $t_{TLH}$ vs. $t_{THL}$. Also, slower AC performance at elevated temperature or reduced $V_{CC}$ is characteristic of CMOS designs. The output transition times are relatively slow as compared to other forms of advanced CMOS logic.

Typical switching performance for the NC7ST00 device is shown in *Figure 15* and *Figure 16*. The imbalance seen in $t_{PLH}$ vs. $t_{PHL}$ is induced by imbalance in the measurement specification. For devices with TTL compatible inputs, the specification calls for the propagation delay measurement to be made from the 1.3V point of the input waveform to the 1.3V point on the output waveform. This is in contrast to the 50% on input to the 50% on output points specified for devices with CMOS compatible inputs. While the 1.3V input measure point is very close to the actual dynamic switching voltage of the TTL compatible input, the 1.3V output measure point is not balanced relative to the rail-to-rail swing of the CMOS output stage. The 1.3V output measure point is the primary source of the apparent $t_{TLH}$ and $t_{THL}$ imbalance. The typical $t_{TLH}$ and $t_{THL}$ performance for the HST series is identical to the HS series as the output stage is identical in both HS and HST.

## AC Performance HS/HST Series (Continued)

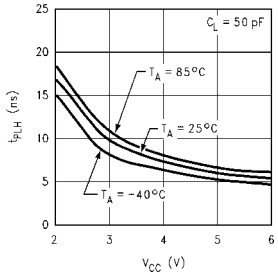


**FIGURE 11. NC7S00 $t_{PLH}$ vs. $V_{CC}$**

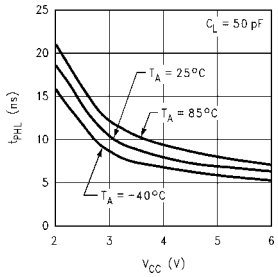


**FIGURE 12. NC7S00 $t_{PHL}$ vs. $V_{CC}$**

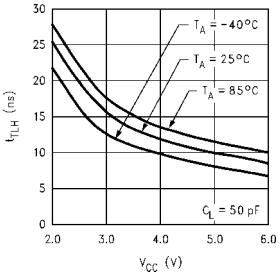


**FIGURE 13. NC7S00 $t_{TLH}$ vs. $V_{CC}$**

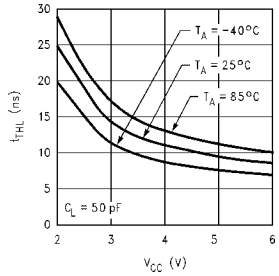


**FIGURE 14. NC7S00 $t_{THL}$ vs. $V_{CC}$**

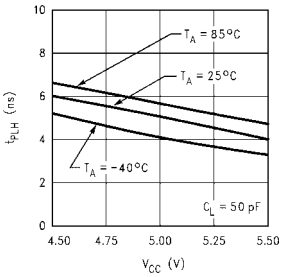


**FIGURE 15. NC7ST00 $t_{PLH}$ vs. $V_{CC}$**

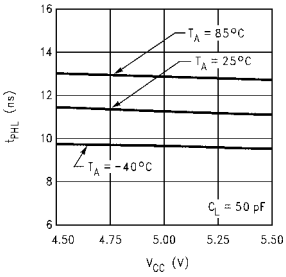


**FIGURE 16. NC7ST00 $t_{PHL}$ vs. $V_{CC}$**

## Characteristics UHS Series

- Ultra High Speed (UHS Series)
  Speeds comparable to LCX when operating at 3V $V_{CC}$
  One half the propagation delay of standard VHC/VHS
- High noise immunity
  $V_{NIH} = V_{NIL}$ = 28% of $V_{CC}$ (CMOS compatible inputs)
- Low noise generation
  Patented noise/EMI reduction circuitry implemented
  Single output switching
- Low quiescent power consumption
  $I_{CC}$ < 2 µa @ 25°C
- High current drive balanced output
  $|I_{OH}| = I_{OL}$ = 32mA @ 4.5V $V_{CC}$
  Four times the current drive of standard VHC/VHS
- Board $V_{CC}$ operating range
  1.8V to 5.5V
- High impedance input and output when powered down
- Over voltage tolerant inputs
- Industry standard Logic functions and pin out
- Space saving SMT SOT23 and SC70 packaging

## DC Comparison Table (NC7SZ00 vs. VHC00)

DC Electrical Characteristics @ $T_A$ = −40 to +85°C (unless otherwise noted)

| Parameter | $V_{CC}$ (V) | NC7SZ00 | LCX00 | $V_{CC}$ (V) | VHC00 | Units |
|---|---|---|---|---|---|---|
| $I_{OH}/I_{OL}$ | 4.5 | −32/32 | NA | 4.5 | −8/8 | mA |
| $I_{OH}/I_{OL}$ | 3.0 | −16/16 | -18/16 | 3.0 | −4/4 | mA |
| $I_{OH}/I_{OL}$ | 2.3 | −8/8 | −8/8 | 2.3 | (not spec'd) | mA |
| $V_{OL}$ @ $I_{OL}$ (Max) | 4.5 | 0.55 | NA | 4.5 | 0.50 | V |
| $V_{OL}$ @ $I_{OL}$ (Max) | 3.0 | 0.40 | 0.4 | 3.0 | 0.44 | V |
| $V_{OL}$ @ $I_{OL}$ (Max) | 2.3 | 0.30 | 0.6 | 2.3 | (not spec'd) | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 4.5 | 3.80 | NA | 4.5 | 3.80 | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 3.0 | 2.40 | 2.4 | 3.0 | 2.48 | V |
| $V_{OH}$ @ $I_{OH}$ (Min) | 2.3 | 1.90 | 1.8 | 2.3 | (not spec'd) | V |
| $V_{IH}$ (Min) (Note 1) | 2.3 to 5.5 | 0.7•$V_{CC}$ | 2.0 | 3.0 to 5.5 | 0.7•$V_{CC}$ | V |
| $V_{IL}$ (Max) (Note 1) | 2.3 to 5.5 | 0.3•$V_{CC}$ | 0.8 | 3.0 to 5.5 | 0.3•$V_{CC}$ | V |
| $I_{IN}$ (Max) | 0 to 5.5 | ±10.0 | 5 | 0 to 5.5 | ±1.0 | µA |
| $I_{OFF}$ (Max) | 0 | ±10.0 | 10 | 0 | (not spec'd) | µA |
| $I_{CC}$ (Max) | 5.5 | 20.0 | 10 | 5.5 | 20.0 | µA |

**Note 1:** $V_{CC}$ is 2.7V to 3.6V for LCX00.

## DC Performance UHS Series

The UHS series is designed and fabricated to have low voltage performance similar to the LCX logic family and is specified to operate over a broad $V_{CC}$ range like the VHC logic family. The DC Comparison Table compares the DC specifications for NC7SZ00 vs. VHC00 and LCX00 NAND gate function. The UHS series is fully specified for operation at the 5V ± 10% $V_{CC}$ range as well as the 3.3V ±0.3V and the 2.5V ± 0.2V low voltage ranges. Except for the NC7SZ384, NC7SZD384, NC7SB3257, NC7WB3125, NC7WBD3125, NC7WB3306, and NC7WBD3306 bus switches, which have TTL compatible control inputs, the UHS series utilize CMOS compatible inputs. The logic input structure of UHS series is designed to be overvoltage tolerant like LCX and VHC families as they can tolerate logic high input voltage levels independent of $V_{CC}$. Thus logic inputs appear as high impedance when $V_{CC}$ is powered down. Like the LCX family, the UHS bi-state and 3-state output stages contain special circuitry to permit them to be high impedance when $V_{CC}$ is powered down. The $I_{OFF}$ specification in the comparison table is indicative of this feature. UHS 3-state output stage, when powered up and in the high impedance state, can remain high impedance independent of $V_{CC}$. For a more detailed discussion, please refer to LCX Family Characteristics in this databook. The NC7SZ66, NC7SB3157 and NC7WB66 switch function I/O ports are tied to the $V_{CC}$ rail by inherent P-N diodes and therefore are not overvoltage tolerant relative to $V_{CC}$.

Typical output current drive characteristics for the NC7SZ00 device are shown in *Figure 17* and *Figure 18* at room temperature and over the recommended $V_{CC}$ operating range. All UHS logic devices with bi-state or 3-state outputs share these high current drive characteristics. The current drive of the NC7SZU04's output is reduced by one half in consideration of it's typical analog application. The drive current naturally decreases with decreasing $V_{CC}$. The high drive nature of UHS permits the driving of transmission lines with incident wave switching.

The typical output current drive characteristics over the recommended operating temperature range and operating at 3V and 4.5V $V_{CC}$ is shown in *Figure 19, Figure 20, Figure 21* and *Figure 22*. Increasing operating temperature will reduce the current drive and increase the on-resistance of CMOS transistors.

## DC Performance UHS Series (Continued)

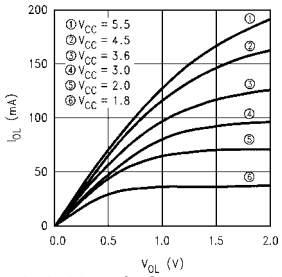


**FIGURE 17. NC7SZ00 Typical $I_{OL}$ vs. $V_{OL}$ @ $T_A$ = 25°C**

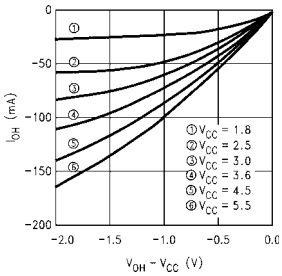


**FIGURE 18. NC7SZ00 Typical $I_{OH}$ vs. $V_{OH}$ @ $T_A$ = 25°C**

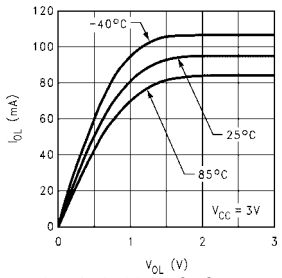


**FIGURE 19. NC7SZ00 Typical $I_{OL}$ vs. $V_{OL}$**

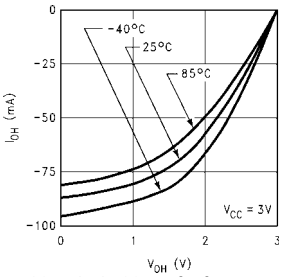


**FIGURE 20. NC7SZ00 Typical $I_{OH}$ vs. $V_{OH}$**

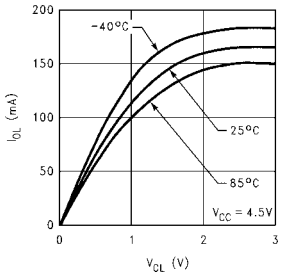


**FIGURE 21. NC7SZ00 Typical $I_{OL}$ vs. $V_{OL}$**

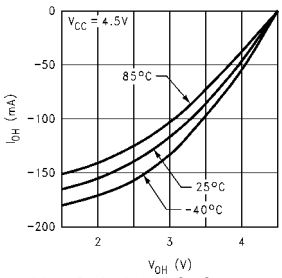


**FIGURE 22. NC7SZ00 Typical $I_{OH}$ vs. $V_{OH}$**

## Input-Output Voltage Transfer Characteristics UHS Series

The Input-Output voltage transfer characteristics are device and circuit design dependent. The UHS series logic devices are based on designs that utilize a CMOS compatible input structure. The basic CMOS compatible input stage is designed to be in its most active region (switching states) at an input voltage approximately one half of the circuit operating $V_{CC}$. Adding hysteresis circuitry to the basic CMOS compatible input stage will add offset voltage with a directional dependence to increase noise immunity of the stage. Implementation of a standard logic device contains the input stage, a logic circuitry stage, and the output stage.

*Figure 23* shows the typical input-output voltage transfer characteristic for the NC7SZ04 device. This is representative of inverting logic functions implemented with no hysteresis circuitry. The transfer has sharp corners, high transfer rate, no evidence of hysteresis, and the input transition voltage is centered on a voltage approximately one half of $V_{CC}$ indicating CMOS input compatibility. The sharp corners and high transfer rate results from the cascading of 3 distinct stages of logic circuitry, i.e. 3 stages of gain.

The only device in the UHS series implemented with input hysteresis (Schmitt Trigger Input) is the NC7SZ14. *Figure 24* shows the typical input-output voltage transfer characteristic for the NC7SZ14 device. Hysteresis is clearly evident as the positive going input transfer voltage is significantly shifted above the $0.5 \bullet V_{CC}$ point while the negative going input transfer voltage has significantly shifted below the $0.5 \bullet V_{CC}$ point.

A special purpose function in the UHS series is the NC7SZU04/NC7WZU04 Unbuffered Inverter. This device consists of only one stage of circuitry, the output stage. The NC7SZU04/NC7WZU04 is intended for special use such as in oscillator or AC coupled inverting amplifier analog type applications. *Figure 25* shows the typical input-output voltage transfer characteristic for the NC7SZU04/NC7WZU04 device. The soft corners and gradual transfer rate are indicative of the single stage of circuitry. The output drive current of the NC7SZU04/NC7WZU04 is half that of the standard UHS logic functions.

The NC7SZ384, NC7SZD384, NC7SB3257, NC7WB3125, NC7WBD3125, NC7WB3306 and NC7WBD3306 Bus Switch devices employ a TTL compatible input structure for the switch control logic. The TTL compatible input stage is designed to be in its most active region (switching states) at an input voltage approximately one third of the circuit operating $V_{CC}$. Thus these TTL compatible inputs are optimized to interface with TTL output swings, operate nominally at standard TTL $V_{CC}$ of 5V ± 10%, and be specified with the standard TTL input logic levels of $V_{IL}$ = 0.8V maximum and $V_{IH}$ = 2.0V minimum.

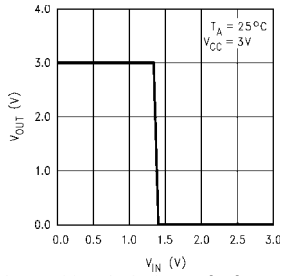


**FIGURE 23. NC7SZ04 Typical $V_{OUT}$ vs. $V_{IN}$ @ $I_{OUT}$ = 0mA**

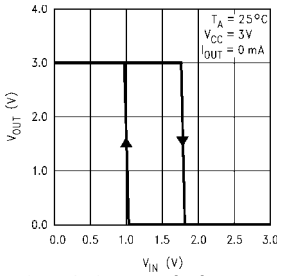


**FIGURE 24. NC7SZ14 Typical $V_{OUT}$ vs. $V_{IN}$**

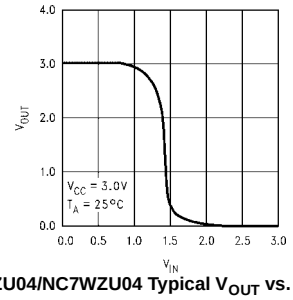


**FIGURE 25. NC7SZU04/NC7WZU04 Typical $V_{OUT}$ vs. $V_{IN}$ @ $I_{OUT}$ = 0mA**

## UHS Switches

The NC7SZ66 Digital Switch device is designed as a non-level shifting pass-switch for digital logic levels. The device employs a P-channel FET in parallel with a N-channel FET to form the pass-switch with very low series on-resistance ($R_{ON}$) over the entire 0V to $V_{CC}$ input voltage range. This allows full swing logic levels to pass through the switch with only the small amount of voltage shifting associated with I•R drop and the switch passes these signals with virtually zero propagation delay. When the switch is turned off, a very high degree of electrical isolation occurs between switch I/O ports. The basic functionality of the Digital Switch is identical to the common Analog/Bilateral Switch. The Digital Switch primarily differs from the Analog Switch in it's on resistance characteristics. The Digital Switch has low $R_{ON}$ but the design does allow for a fairly wide variation in $R_{ON}$ over the switch's operating input voltage range. Analog switches tend to have higher $R_{ON}$ but they strive to limit the variation in $R_{ON}$ over the input voltage operating range to help preserve signal fidelity. The Digital Switch may be used in analog applications if variation in $R_{ON}$ is not critical. The NC7SZ66's switch control input is CMOS compatible and the device is specified to operate over the broad $V_{CC}$ voltage range of 2.3V to 5.5V. The switch control input is overvoltage tolerant relative to the $V_{CC}$ potential but the switch I/O ports are not. Voltages applied to the switch I/O ports should be limited to $V_{CC}$ + 0.5V to avoid unwanted forward biasing of P-N diodes associated with the P-channel FET of the switch. The NC7SB3157 and the NC7WB66 devices also utilize the pass switch circuitry and are intended for analog and digital applications.

The NC7SZ384 Bus Switch employs a single N-channel FET as the pass-switch and as such it inherently limits the logic high voltage passed to $V_{CC}$-$VT_{ON}$ under no load conditions. $VT_{ON}$ is effectively 1V at 25°C and no load current. Therefore, operating at a $V_{CC}$ of 5V, a 5V level on the switch input port will be limited to about 4V at the output port at no load current. Input logic low levels and logic high levels less than $V_{CC}$-$VT_{ON}$ will pass unlimited except for minor I•R drop across the switch due to any load current. Operating specifications for $V_{CC}$ of 4V is provided for those applications where there may be a need to limit the switch output port voltage to 3V. Operating at 4V $V_{CC}$, a 5V input will be limited to typically 3V at 25°C and no load current. The control input and I/O switch ports are overvoltage tolerant relative to the $V_{CC}$ potential. The NC7SB3257, NC7WB3125 and NC7WB3306 are bus switch devices employing circuitry similar to the NC7SZ384.

The NC7SZD384 Bus Switch employs a single N-channel FET as the pass-switch and includes circuitry to effectively increase the inherent logic high level shifting/limiting characteristics of the switch. $VT_{ON}$ is effectively 1.5V at 25°C and no load current and limits the logic high voltage passed to $V_{CC}$-$VT_{ON}$. Therefore, operating at a $V_{CC}$ of 5V, a 5V level on the switch input port will be limited to about 3.5V at the output port at no load current. Input logic low levels and logic high levels less than $V_{CC}$-$VT_{ON}$ will pass unlimited except for minor I•R drop across the switch due to any load current. For those applications where the logic high levels need to be limited, the NC7SZD384 has enhanced level shift capability without having to resort to lowering the $V_{CC}$ to 4V as was suggested for the NC7SZ384 device. The control input and I/O switch ports are overvoltage tolerant relative to the $V_{CC}$ potential. The NC7WBD3125 and NC7WBD3306 are level shifting bus switch devices similar to the NC7SZD384.

## AC Comparison Table (NC7SZ00 vs. VHC00)

AC Electrical Characteristics @ $T_A = -40$ to +85°C; $t_r = t_f = 3$ ns (unless otherwise noted)

| Parameter | $V_{CC}$ (V) | NC7SZ00 | VHC00 | LCX00 | $C_L$ (pF) | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ (Max) | 5 ± 0.5 | 4.5 | 8.5 | NA | 50 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 3.3 ± 0.3 | 5.2 | 13.0 | 5.2 | 50 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 5 ± 0.5 | 4.1 | 6.5 | NA | 15 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 3.3 ± 0.3 | 4.7 | 9.5 | (not spec'd) | 15 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 2.5 ± 0.2 | 7.0 | (not spec'd) | (not spec'd) | 15 | ns |
| $t_{PLH}$, $t_{PHL}$ (Max) | 1.8 | 10 | (not spec'd) | (not spec'd) | 15 | ns |
| $C_{PD}$ (Typ @ 25°C) | 5.0 | 30 | 19 | NA | | pF |
| $C_{IN}$ (Typ/Max @ 25°C) | | 4 | 4/10 | 7 (typ) | | pF |

## AC Performance UHS Switches

The TinyLogic UHS series is fabricated on a 0.8 micron advanced CMOS process which enables ultra high speed AC switching performance. The switching speed and current drive of UHS is comparable to the LCX logic family when operating in the 3.3V $V_{CC}$ range. However the UHS logic devices are specified to operate over a broad $V_{CC}$ range of 1.8V to 5.5V. UHS series has 4 times the current drive and switches typically twice as fast as compared to the standard VHC family. The high current drive enables UHS to drive transmission lines with incident wave switching.

The AC Comparison Table compares the AC specifications for the NC7SZ00 vs. the VHC00 and the LCX00 NAND gate function.

Typical switching performance for the NC7SZ00 device is shown in *Figure 26* and *Figure 27* over the recommended $V_{CC}$ operating range and temperature range. Characteristic of CMOS designs, $t_{PLH}$ vs. $t_{PHL}$ is well balanced. Slower AC performance as temperature is elevated or $V_{CC}$ is reduced is also characteristic of CMOS designs. UHS series switching speeds are the fastest of any single-gate logic devices available. Into a 50 pF load, output rise and fall times are typically <2.2 ns for the 5V $V_{CC}$ range and <2.9 ns for the 3.3V $V_{CC}$ range.

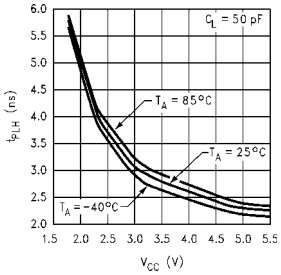


**FIGURE 26. NC7SZ00 Typical $t_{PLH}$ vs. $V_{CC}$**

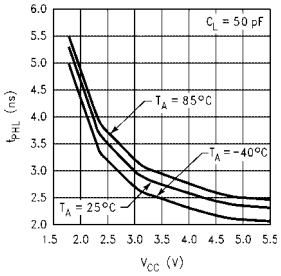


**FIGURE 27. NC7SZ00 Typical $t_{PHL}$ vs. $V_{CC}$**

## Switching Induced Noise

All of the functions in the UHS series, except the NC7SZU04, SZ66, SB3157, WB66, SZ384, SZD384,SB3257, WB3125, WBD3125, WB3306 and WBD3306 employ Graduated Turn-On (GTO™) circuitry to reduce switching induced noise while preserving high performance switching speeds. Please refer to the CROSSVOLT™ Family Characteristics section of this databook for a more detailed discussion of the GTO.