AN-9057

Assembly Guidelines for Asymmetric Dual Power33 Packaging

Introduction

The Fairchild Dual Power33 package is based on Molded Leadless Packaging (MLP) technology. This technology has been increasingly used for power related products due to its low package height and excellent thermal performance, with large thermal pads in the center of the package that solder directly to the printed wiring board (PWB). Modularity in package design, single and multi-die packages, is within the capability of MLP technology.

The Dual Power33 has two large die-attach pads, allowing direct soldering to the PWB for best thermal and electrical performance. These two pads are the co-packaged high- and low-side MOSFETs. The Dual Power33 is designed to be used in high-current synchronous buck DC-DC circuits, saving board space and component count by integrating the high- and low-side MOSFETs into one package.

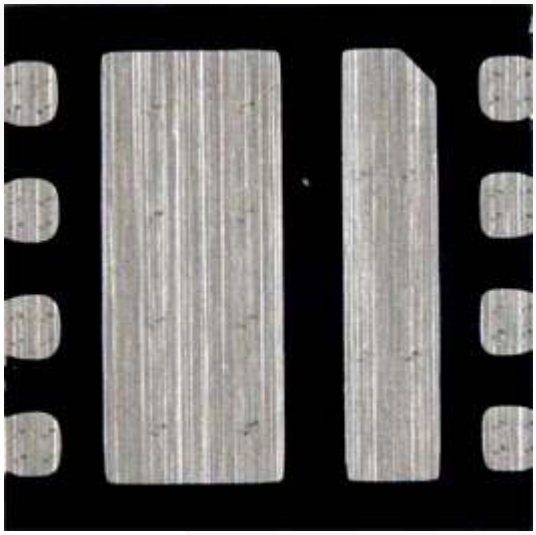

Figure 1. Bottom View Showing Pads for Dual Power33

This application note focuses on the soldering and back-end processing of the Dual Power33.

Board Mounting

The solder joint and pad design are the most important factors in creating a reliable assembly. The pad dimensions must be designed to allow for tolerances in PWB fabrication and pick and place, which are necessary for proper solder fillet formation. MLP packages, when the pre-plated lead-frame is sawn, show bare copper on the end of the exposed edge leads. This is normal and is addressed by IPC JEDEC J-STD-001C “Bottom Only Termination” standard. In practice, it has been found that optimized PWB pad design and a robust solder process often yield solder fillets to the ends of the lead due to the cleaning action of the flux in the solder paste.

Figure 2. Exposed Copper on Package Edge, Solder Wetting after Reflow, Singulation Process

PWB Design Considerations

Any land pad pattern must take into account the various PWB and board assembly tolerances for successful soldering of the MLP to the PWB. These factors have already been considered for the recommended footprint given on the datasheet. This recommended footprint should be followed to assure best assembly yield, thermal performance, and overall system performance.

Pad Finish

The Dual Power33 is sold with a NiPdAu lead-free lead finish. Immersion silver, immersion nickel, gold, and Organic Surface Protectant (OSP) are the pad finishes of choice for lead-free processing. Each finish has useful properties and each has challenges. It is beyond the scope of this paper to debate each solution’s merits. No one finish is right for all applications, but the most common in large-scale consumer electronics, largely due to cost, is OSP. A high-quality OSP, formulated for the rigors of lead-free reflow, like Enthone® Entek® Plus HT, is recommended.

PWB Material

It is recommended that lead free FR-4 is used in PWB construction. Lower quality FR-4 can cause numerous problems with the reflow temperatures seen in lead-free solder. Consult IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" for further information on choosing the correct PWB material for the intended application.

Using VIAs with Dual Power33

Designers often wish to place vias inside the thermal pads. While this is acceptable, realize that vias often create voiding and is advised to carefully characterize the PWB and process designs with x-ray inspection to ensure there is not a voiding problem. Several types of vias can be used in PWB design. Blind vias are not recommended because they often trap gases generated during reflow and yield high percentages of voiding. Solder mask can be placed over the top of the via to prevent solder from wicking down the via. It has been shown that this creates a higher incidence of voiding than an open through-hole or filled via. If through-hole vias are used, a drill size of 0.3mm with one-ounce copper plating yields good performance. With through-hole vias, solder wicking through the hole, or solder protrusion, must be considered. In high-reliability applications, filled vias are preferred due to lower incidences of voiding during reflow. Expect this approach to eliminate the stress riser created by a void at the edges of the via barrel.

Stencil Design

It is estimated that 60% of all assembly errors are due to paste printing. For a controlled, high-yielding manufacturing process, it is the most critical phase of assembly. Due to the importance of the stencil design, many stencil types have been characterized to determine the optimal stencil design for the recommended footprint pad on a typical application board with OSP surface finish, thermal vias, on FR-4. Solder paste coverage for the thermal pads is printed ranging from 50-65% coverage. To allow gases to escape during reflow, it is recommended that the paste be deposited in a grid allowing "channels" for gases to vent. It's been shown that 40-50% solder coverage on the large "S1/D2" pad yielded good void performance, while maintaining good standoff height. For this design, the paste was printed from a 4 mil thick stainless steel stencil. Various different stencil apertures shapes can be used, but were not studied here. The paste was printed on the outer pins with a slightly reduced ratio to the PWB pad. IPC-7525 "Stencil Design Guidelines" gives a formula for calculating the area ratio for paste release prediction:

$$Area\ Ratio = \frac{Area\ of\ Pad}{Area\ of\ Aperture\ Walls} = \frac{L * W}{2 * (L * W) * T}$$

where L is the length, W the width, and T the thickness of the stencil. When using this equation, an Area Ratio >0.66 should yield acceptable paste release. The recommended stencil apertures can be found in the appendix.

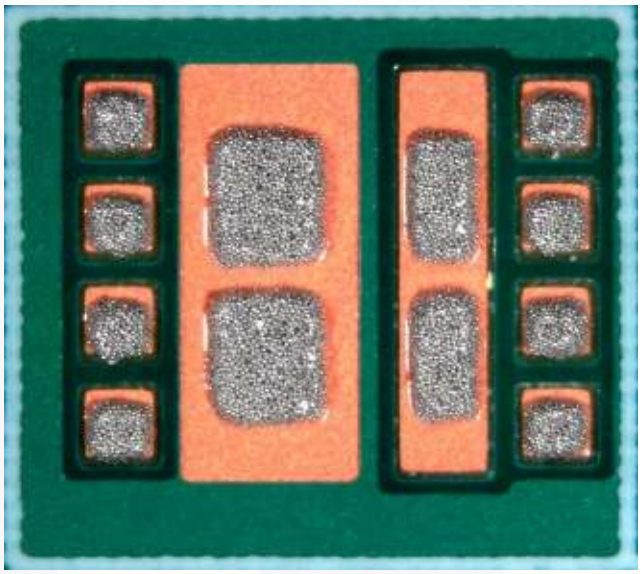

Figure 3. Printed Solder Paste, 40% Coverage

Solder Paste

The Dual Power33 is a RoHS-compliant and lead-free package. The lead finish is NiPdAu. Any standard lead-free no-clean solder paste commonly used in the industry should work with this package. The IPC Solder Products Value Council has stated that the lead-free alloy, 96.5 Sn/3.0Au/0.5Cu, commonly known as SAC 305, is "…the lead-free solder paste alloy of choice for the electronics industry." Type-3 no-clean paste, SAC 305 alloy, was used for the construction of the boards studied to optimize the process for this application note.

Reflow Profile

The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor for their specific products. Obtaining this information from the paste vendor is strongly recommended. If using a KIC® profiler, downloading the latest paste library from KIC yields ramp rate and soak times at temperature for most commonly used solder pastes. Using this data, the software can optimize the zone set-points and speed. The Fairchild Dual Power33 is rated for 260ºC peak temperature reflow. Below is a sample reflow profile used for building demonstration boards. Appendix A is a reflow profile example. This profile is provided for reference only: different PWBs, ovens, and pastes require changes to this profile, perhaps dramatic ones.

Voiding

Voiding is a very controversial topic in the industry. The move to lead-free solders has driven the need for intense study in the area of solders, solder joints, and reliability effects. There are varying viewpoints on the effect of vias and allowable quantity. There are several types of voids; but for simplicity, this applications note classifies them into macro voids and micro voids.

Macro voids can also be called process voids. Macro voids are the large-sized voids commonly seen on x-ray during inspection. These voids are due to process design and process control issues, or PWB design issues. All of the parameters discussed in this application note effect macro voiding. Most standards that currently exist, such as IPC-610D, specifically address void criteria for BGA and limit it to 25%. This standard is for macro voiding.

There is currently no industry standard for macro voiding in MLP solder joints. Fairchild has completed several reliability studies characterizing voiding in various types of components with large thermal pads and the effect on reliability. It's been found that components with ≤25% voiding exhibit acceptable reliability performance in package qualification temperature cycling.

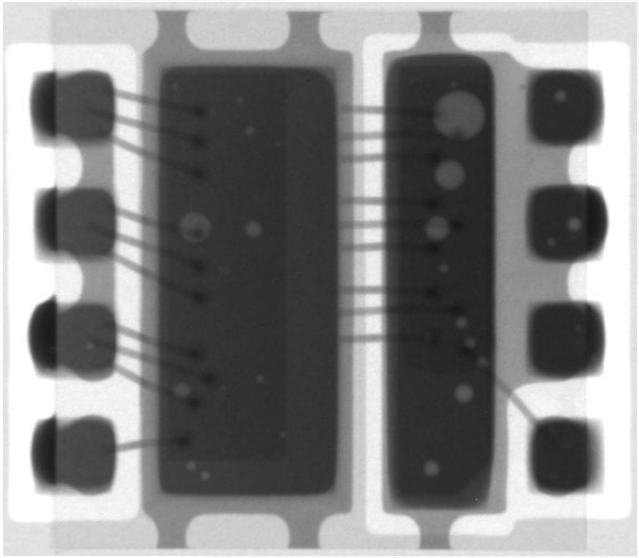

Figure 4. X-Ray Showing Voiding Caused by Normal Process Variation During Reflow

There are several forms of micro voiding, namely planar micro voids and Kirkendall voids. The mechanism of void creation is different, but both are practically undetectable by x-ray inspection. Both types are currently the subject of several in-depth studies; however, none have confirmed theories of creation.

Planar micro voids, or "champagne voids," occur at the PWB land-to-solder-joint interface. There are several theories on the mechanism that creates planar micro voids, but there is no industry consensus on the causal mechanism. Planar micro voids are a risk for reliability failures.

Kirkendall voids are created at the interface of two dissimilar metals at higher temperatures. In the case of solder attachments, at the pad to joint inter-metallic layer. They are not due to the reflow process; Kirkendall voids are created by electro-migration in assemblies that spend large amounts of time above 100ºC. There is conflicting evidence on whether Kirkendall voids are a reliability risk or not.

Rework

Due to the high temperatures associated with lead-free reflow, it is recommended that this component not be reused if rework becomes necessary. The Dual Power33 should be removed from the PWB with hot air. After removal, the Dual Power33 should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick and the pads cleaned and new paste printed with a mini stencil. Localized hot air can then be applied to reflow the solder and make the joint. Due to the thermal performance of this component and the typical high-performance PWB on which it is mounted, quite a bit of heat energy is necessary. Heating of the PWB may be helpful for the rework process.

Board-Level Reliability

Per JDC-STD-001D, a solder fillet is not required on the side of the lead for this package. However, it has been found through modeling and temperature cycling that a solder fillet on the lead end can improve reliability. An improvement of 20% can be expected with this fillet. It has also been found that the 20% reliability enhancement is attained even when the fillet only wets halfway up the side of the lead. The customer can expect to create reliability enhancing solder fillets through proper process design and control.

As part of the standard reliability testing, this package was temperature cycled from -40 to 125°C following IPC-9701 temperature cycle specifications. There were no failures in the sample set after 1000 cycles to pass the test.

APPENDIX

The edge pins and “D1” high-side solder apertures were not varied, only the “S1/D2” pad had solder area coverage varied.

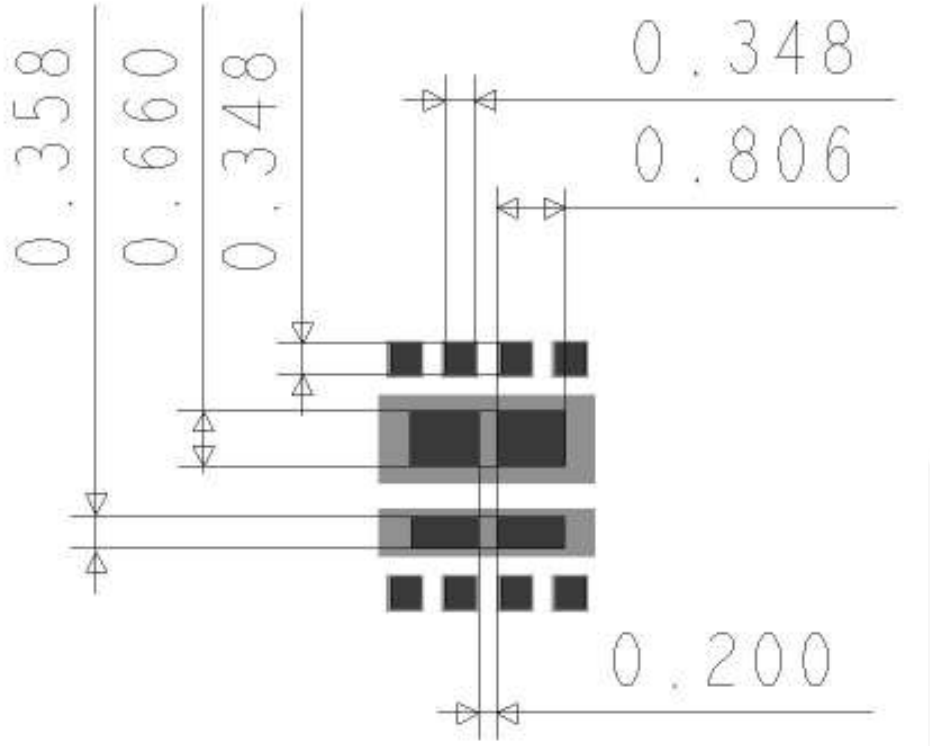

Figure 5. Dimensioned Stencil Apertures, Edge Pins and “D1” Pad Dimensions

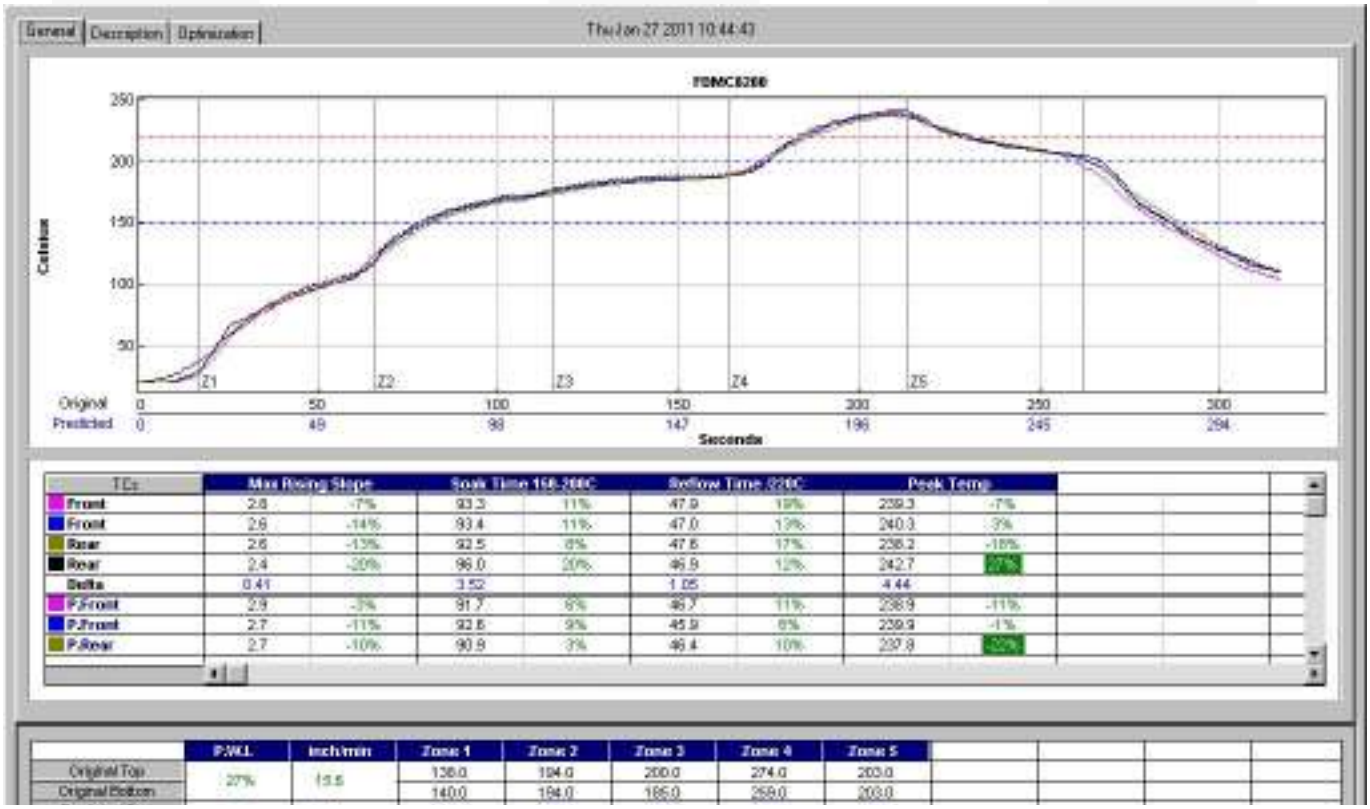

Figure 6. Reflow Profile Used for Demonstration Boards

References

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[3] *Comley, David, et al, "The QFN: Smaller, Faster and Less Expensive," Chip Scale Review.com, August/September 2002.*

[4] *Englemaier, Werner, "Voids in solder joints-reliability," Global SMT & Package, December 2005.*

[5] *IPC Solder Products Value Council, "Round Robin Testing and Analysis of Lead Free Solder Pastes with Alloys of Tin, Silver and Copper," 2005.*

[6] *IPC-A-610-D, "Acceptance of Electronic Assemblies," February 2005.*

[7] *IPC J-STD-001D, "Requirements for Soldered Electrical and Electronic Assemblies."*

[8] *IPC-SM-7525A, "Stencil Design Guidelines," May 2000.*

[9] *JEDEC, JESD22-B102D, "Solderability," VA, Sept. 2004.*

[10] *Syed, Ahmer, et al, "Board Level Assembly and Reliability Considerations for QFN Type Packages," Amkor Technology, Inc., Chandler, AZ.*

Related Datasheets

FDMC8200 — 30V Dual N-Channel PowerTrench® MOSFET

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