Application Note AN6016

LCD Backlight Inverter Drive IC (FAN7311)

1. Description

Design goals for a Cold Cathode Fluorescent Lamp (CCFL) inverter for use in a notebook computer or other portable applications include small size, high efficiency, and low cost. The FAN7311 provides the necessary circuit blocks to implement a highly efficient CCFL backlight power supply in 20-SSOP and 20-SOIC packages. The FAN7311 typically consumes less than 4mA of operating current, improving overall system efficiency. External parts count is minimized and system cost is reduced by the integration of features including; feedback-controlled Pulse Width Modulation (PWM) driver stage, soft start, open lamp regulation, and Under Voltage Lockout protection (UVLO). The FAN7311 includes an internal shunt regulator that allows operation with an input voltage from 5V to 25.5V. It supports analog and burst dimming modes of operation. The FAN7311 provides open lamp regulation and protection. Open lamp regulation protects the transformer from over-voltage during start up or when an open lamp occurs. The transformer voltage is regulated by reducing duty cycle when an over-voltage is detected. Open lamp protection can be used to shut down an IC when an open lamp condition continues longer than a specified time.

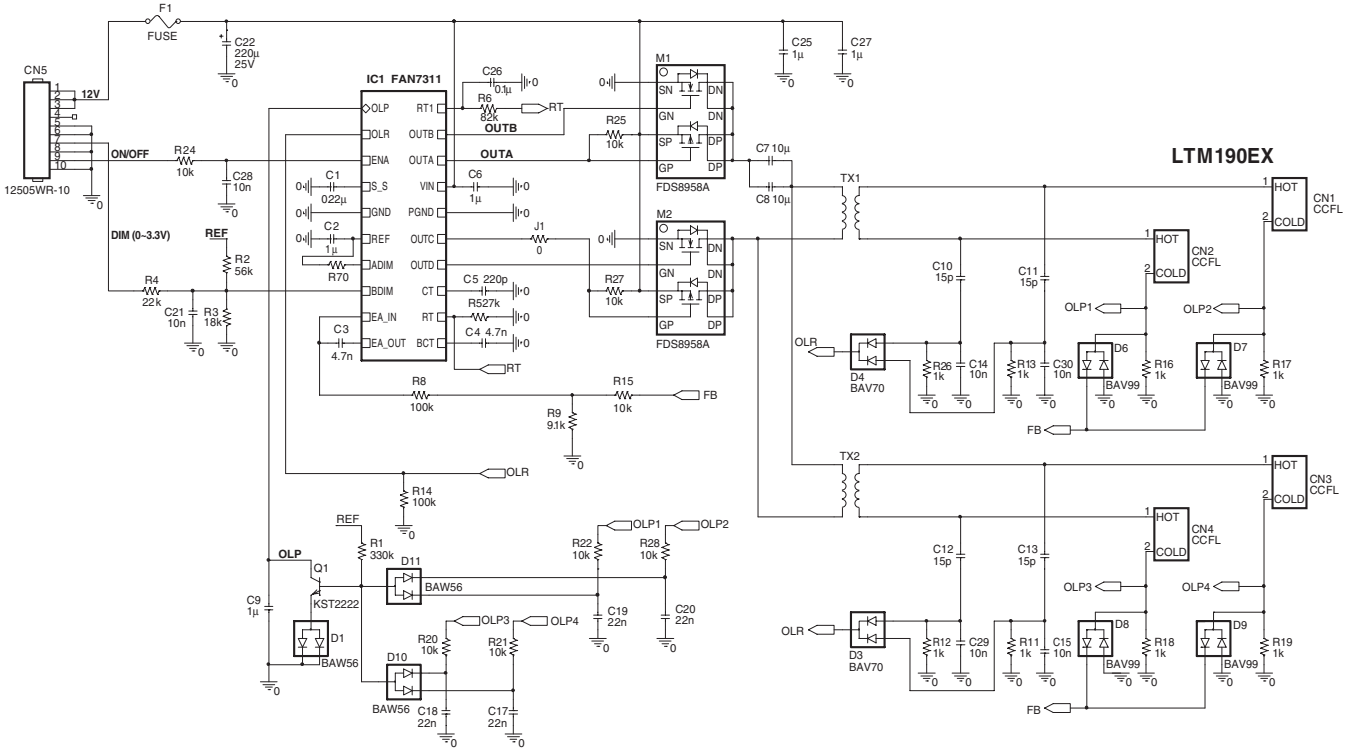


Figure 1. Application Circuit

2. Block Diagram and Basic Operation

2.1 Block Diagram

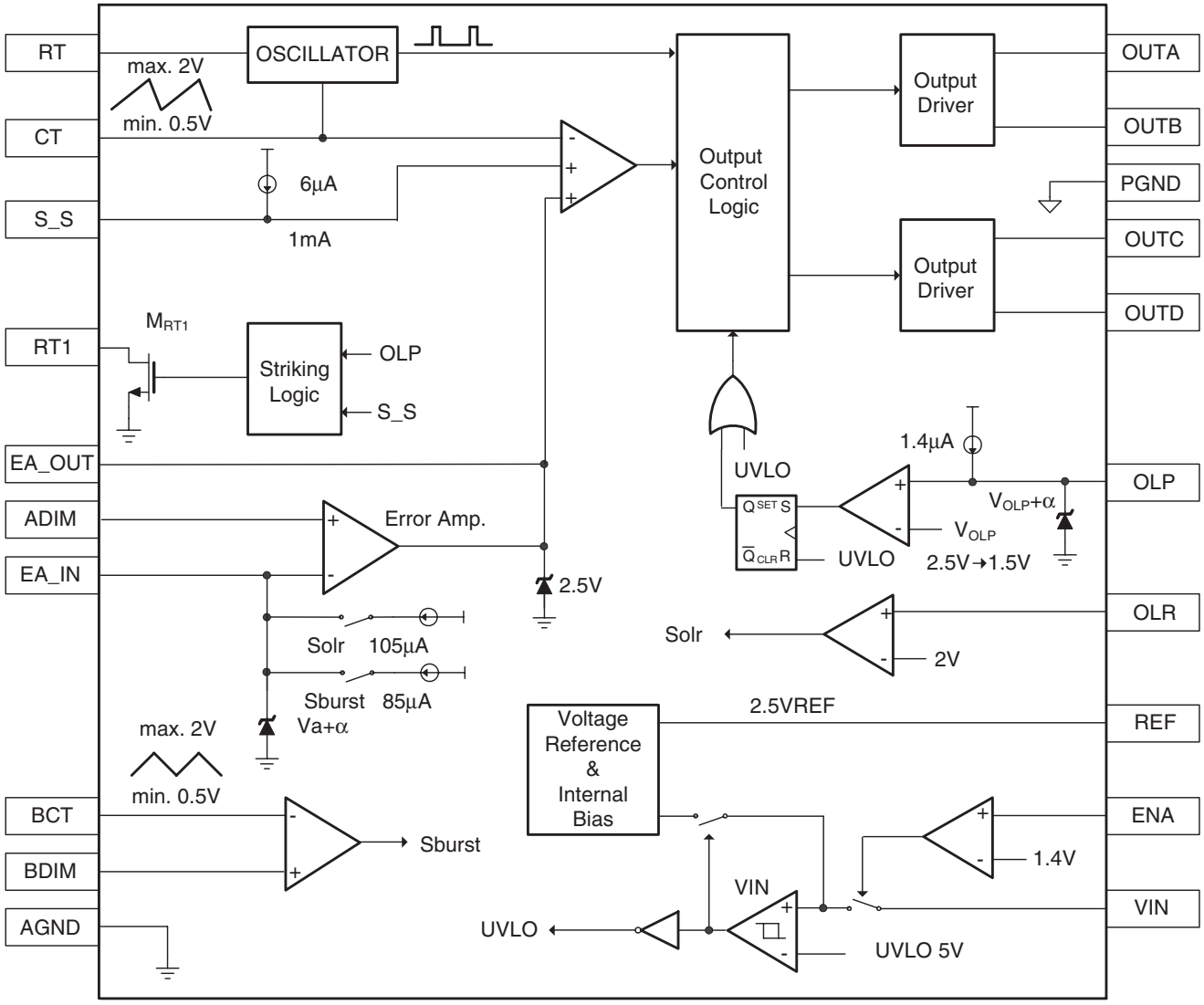


Figure 2. Block Diagram

2.2 Under Voltage Lockout (UVLO)

The UVLO circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the V_{IN} value. The UVLO circuit turns on the control circuit when V_{IN} exceeds 5V. When V_{IN} is lower than 5V, the IC's standby current is less than 200µA.

2.3 ENA

Applying voltage higher than 2V to ENA pin enables the operation of the IC. Applying voltage lower than 0.7V to ENA pin disables the operation of the inverter.

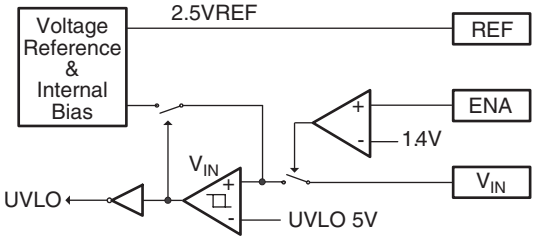


Figure 3. Under Voltage Lockout and ENA Circuits

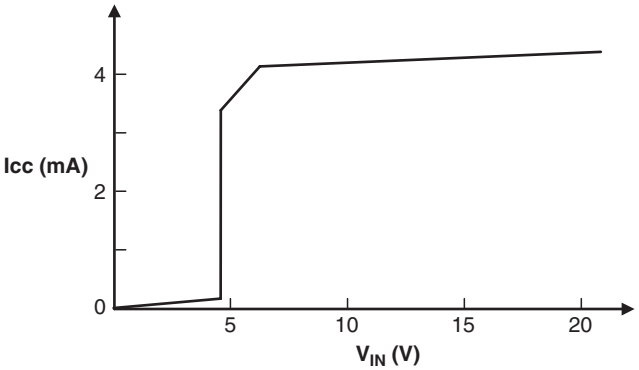


Figure 4. Start Voltage and Operating Current

2.4 Soft Start

The soft-start function is provided by the S_S pin and is connected through a capacitor to GND. A soft-start circuit ensures a gradual increase in the input and output power. The capacitor connected to S_S pin determines the rise rate of the duty ratio. It is charged by a current source of 6µA.

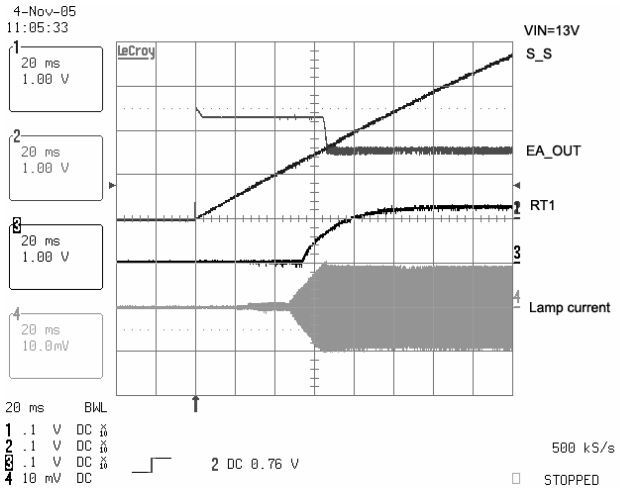


Figure 5. Soft Start During Initial Operation

2.5 Oscillator

2.5.1 Main Oscillator

Timing capacitor C_T is charged by the reference current source. The source is formed by the timing resistor R_T whose voltage is regulated at 1.25V. The sawtooth waveform of the main oscillator circuit charges up to 2V, then the capacitor begins discharging down to 0.5V. The capacitor starts charging again and a new switching cycle begins.

$$I_{charge} = \frac{3}{4}\frac{1.25}{R_T} \quad (2.1)$$

The main frequency can be programmed by adjusting the values of R_T and C_T. The main frequency can be calculated as shown below.

$$f_{op} = \frac{19}{32\,R_T C_T} \quad (2.2)$$

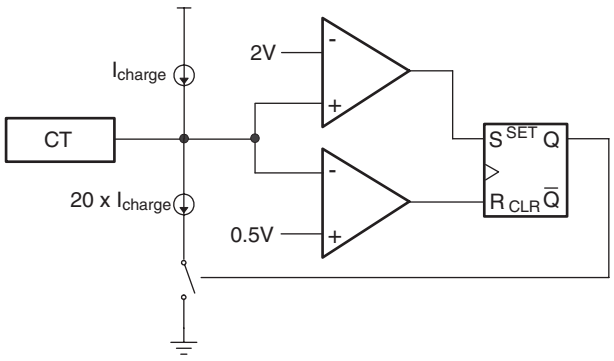


Figure 6a. Main Oscillator Circuit

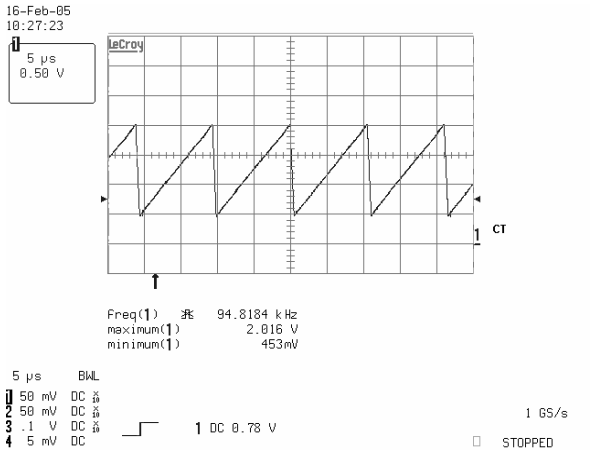


Figure 6b. Main Oscillator Waveform

2.5.2 Burst Dimming Oscillator

Burst dimming timing capacitor BC_T is charged by the reference current source, formed by the timing resistor R_T whose voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once reached, the capacitor begins discharging down to 0.5V, then starts charging again and a new switching cycle begins.

$$I_{charge} = \frac{3}{32}\frac{1.25}{R_T} \quad (2.3)$$

The burst dimming frequency can be programmed by adjusting the values of R_T and BC_T. The burst dimming frequency can be calculated as below.

$$f_{burst} = \frac{3.75}{96\ R_T BC_T} \quad (2.4)$$

The burst dimming frequency should be greater than 120Hz to avoid visible flicker. To compare the input of BDIM pin with the 0.5~2V triangular wave of burst oscillator makes the PWM pulse for burst dimming. The PWM pulse controls EA_OUT voltage by summing 85µA into the EA_IN pin. Figure 7 shows burst dimming oscillator circuit and waveform.

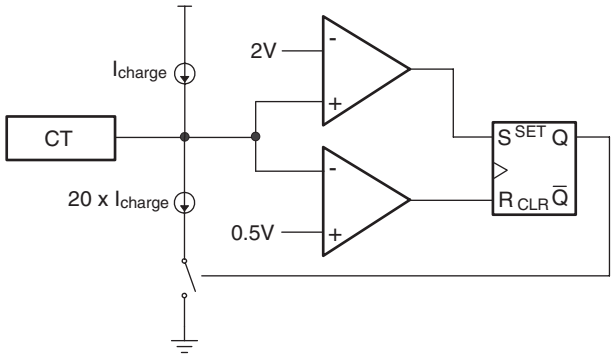


Figure 7a. Burst Oscillator Circuit

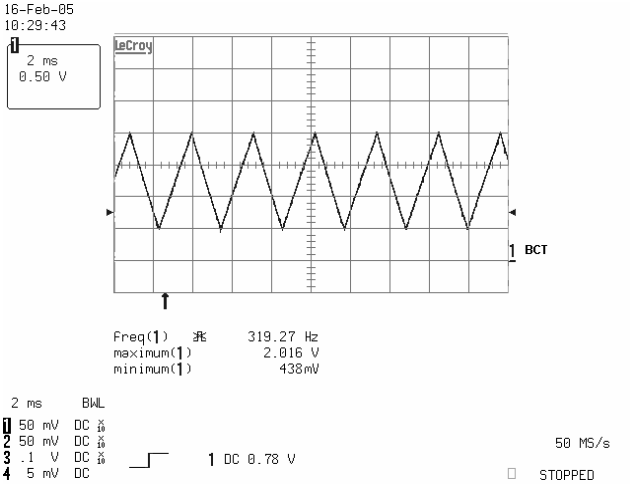


Figure 7b. Burst Oscillator Waveform

2.6 Analog Dimming

For analog dimming, the lamp intensity is controlled with the ADIM signal. A 2.5V on ADIM brings full brightness. Analog dimming waveforms are shown in Figures 8 and 9.

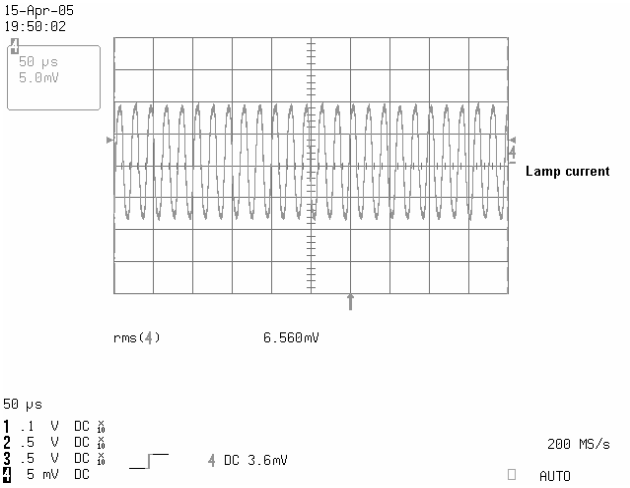


Figure 8. Analog Dimming at Maximum

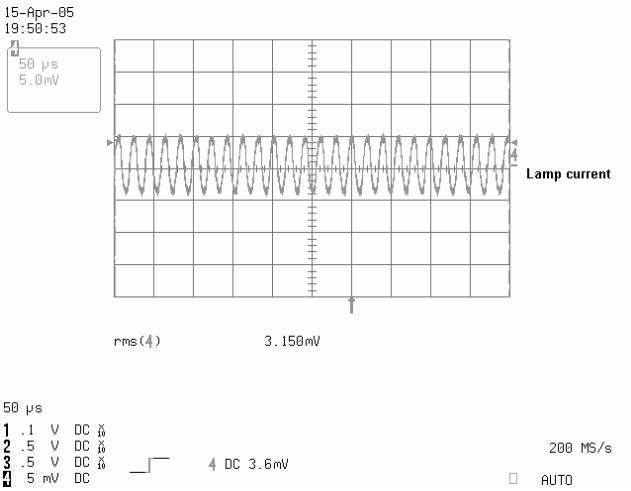


Figure 9. Analog Dimming at Minimum

2.6.1 Setting Lamp Current Sensing Resistors

1) Positive Polarity Analog Dimming

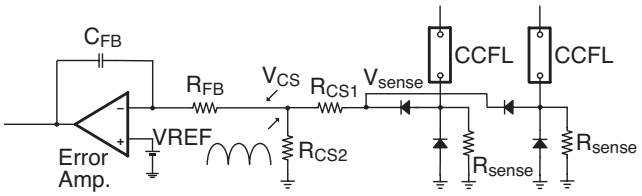


Figure 10. Calculating Value of the Analog Dimming Circuit Parameter

Lamp current is sensed at R_{sense} and the sensed voltage is divided by R_{CS1} and R_{CS2} and is averaged at Error Amp. by R_{FB} and C_{FB}.

$$R_{sense\_eq} = \frac{1 + \frac{V_{DF}}{I_{lamp} \cdot (R_{cs1} + R_{cs2})}}{R} \approx R_{sense} \parallel (R_{cs1} + R_{cs2}),$$

V_{DF} is diode forward voltage

$$V_{sense} = \left(\frac{1}{\pi}\int_0^{\pi} \sqrt{2} \cdot I_{Lamp} \cdot R_{sense\_eq} \cdot \sin\theta \cdot d\theta\right) - V_{DF}$$

$$= \frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense\_eq} - V_{DF} \quad (1)$$

$$V_{CS} = V_{sense} \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} = \left(\frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense} - V_{DF}\right) \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} \quad (2.5)$$

Equation (2.5) assumes that the error amplifier loop is closed. The relationship between V_{CS} and V_{ref} is given in equation (2.6).

$$V_{ref} = V_{CS} = V_{sense} \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}}$$

$$= \left(\frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense} - V_{DF}\right) \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} \quad (2.6)$$

$$\frac{R_{cs1}}{R_{cs2}} = \frac{V_{sense}}{V_{ref}} - 1 \quad (2.7)$$

For example, suppose:

$$V_{ref} = 2.5V,\ I_{Lamp} = 6.5mA,\ R_{sense} = 1k\Omega, R_{cs1} = 10k\Omega$$

From these values, an approximate value of R_{cs2} can be derived. To get a more precise value for R_{CS2}, use an iterative calculation. Use R_{sense} to calculate R_{CS2}, because the R_{sense_eq} value is unknown. After finding the value of R_{sense_eq}, use R_{sense_eq} to calculate R_{CS2}. Calculate iteratively until the previous R_{sense_eq} value is almost equal to the current R_{sense_eq} value.

The data to input

The calculated data

V_{REF}	2.5	
I_{lamp}	6.5	
R_{sense}	1	kΩ
Rsense_eff	0.95	kΩ
Diode drop voltage	0.3	V
Vsense	5.259453252	V
R_{CS1}/R_{CS2}	1.103781301	
R_{CS1}	10	kΩ
R_{CS2}	9.059765727	kΩ

$R_{sense\_effective}$ 0.950148969kΩ = $R_{sense}/(R_{CS1}+R_{CS2})$

2) Negative Polarity Analog Dimming

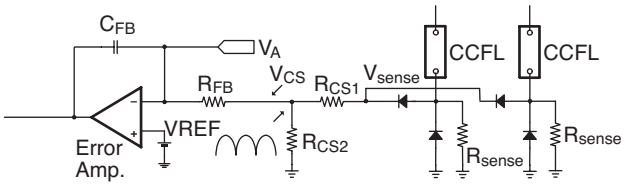


Figure 11. Calculating Value of the Analog Dimming Inverting Circuit Parameter

Lamp current is sensed at R_{sense} and the sensed voltage is divided by R_{cs1} and R_{cs2} and is averaged at Error Amp. by R_{FB} and C_{FB}.

$$R_{sense\_eq} = \frac{1 + \frac{V_{DF}}{I_{lamp} \cdot (R_{cs1} + R_{cs2})}}{R} \approx R_{sense} \parallel (R_{cs1} + R_{cs2}),$$

V_{DF} is diode forward voltage

$$V_{sense} = \left(\frac{1}{\pi}\int_0^{\pi} \sqrt{2} \cdot I_{Lamp} \cdot R_{sense\_eq} \cdot \sin\theta \cdot d\theta\right) - V_{DF}$$

$$= \frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense\_eq} - V_{DF} \quad (1)$$

$$V_{CS} = V_{sense} \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} = \left(\frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense} - V_{DF}\right) \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} \quad (2.8)$$

Equation (2.8) assumes the error amplifier loop is closed. The relationship between V_{CS} and V_A (dimming control voltage) is given in equation (2.9).

$$V_{ref} = \frac{V_A \cdot R_{FB} + V_{CS} \cdot R_A}{R_{FB} + R_A} \quad (2.9)$$

The relationship between dimming control voltage and lamp current can be programmed for the application. For example, suppose:

$$V_{Amin.} = 0,\ I_{Lamp.max} = 7mA \quad (2.10)$$

$$V_{Amax.} = 3.3,\ I_{Lamp.min} = 3mA \quad (2.11)$$

$$I_{Lamp.min} = \alpha \cdot I_{Lamp.max} \quad (2.12)$$

Substituting for V_A and V_{CS} in equation (2.9) from equation (2.10) results in:

$$V_{REF} = \frac{V_{CSmax} \cdot R_A}{R_{FB} + R_A} \quad (2.13)$$

Substituting for V_A and V_{CS} in equation (2.9) from equation (2.11) results in:

$$V_{ref} = \frac{V_{Amax} \cdot R_{FB} + V_{CSmin} \cdot R_A}{R_{FB} + R_A}$$

$$= \frac{V_{Amax} \cdot R_{FB} + \alpha \cdot V_{CSmax} \cdot R_A}{R_{FB} + R_A} \quad (2.14)$$

Multiplying equation (2.13) by $R_{FB} + R_A$ gives:

$$V_{ref} \cdot R_{FB} + V_{ref} \cdot R_A = V_{CSmax} \cdot R_A \quad (2.15)$$

Multiplying equation (2.14) by $R_{FB} + R_A$ gives:

$$V_{ref} \cdot R_{FB} + V_{ref} \cdot R_A = V_{Amax} \cdot R_{FB} + \alpha \cdot V_{CSmax} \cdot R_A \quad (2.16)$$

$$(V_{ref} - V_{Amax}) \cdot R_{FB} + V_{ref} \cdot R_A = \alpha \cdot V_{CSmax} \cdot R_A \quad (2.17)$$

Multiplying equation (2.15) by α gives:

$$\alpha \cdot V_{ref} \cdot R_{FB} + \alpha \cdot V_{ref} \cdot R_A = \alpha \cdot V_{CSmax} \cdot R_A \quad (2.18)$$

Subtracting equation (2.17) from equation (2.18) gives:

$$(V_{Amax} + V_{ref}^{(\alpha-1)}) \cdot R_{FB} + V_{ref}^{(\alpha-1)} \cdot R_A = 0 \quad (2.19)$$

$$(V_{Amax} + V_{ref}^{(\alpha-1)}) \cdot R_{FB} = V_{ref}^{(\alpha-1)} \cdot R_A \quad (2.20)$$

Equation (2.20) can be rewritten as:

$$R_A = \frac{(V_{Amax} + V_{ref}^{(\alpha-1)}) \cdot R_{FB}}{V_{ref}^{(\alpha-1)}} = \beta \cdot R_{FB} \quad (2.21)$$

R_A is calculated by selecting R_{FB} and solving equation (2.21). Substituting for R_A in equation (2.13) from equation (2.21) and rewriting gives:

$$V_{CSmax} = \frac{V_{ref} \cdot (R_{FB} + R_A)}{R_A} = \frac{V_{ref} \cdot (1+\beta) \cdot R_{FB}}{\beta \cdot R_{FB}}$$

$$= \frac{V_{ref} \cdot (1+\beta)}{\beta} = V_{ref} \cdot \left(1 + \frac{1}{\beta}\right)$$

$$= V_{sense} \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}}$$

$$= \left(\frac{2}{\pi} \cdot \sqrt{2} \cdot I_{Lamp} \cdot R_{sense} - V_{DF}\right) \cdot \frac{R_{cs2}}{R_{cs1} + R_{cs2}} \quad (2.22)$$

$$\frac{R_{cs1}}{R_{cs2}} = \frac{V_{sense}}{V_{ref}\left(1 + \frac{1}{\beta}\right)} - 1 \quad (2.23)$$

For example:

$$V_{ref} = 2.5V,\ I_{lampmax} = 6.7mA,\ I_{lampmin} = 4mA,$$

$$R_{FB} = 100k\Omega,\ R_{sense} = 1.5k\Omega,\ R_{CSI} = 10k\Omega$$

From these values, it is possible to obtain the value of R_{CS2}. To get more precise value of RCS2, use an iterative calculation. Use R_{sense} to calculate R_{CS2}, because R_{sense_eq} is unknown. After the first calculation, R_{sense_eq} can be resolved. Calculate the R_{CS2} value using R_{sense_eq}. Calculate iteratively until the previous R_{sense_eq} value becomes almost equal to the current R_{sense_eq} value.

The data to input

The calculated data

	V_{REF}	V_A	I_{lamp}
Min.	–	0	4
Typ.	2.5	-	–
Max.	–	3.2	6.7
			α 0.597014925 6.7

$I_{lamp\_max}/I_{lamp\_min}$

R_{FB}	100	kΩ
R_A	217.6296296	kΩ
b	2.176296296	
V_{CSmax}	3.64874064	
R_{sense}	1.5	kΩ
R_{sense_eff}	1.3861	
Diode drop voltage	0.3	V
Avg_max_{Vsense}	8.061120587	V
R_{CS1}/R_{CS2}	1.209288459	
R_{CS1}	10	kΩ
R_{CS2}	8.269325588	kΩ

$R_{sense\_effective}$ 1.386187316kΩ $= R_{sense}//(R_{CS1}+R_{CS2})$

2.7 Burst Dimming

Lamp intensity is controlled with the BDIM signal. 0V on BDIM commands full brightness. The duty cycle of the burst dimming comparator determines the lamp brightness as a percent of the rated lamp current. Burst dimming is implemented by summing 85µA into the feedback node to turn down the lamp. If there is sufficient voltage for the lamp to strike, the feedback loop controls the lamp at the rated current using a fixed current-sense resistor. When the voltage of EA_IN is brought higher than V_{ref}, EA_OUT becomes low and the MOSFET stops switching. At this time, the resonant tank voltage decays until the lamp extinguishes. C_{FB} is reduced, if possible, to speed up the lamp re-strike. Burst dimming waveforms are shown in Figures 12, 13, and 14.

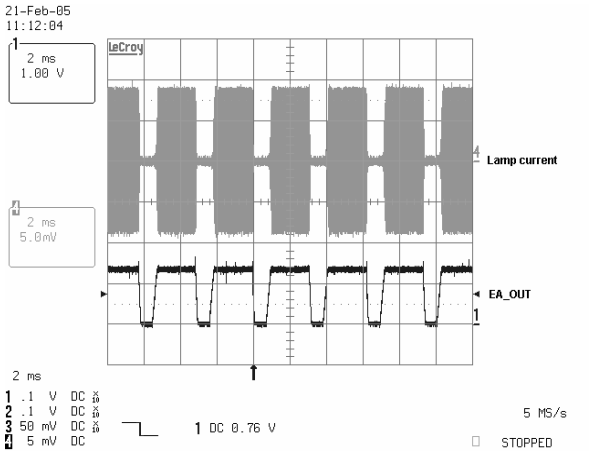


Figure 12. Burst Dimming at 75%

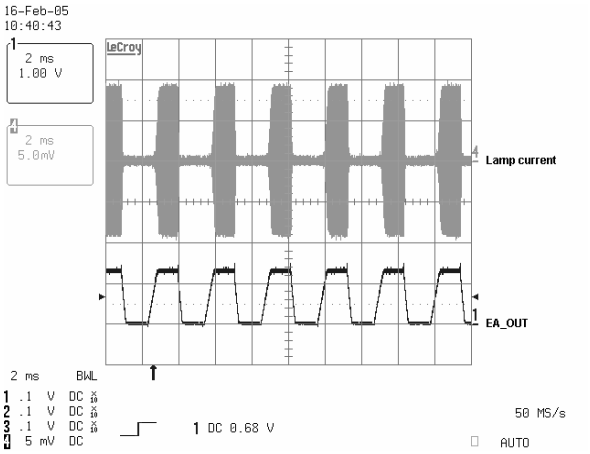


Figure 13. Burst Dimming at 50%

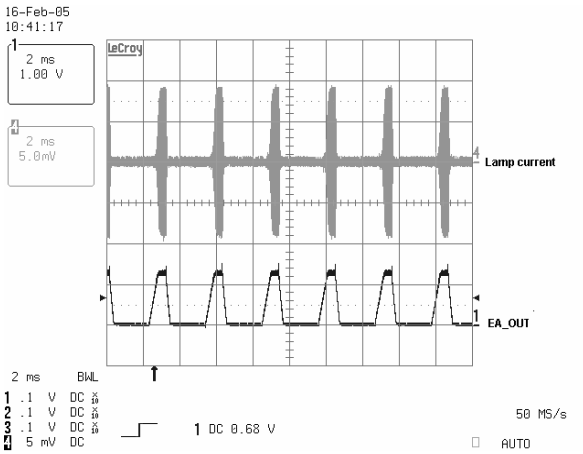


Figure 14. Burst Dimming at 25%

2.8 Open Lamp Regulation and Open Lamp Protection

Power stage operation must be suspended if an open lamp occurs, because the power stage is at high gain. When a voltage higher than 2V is applied to the OLR (Open Lamp Regulation) pin, the part enters the regulation mode and controls EA_OUT voltage to limit the lamp voltage by adding 105µA into the feedback node. The OLP (Open Lamp Protection) capacitor, which is connected to the OLP pin, is charged by the 1.4µA internal current source.

2.8.1 Open Lamp at Initial Operation

OLP voltage starts from 1V. After reaching 2.5V, the IC shuts down when all the output are high.

The relationship between the OLP capacitor and the time ΔT before the IC shuts down is calculated using the approximation I = CΔV/ΔT, where I = 1.4µA, ΔV = 1.5V, resulting in ΔT(s) = 1.1C(µF).

2.8.2 Normal Operation and Open Lamp

OLP voltage starts at 0V. After reaching 1.5V, the IC shuts down when all the outputs are high.

The relationship between the OLP capacitor and the time ΔT before the IC shuts down is calculated using the approximation I = CΔV/ΔT, where I = 1.4µA, ΔV = 1.5V, resulting in ΔT(s) = 1.1C(µF).

2.8.3 OLP Operation

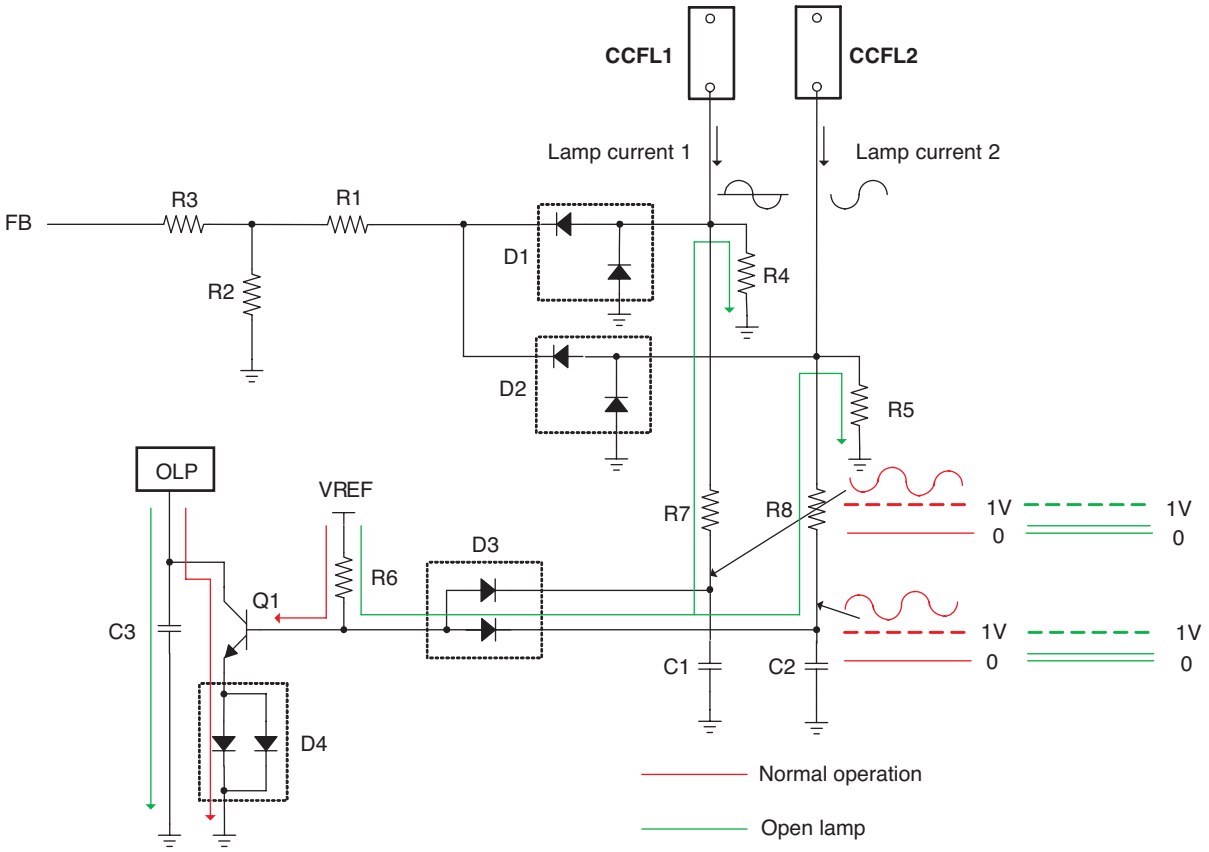
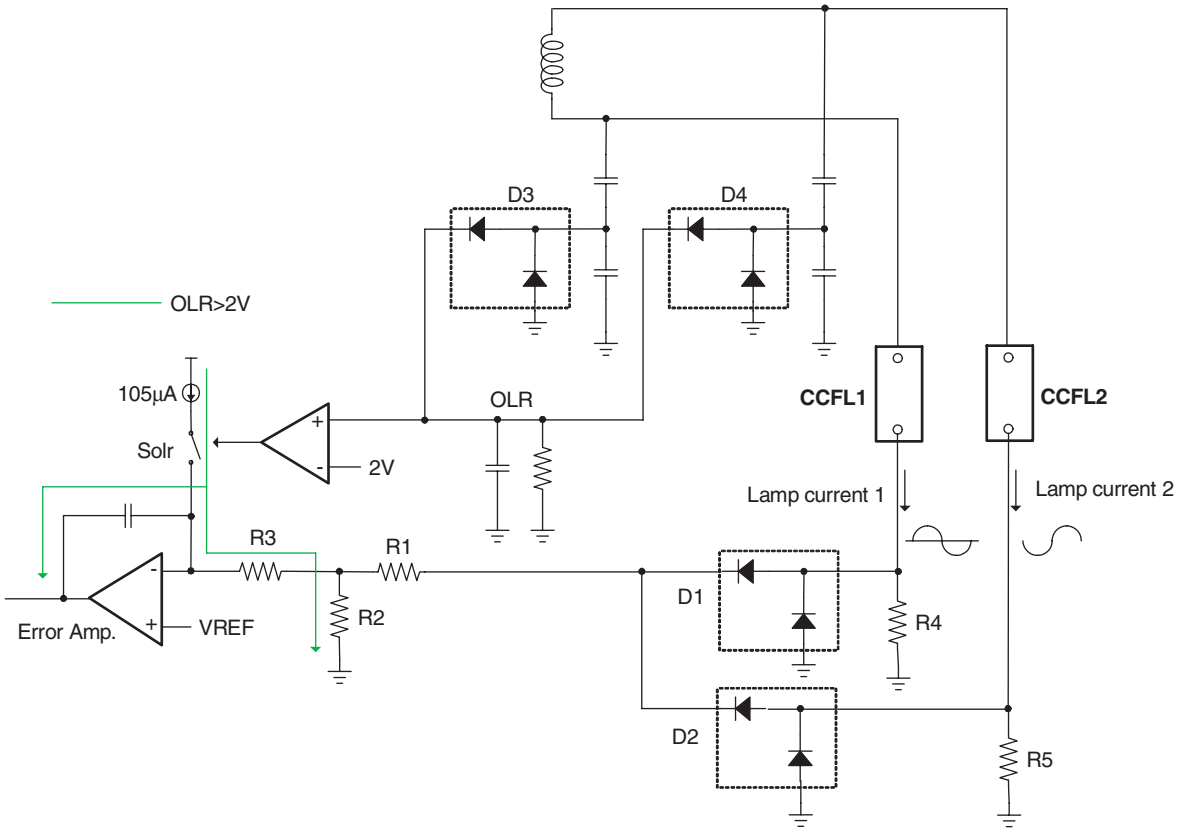


Figure 15. Operating OLP

In normal operation, the voltage of D3's cathode is over 1V and D3 is turned off; Q1 is on; and OLP remains low. When open lamp occurs, the voltage of D3's cathode is under 1V and either D3 is turned on. Then Q1 is turned off and OLP start charging by an internal current source of 1.4µA. If OLP reaches 2V, the IC is shut down. The base current of Q1 should be more than 1.4µA/hfe. R6 is determined by this condition. R4, R5, R7, and R8 are determined so that Q1 and D4 are turned off in the open lamp condition. C1 and C2 are determined so that the voltage of D3's cathode is over 1V in normal operation.

2.8.4 OLR Operation



OLR > 2V ↑ → Solr on duty ↑ → EA_IN ↑ → EA_OUT ↑ → Switching duty ↑ → Lamp voltage ↓
→ OLR > 2V ↓ → Solr on duty ↓ → EA_IN → EA_OUT ↓ → Switching duty ↑ → Lamp voltage ↑

Figure 16. Operating OLR

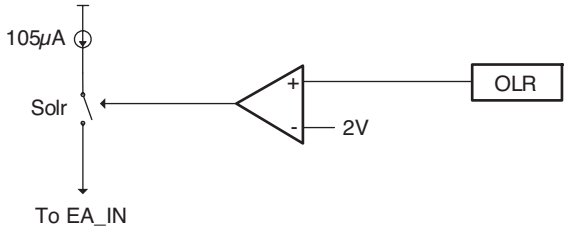


Figure 17. Open Lamp Regulation Circuit

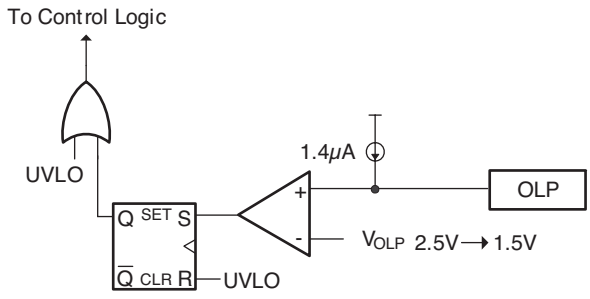


Figure 18. Open Lamp Protection Circuit

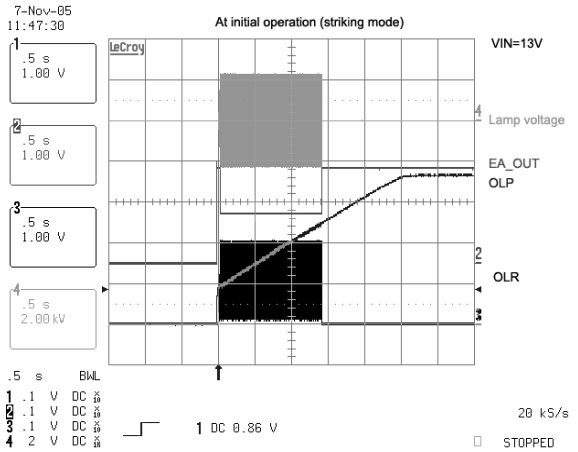
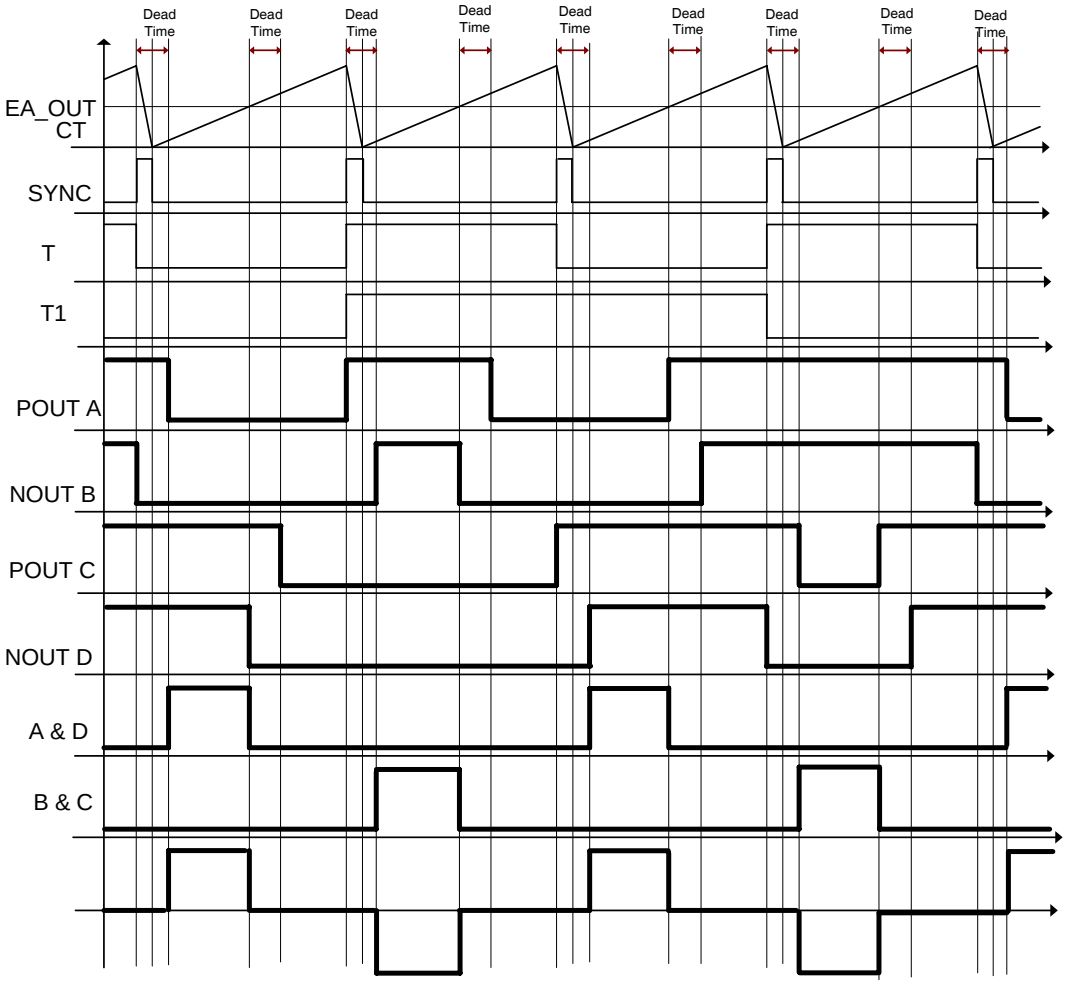


Figure 19. OLR Voltage During Striking Mode

2.9 Output Driver

The four output drives are designed so that the two pairs of switches, pair A and B and pair C and D, never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair drives the other half-bridge. The detailed timing relationship is shown below.



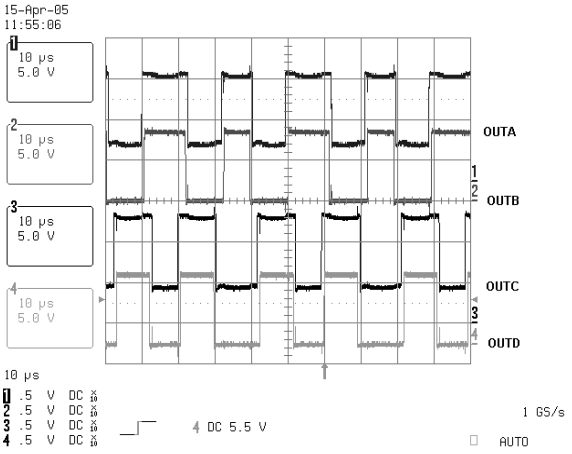
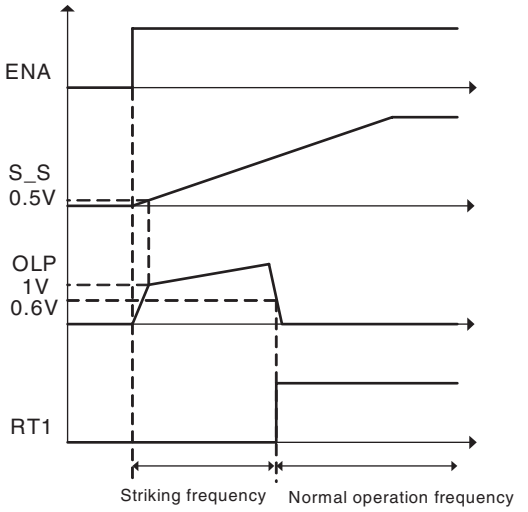


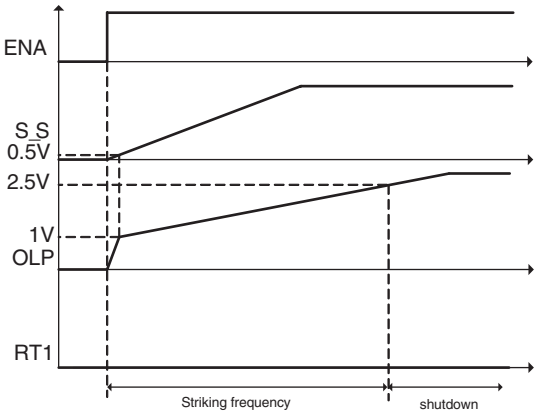
Figure 20. New Phase Shift Control Waveforms

2.10 CCFL Striking Sequence



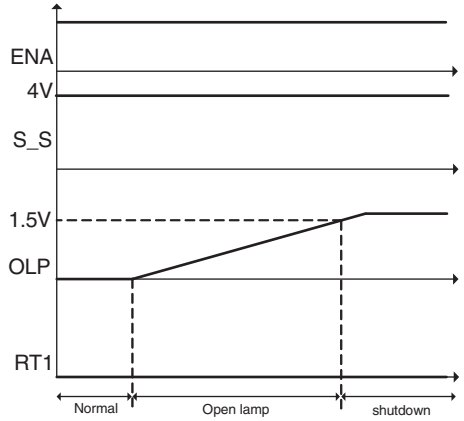
$$F_{st} = \frac{19}{64} \cdot \frac{1}{(R_T // R_{T1}) \cdot C_T} \qquad F_{nor} = \frac{19}{64} \cdot \frac{1}{(R_T // R_{T1}) \cdot C_T}$$

Figure 21. CCFL Ignites



$$F_{st} = \frac{19}{64} \frac{1}{(R_T // R_{T1}) \cdot C_T}$$

Figure 22. CCFL Does Not Ignite



$$F_{nor} = \frac{19}{64} \cdot \frac{1}{(R_T // R_{T1}) \cdot C_T}$$

Figure 23. Open Lamp

2.11 PCB Layout Guideline

1. Separating ground for analog and power portions of circuitry is one of the simplest and most effective methods of noise suppression. This is shown in Figure 24.
2. The traces between drive output and the MOSFET gates should be as short as possible and as wide as possible.
3. The traces of R_T, C_T, and BC_T should be kept away from high-current components and traces.

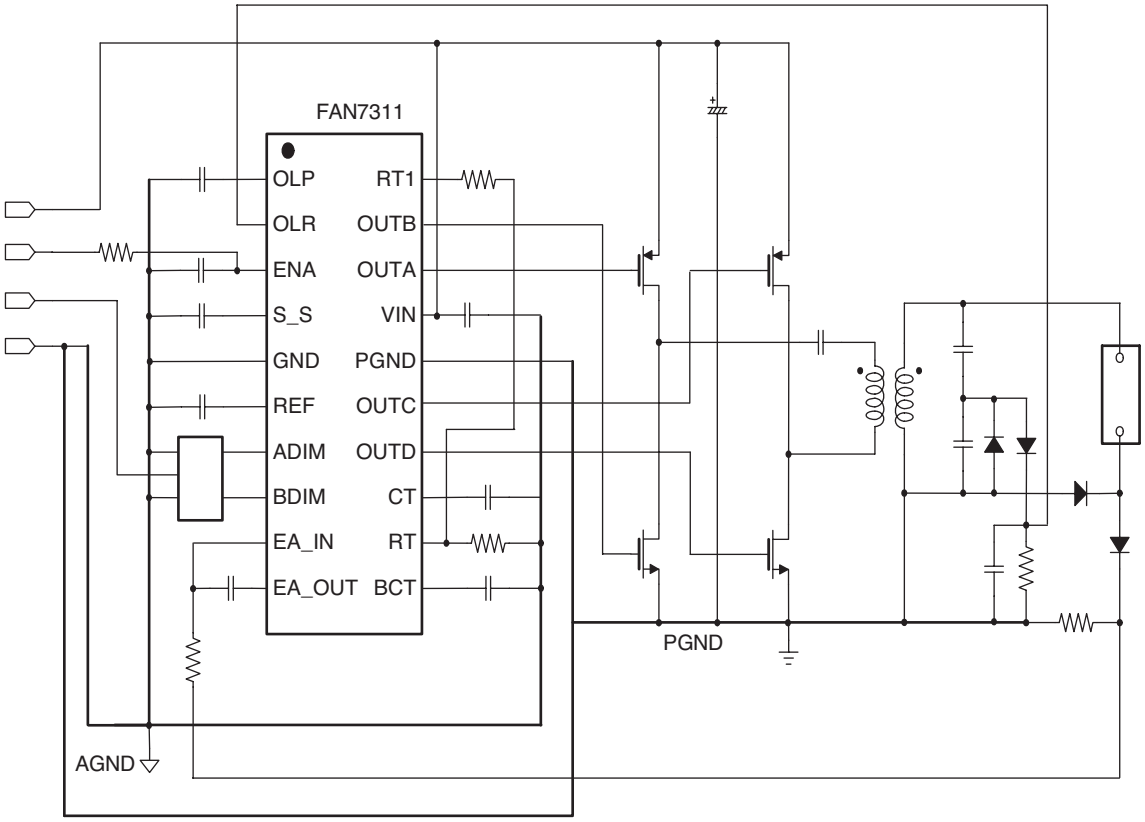


Figure 24. PCB Layout

3. Power Stage Design

3.1 Resonant Circuit

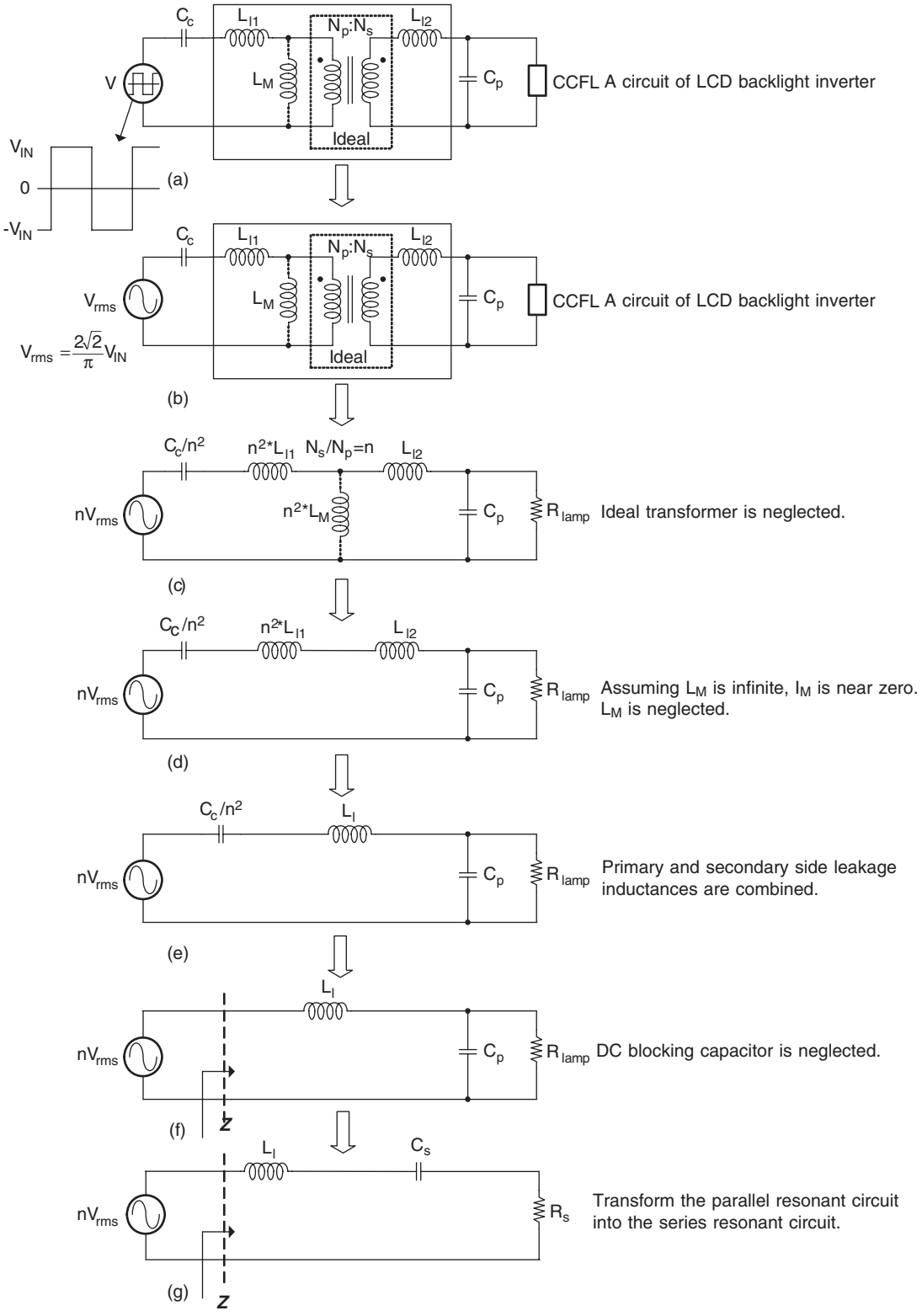


Figure 25. Resonant Circuit

The resonant circuit (f) in Fig. 25 is a second-order low-pass filter and can be described by the following normalized parameters:

- The corner frequency:

$$\omega_0 = \frac{1}{\sqrt{L_I C_p}} \tag{3.1}$$

- The characteristic impedance:

$$Z_0 = \omega_0 L_I = \frac{1}{\omega_0 C_p} = \sqrt{\frac{L_I}{C_p}} \tag{3.2}$$

- The loaded quality factor at the corner frequency f_o:

$$Q_L = \omega_0 C_p R_{lamp} = \frac{R_{lamp}}{\omega_0 L_I} = \frac{R_{lamp}}{Z_0} \tag{3.3}$$

- The resonant frequency that forms the boundary between capacitive and inductive loads:

$$\omega_r = \frac{1}{\sqrt{L_I C_s}} \tag{3.4}$$

- The loaded quality factor at the resonant frequency f_r:

$$Q_r = \frac{\omega_r L_I}{R_s} = \frac{1}{\omega_r C_s R_s} \tag{3.5}$$

- The input impedance of the resonant circuit (f) in Fig. 25 is:

$$Z = j\omega L + \frac{R_{lamp} \cdot \frac{1}{j\omega C_p}}{R_{lamp} + \frac{1}{j\omega C_p}} = \frac{R_{lamp}\left[1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{1}{Q_L}\left(\frac{\omega}{\omega_0}\right)\right]}{1 + jQ_L\left(\frac{\omega}{\omega_0}\right)}$$

$$= Ze^{j\varphi} = R_S + jX_s \tag{3.6}$$

where,

$$\frac{Z}{Z_0} = \sqrt{\frac{Q_L^2\left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]^2 + \left(\frac{\omega}{\omega_0}\right)^2}{1 + \left(Q_L\frac{\omega}{\omega_0}\right)^2}} \tag{3.7}$$

$$\varphi = \arctan\left\{Q_L\left(\frac{\omega}{\omega_0}\right)\left[\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q_L^2} - 1\right]\right\} \tag{3.8}$$

$$R_S = Z\cos\varphi \tag{3.9}$$

$$X_S = Z\sin\varphi \tag{3.10}$$

- The resonant frequency, f_r, is defined as a frequency at which the phase shift is zero. The ratio of f_r to the corner frequency, f_o, is:

$$\frac{f_r}{f_0} = \sqrt{1 - \frac{1}{Q_L^2}}, \quad \text{for} \quad Q_L \geq 1 \tag{3.11}$$

The loaded quality factors Q_L and Q_r are related by:

$$Q_r = \frac{\omega_r L}{R_s} = \frac{1}{\omega_r C_s R_s} = \omega_r C_p R_{lamp}$$

$$= Q_r\left(\frac{\omega_\rho}{\omega_0}\right) = \sqrt{Q_L^2 - 1}, \quad \text{for} \quad Q_L \geq 1 \tag{3.12}$$

3.2 Voltage Transfer Function

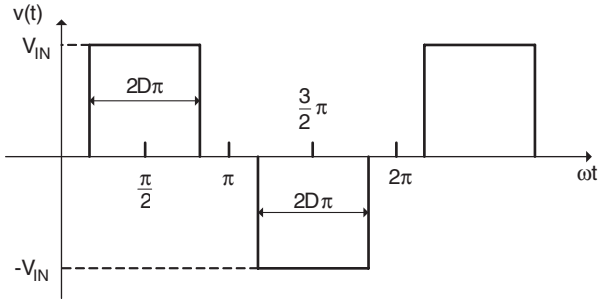


Figure 26. Input Voltage of the Resonant Circuit

As shown in Fig. 26, the input voltage of the resonant circuit v is a square wave of magnitude V_{IN}, given by:

$$\begin{aligned}
&v = 0, \text{ for } 0 < \omega t \leq \left(\frac{1}{2} - D\right)\pi \\
&v = V_{IN}, \text{ for } \left(\frac{1}{2} - D\right)\pi < \omega t \leq \left(\frac{1}{2} - D\right)\pi \\
&v = 0, \text{ for } \left(\frac{1}{2} + D\right)\pi < \omega t \leq \left(\frac{3}{2} - D\right)\pi \\
&v = -V_{IN}, \text{ for } \left(\frac{3}{2} - D\right)\pi < \omega t \leq \left(\frac{3}{2} - D\right)\pi \\
&v = 0, \text{ for } \left(\frac{3}{2} - D\right)\pi < \omega t \leq 2\pi
\end{aligned} \tag{3.13}$$

The fundamental component of this voltage is:

$$v_{i1} = V_m \sin(\omega t), \tag{3.14}$$

in which the amplitude of v_{i1} can be found from Fourier analysis as:

$$V_m = \frac{4}{\pi} V_{IN} \sin D\pi \tag{3.15}$$

You can obtain the rms value of v_{i1}:

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{2\sqrt{2}}{\pi} V_{IN} \sin D\pi \tag{3.16}$$

Which leads to the voltage transfer function from V_{IN} to the fundamental component at the input of the resonant circuit:

$$M_{Vs} = \frac{V_{rms}}{V_{IN}} = \frac{2\sqrt{2}}{\pi} \sin D\pi \tag{3.17}$$

According to Fig. 25(f), the voltage transfer function of the resonant circuit is:

$$M_{Vr} = \frac{V_{Ri}}{\sqrt{2}\cdot nV_{rms}} = \frac{\dfrac{\dfrac{R_{lamp}}{j\omega C_p}}{R_{lamp}+\dfrac{1}{j\omega C_p}}}{j\omega L+\dfrac{\dfrac{R_{lamp}}{j\omega C_p}}{R_{lamp}+\dfrac{1}{j\omega C_p}}}$$

$$= \frac{1}{1-\left(\frac{\omega}{\omega_0}\right)^2+j\frac{1}{Q_L}\left(\frac{\omega}{\omega_0}\right)} = M_{Vr}{}^{j\varphi} \qquad (3.18)$$

where,

$$M_{Vr} = \frac{V_{Ri}}{nV_{rms}} = \frac{1}{\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2+\frac{1}{Q_L{}^2}\left(\frac{\omega}{\omega_0}\right)^2}} \qquad (3.19)$$

$$\varphi = -\arctan\left[\frac{\frac{1}{Q_L}\left(\frac{\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right] \qquad (3.20)$$

The maximum value of MVr is obtained by differentiating the quantity under the square-root sign with respect to f/fo and setting the result equal to zero. Hence, the normalized peak frequency is:

$$\frac{f_{pk}}{f_0} = 0, \text{ for } 0 \le Q_L \le \frac{1}{\sqrt{2}} \qquad (3.21)$$

$$\frac{f_{pk}}{f_0} = \sqrt{1-\frac{1}{4Q_L{}^2}}, \text{ for } Q_L \le \frac{1}{\sqrt{2}}$$

resulting in the maximum magnitude of the voltage transfer function of the resonant circuit:

$$M_{Vr(max)} = 1, \text{ for } 0 \le Q_L \le \frac{1}{\sqrt{2}}$$

$$M_{Vr(max)} = \frac{Q_L}{\sqrt{1-\frac{1}{4Q_L{}^2}}}, \text{ for } Q_L \le \frac{1}{\sqrt{2}} \qquad (3.22)$$

The magnitude of the DC-to-AC voltage transfer function of the LCD backlight inverter without losses is obtained from (3.17) and (3.22):

$$M_{VI} = \frac{V_{lamp}}{V_{IN}} = M_{Vs}\cdot(nM_{Vr})$$

$$= \frac{2\sqrt{2}\cdot n\sin D\pi}{\pi\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]+\frac{1}{Q_L{}^2}\left(\frac{\omega}{\omega_0}\right)^2}} \qquad (3.23)$$

The maximum magnitude of the DC-to-AC voltage transfer function of the LCD backlight inverter without losses is:

$$M_{VI(max)} = \frac{2\sqrt{2}\cdot n}{\pi}, \text{ for } 0 \le Q_L \le \frac{1}{\sqrt{2}}$$

$$M_{VI(max)} = \frac{2\sqrt{2}\cdot nQ_L}{\pi\sqrt{1-\frac{1}{4Q_L{}^2}}}, \text{ for } Q_L \ge \frac{1}{\sqrt{2}} \qquad (3.24)$$

3.2 Design Procedure

A LCD monitor backlight circuit illustrates a design based on the FAN7311. The inverter is designed to drive two CCFLs with the following specifications.

Panel Model	LM151X2(LG.PHILIPS LCD)
Input Voltage	9 ~ 15V
Striking Voltage	880Vrms
Operating Voltage	585Vrms (Typ.)
Operating Current	8mArms (Typ.)
Operating Frequency	50kHz (Typ.)
Rated Power	4.68W/CCFL
Efficiency	85% (Typ.)

1) Select Transformer's Primary Turns

The number of primary turns is determined by Faraday's law. $N_{p,min}$ is fixed by the minimum voltage across the primary and the maximum on time.

$$N_{p,min} = \frac{V_{IN,min}\cdot\Delta t_{max}}{\Delta B\cdot A_e}$$

where $N_{p,min}$ = Minimum number of primary turns
$V_{IN,min}$ = Minimum input voltage (Volts)
ΔB = Core magnetic flux density change (Tesla)
Δt_{max} = Maximum overlap on-time of diagonal MOSFET switches (us)
A_e = Core cross-sectional area (mm^2)

A transformer used in a full-bridge topology operates in two quadrants of the B-H curve such that the maximum magnetic flux density is $B_{max} = 0.5\Delta B$. For most cores, saturation magnetic flux density is about 400mT. Margin considered, determine that the maximum magnetic flux density B_{max} = 0.5 Bsat, so the maximum magnetic flux density is B_{max} = 200mT. In an example with a minimum voltage of 9V, operating frequency 50KHz, maximum on time of diagonal MOSFET switches of 10μs and a core cross-sectional area (EPC17, EPC19, EFD1820) of $22mm^2$, the minimum number of primary turns required is:

$$N_{p,min} = \frac{V_{IN,min}\cdot\Delta t_{max}}{\Delta B\cdot A_e} = \frac{9\cdot 10}{400\cdot 22} \approx 10T_s$$

2) Select Q_L and Operation Frequency to Determine the Turns Ratio

Select a value of 1 for Q_L. Assume that $f_{op} = f_{pk} = 50kHz$ based on the LCD panel specification. From (3.21), the corner frequency is:

$$f_o = \frac{f_{pk}}{\sqrt{1-\frac{1}{2Q_L^2}}} = \frac{50}{\sqrt{1-\frac{1}{2\cdot 1.1^2}}} = 70.7(kHz)$$

From (3.11), the resonant frequency that forms the boundary between capacitive and inductive loads is:

$$f_r = f_o \cdot \sqrt{1-\frac{1}{Q_L^2}} = f_{pk} \cdot \frac{\sqrt{1-\frac{1}{Q_L^2}}}{\sqrt{1-\frac{1}{2Q_L^2}}} = 0(kHz)$$

Therefore, zero-voltage switching (ZVS) can be achieved at any operating frequency. For the reference design, the required secondary lamp voltage is 585V and the minimum voltage is 9V. Therefore, from (3.23), the minimum number of the turns ratio is:

$$n \geq \frac{585}{9} \cdot \frac{\pi\sqrt{\left[1-\left(\frac{\omega_{op}}{\omega_0}\right)^2\right]^2+\frac{1}{Q_L^2}\left(\frac{\omega_{op}}{\omega_0}\right)^2}}{2\sqrt{2}\sin D\pi} \approx 62.5T_s,$$

$$\therefore M_{VI} = \frac{2\sqrt{2}\cdot n\sin D\pi}{\pi\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2+\frac{1}{Q_L^2}\left(\frac{\omega}{\omega_0}\right)^2}} \geq \frac{585}{9}$$

3) Determine the Required Output Capacitance

Using the above specifications, the equivalent resistance of a CCFL is:

$$R_{lamp} = \frac{V_{lamp}}{I_{lamp}} = \frac{585}{0.008} \approx 75(k\Omega)$$

The corner frequency is 70.7kHz. Assume a parasitic capacitance per lamp of 10pF. Each parasitic capacitance is effectively in parallel with each of the output capacitors.

The output capacitor is:

$$C_{out} = C_p - C_{para} = \frac{Q_L}{\omega_o R_{lamp}} - 10pF \approx 21pF,$$

$$\therefore Q_L = \omega_o R_{lamp} C_p$$

Using (3.3), the value of the leakage inductance is:

$$L_I = \frac{1}{\omega_o^2 C_p} \approx 164.6(mH)$$

Note: Considering minimum primary turns, minimum turns ratio, and leakage inductance, determine primary turns, turns ratio, and the gap of core to get the required leakage inductance. For the sample design, the number of primary turns is $30T_s$ and that of the secondary turns is $2200T_s$. Turns ratio is 66.7.

4) Select the Proper Wire Gauges for the Primary and Secondary Transformer Windings

The approximate primary winding rms current I_p and approximate secondary winding rms current I_s are determined by the following equations.

$$I_p = \frac{\pi}{2\sqrt{2}} \cdot \frac{P_{lamp}}{\eta V_{IN}},$$

$$\therefore P_{lamp} = \eta V_{IN} I_{IN},\ I_{IN} = \frac{2\sqrt{2}}{\pi} I_p$$

$$I_s = \sqrt{I_{lamp}^2 + [2\pi f_{op} C_{out} V_{lamp}]^2}$$

Values that must be known or selected initially:

Parameter	Description	Typical Value	Units
V_{lamp}	Nominal lamp operating voltage	585	V
I_{lamp}	Nominal lamp operating current	8	mA
f_{op}	Operating frequency	50	kHz
f_{pk}	Peak frequency	50	kHz
V_{in}	Input voltage	9	V
D	Duty ratio at input voltage	50	%
Q_L	Loaded factor at the corner frequency	1	
C_{para}	Parasitic capacitance	10	pF
A_e	Core cross-sectional area	22	mm^2
B_{sat}	Saturation magnetic flux density	0.4	T
$AL_{leakage}$	AL value of leakage inductance	22	nH/N^2

Values that are calculated:

B_{max}	Maximum magnetic flux density	0.2	T
ΔB	Core magnetic flux density change	0.4	T
Δt_{max}	Maximum overlap on-time of diagonal switches	10	µs
f_o	Corner frequency	70.71067812	kHz
f_r	Resonant frequency	0	kHz
R_{lamp}	Equivalent resistance of a CCFL	73.125	k¾
$N_{p,min}$	The minimum number of transformer's primary turns	10	Turns
n_{min}	The minimum number of the turns ratio	62.5	
C_{out}	The output capacitor	20.78	pF
L_l	The leakage inductance of the transformer	164.59	mH
N_p	The number of transformer's primary turns	31	Turns

Values that must be selected with more than minimum turn ratio.

n	The number of the turns ratio	62.5	

The values that are calculated:

N_s	The number of transformer's secondary turns	1934.1	Turns