Application Note AN6012

Design of Power Factor Correction Circuit Using FAN7528

1. Introduction

The FAN7528 is an active power factor correction (PFC) controller for the boost PFC application which operates in the critical conduction mode (CRM). The critical conduction mode boost power factor converter operates at the boundary of continuous conduction mode and discontinuous conduction mode. The CRM PFC controllers are of two kinds: the current mode CRM PFC controller and the voltage mode CRM PFC controller. For the current mode, a boost switch is turned on when the inductor current reaches zero and turned off when the inductor current meets the desired current reference. In this case, the rectified AC line voltage should be sensed to generate the current reference as in the FAN7527B, however the sensing network can cause additional power loss. In the voltage mode, the switch turn-on is the same as that of the current mode, but the switch turn-off is determined by an internal ramp signal. The ramp signal is compared with an error amplifier output and the switch turn-on time is controlled to be constant as shown in Fig. 1. If the turn-on time is constant, the peak inductor current is proportional to the rectified AC line voltage as shown in Fig. 2. In this way, the input current waveform follows the waveform of the input voltage, thereby obtaining a good power factor. The FAN7528 is a voltage mode CRM PFC controller. Because the voltage mode CRM PFC controller does not need the rectified AC line voltage information, it can save the power loss of the sensing network.

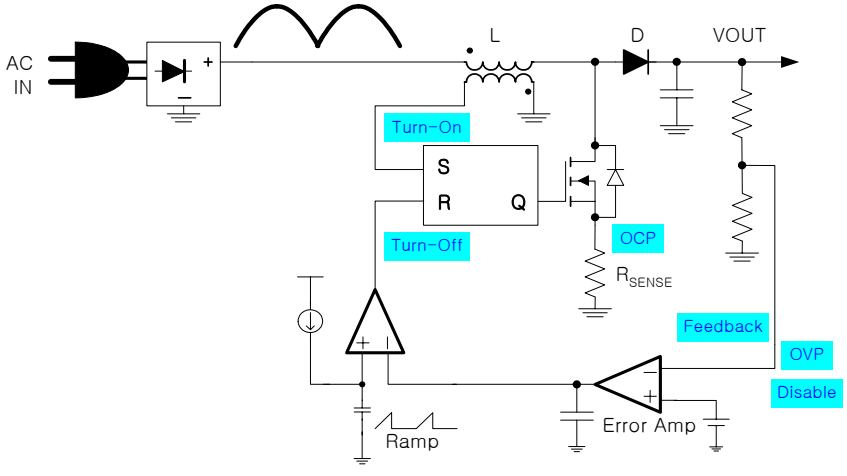

Figure 1. Voltage Mode CRM Boost PFC Circuit

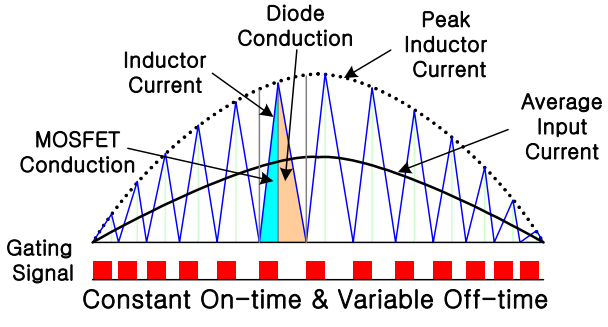

Figure 2. CRM Boost PFC Inductor Current Waveform

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Unlike the conventional fixed output CRM PFC controllers, the FAN7528 has the dual output control function according to the AC line voltage without sensing the rectified AC line voltage. As shown in Fig. 3, the boost output voltage is proportional to the peak value of the AC line voltage before the IC starts switching. Because the feedback loop senses the output voltage, the sensed output voltage information can be used to get the information of the AC line voltage range, which is 100Vac for Japan and America and 220Vac for EU. Based on this information, the FAN7528 changes the internal reference voltage to be 1.5V for low line condition and 2.5V for high line condition. As shown in Figures 4 and 5, the output voltage is controlled to be 240V when the AC line voltage is 90Vac and 400V when it is 264Vac.

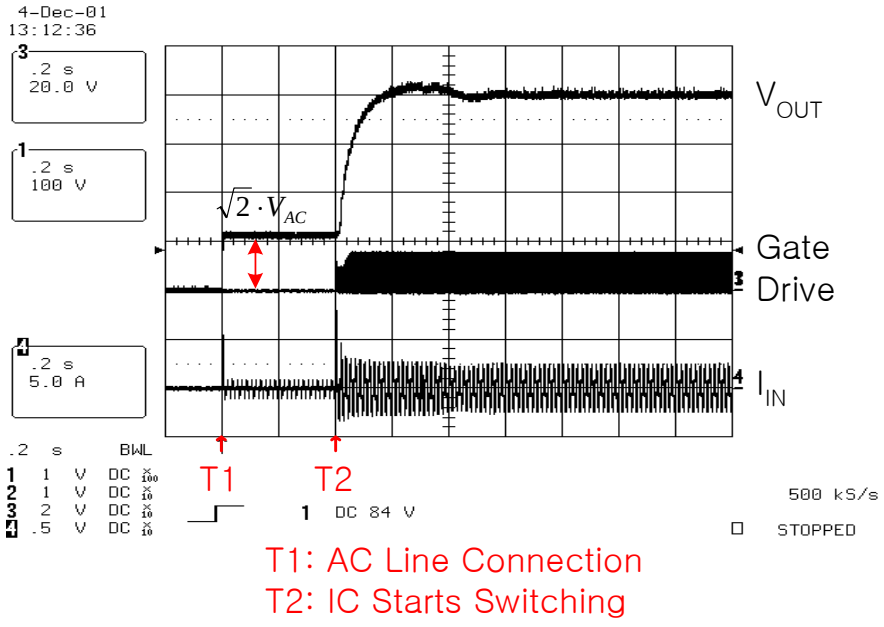

Figure 3. Typical Start-up Waveform

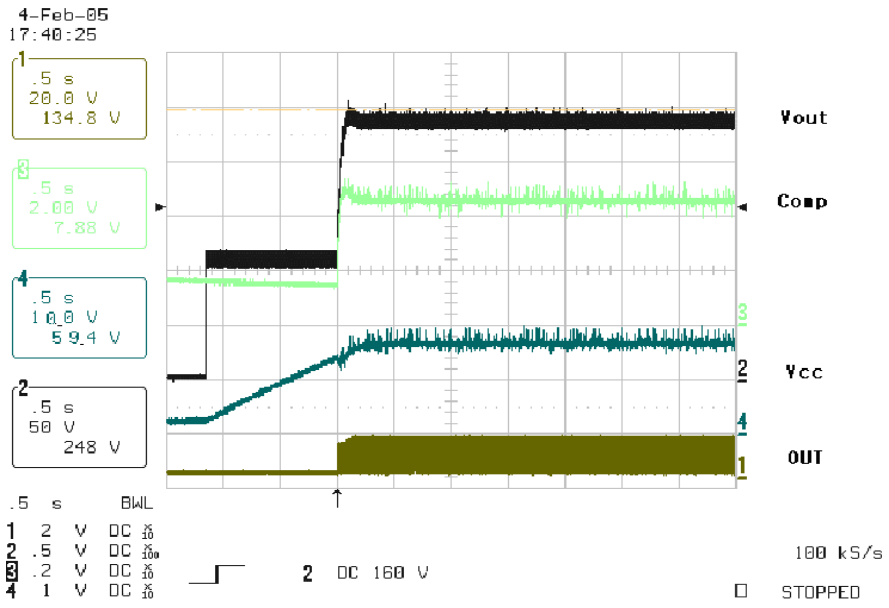

Figure 4. FAN7528 Start-up Waveform When 90Vac

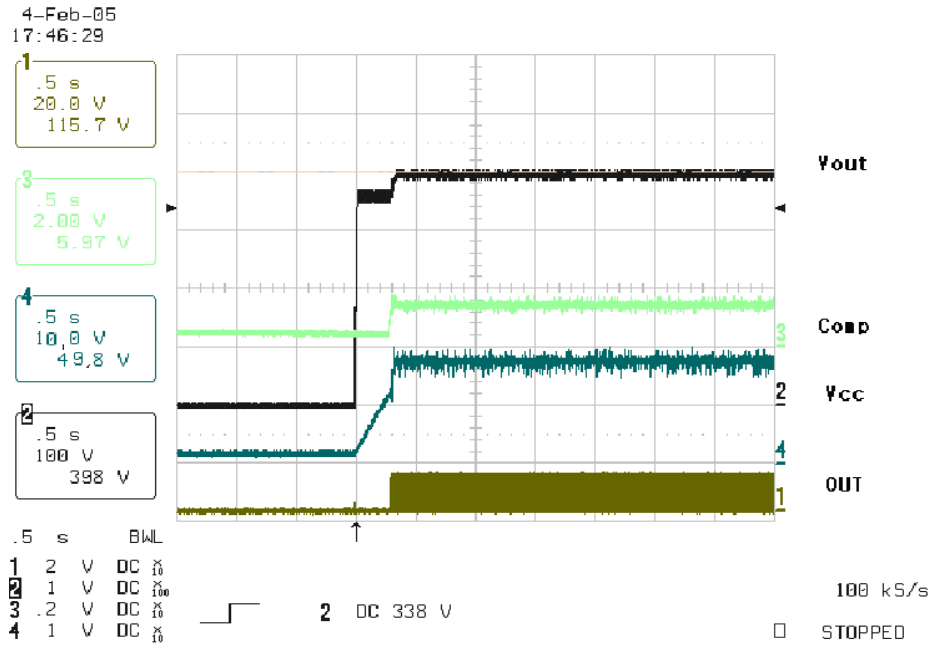

Figure 5. FAN7528 Start-up Waveform When 264Vac

Fig. 6 shows the block diagram of the FAN7528.

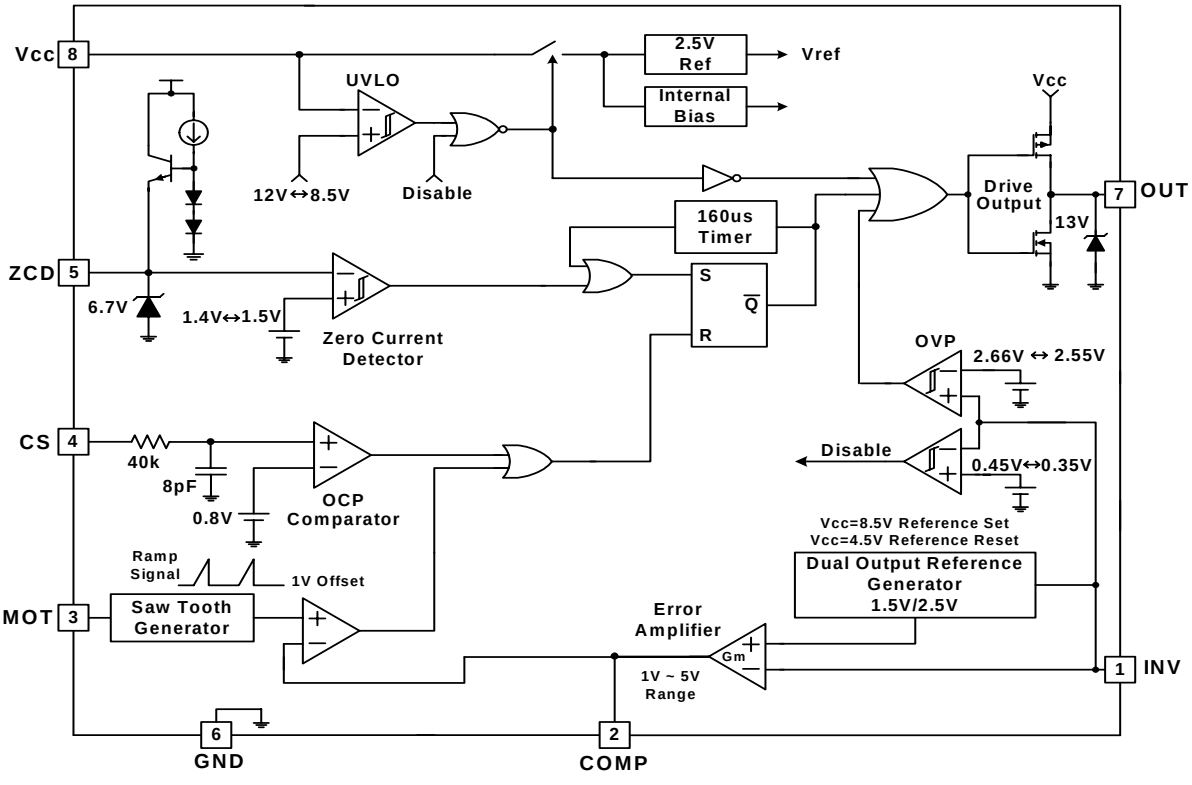

Figure 6. Block Diagram of the FAN7528

It contains following blocks.

- Error amplifier block
- Zero current detector block
- Saw tooth generator block
- Over current protection block
- Switch drive block

2. Device Block Description

2.1 Error Amplifier Block

The error amplifier block consists of a transconductance amplifier, dual output reference generator, output OVP comparator and disable comparator. For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) is good for the implementation of OVP and disable function. The output current of the amplifier changes according to the voltage difference of the inverting input and the non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the switch turn-off signal. The dual output reference generator changes the reference voltage for the non-inverting input according to the voltage level of the inverting input before the FAN7528 starts switching. When the AC line is connected to the boost converter, Vcc voltage starts to increase from zero voltage. If the Vcc voltage reaches 8.5V, the dual output reference generator compares the INV pin voltage with the 1.3V reference, and if the INV pin voltage is higher than 1.3V, the reference voltage is set to be 2.5V; and if it is lower than 1.3V, the reference voltage is set to be 1.5V. If the PFC output is set to be 400V at high line, the PFC output voltage is 240V (=400*1.5/2.5) at low line. The reference voltage is reset when the Vcc is lower than 4.5V. The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.66V and there is 0.11V hysteresis. The disable comparator disables the operation of the FAN7528 when the voltage of the inverting input is lower than 0.45V and there is 100mV hysteresis. An external transistor can be used to disable the IC as shown in Fig. 7. The IC operating current decreases under 65uA to reduce power consumption if the IC is disabled.

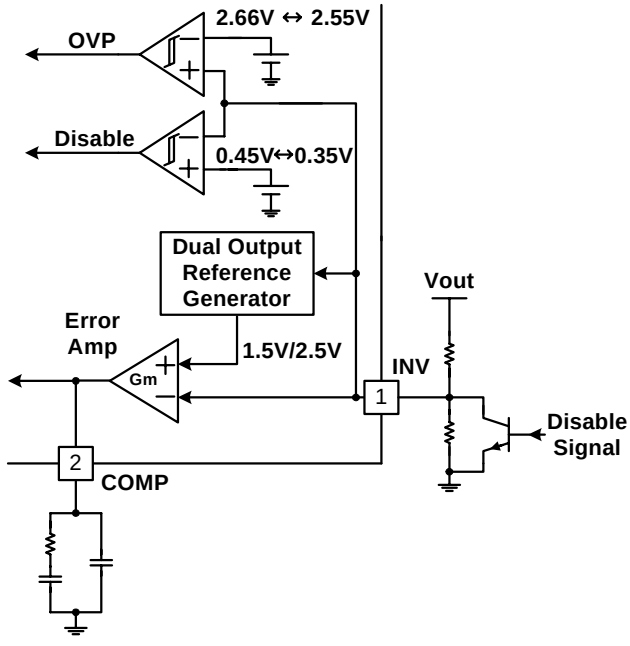

Figure 7. Error Amplifier Block

Table 1 summarizes high line output voltage (V_{O_high}), low line output voltage (V_{O_low}), dual output selection AC line voltage and OVP level. If you set the high line output voltage to be 400V, the low line output voltage is 240V and the dual output selection AC line voltage is 147Vac. If the AC line voltage is higher than 147Vac, the output voltage is controlled to be 400V. And the OVP level is 426V.

Table 1. Output Voltage Setting

V_{o_high}	V_{o_low}	Dual Output Selection AC line Voltage	OVP Voltage
400V	240V	147Vac	426V
395V	237V	145Vac	420V
390V	234V	143.4Vac	415V
385V	231V	141.6Vac	410V
380V	228V	140Vac	404V

2.2 Zero Current Detection Block

The zero current detector (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. Because the polarity of the auxiliary winding is opposite to the inductor winding, the auxiliary winding voltage is negative and proportional to the rectified AC line voltage when the MOSFET is turned on. If the MOSFET is turned off, the voltage becomes positive and proportional to the difference between Vout and Vin. If the inductor current reaches zero, the junction capacitor of the MOSFET resonates with the boost inductor, and then the auxiliary winding voltage decreases resonantly. If it reaches 1.4V, the zero current detector turns on the MOSFET. The ZCD pin is protected internally by two clamps: the 6.7V high clamp and the 0.6V low clamp as shown in Fig. 8.

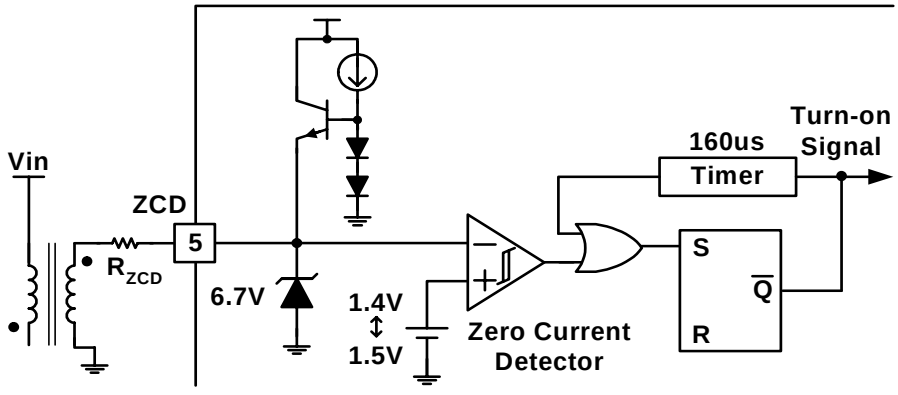

Figure 8. Zero Current Detector Block

Fig. 9 shows typical ZCD related waveforms. Because the ZCD pin has some capacitance, there can be some delay caused by R_{zcd} and the turn-on time can be delayed. Ideally, the switch must be turned on when the inductor current reaches zero; but because of the structure of the ZCD block and R_{zcd} delay, it is turned on after some delay time. During this delay time, the stored charge of the Coss (MOSFET output capacitor) is discharged through the path indicated in Fig. 10. This charge is transferred into a small filter capacitor, C_{in1}, which is connected to the bridge diode. Therefore, there is no current flow from the input side, meaning the input current I_{in} is zero during this period. For better total harmonic distortion (THD), it is important to make t_{zero} / T_S as small as possible. As shown in Fig. 9, t_{zero} is proportional to $\sqrt{L \cdot C_{oss}}$ but t_{on} and t_{dis} are proportional to L. Therefore t_{zero} / T_S is approximately inversely proportional to $\sqrt{L}$. Therefore THD increases as the inductance decreases. Reducing the inductance can decrease the inductor size and cost but the switching loss increases because of the increased switching frequency.

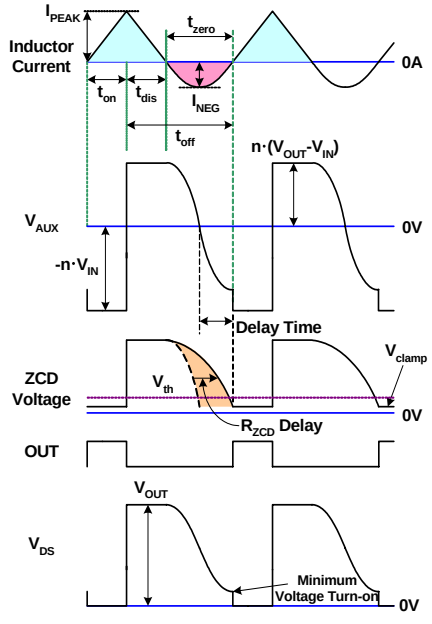

Figure 9. Zero Current Detector Waveform

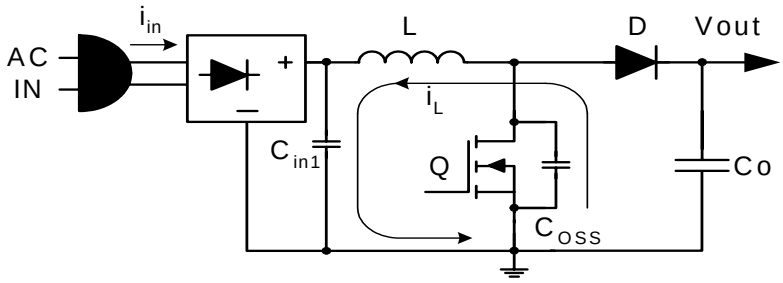

Figure 10. Current Flow During t_{zero}

In the ZCD block, there is an internal timer to provide a means to start or restart the switching if the drive output has been low for more than 160us from the falling edge of the drive output. Without this timer, the PFC converter does not work because the inductor current is always zero when the IC initially starts operation and the ZCD winding voltage does not become positive without any switching.

2.3 Saw Tooth Generator Block

The output of the error amplifier and the output of the saw tooth generator are compared to determine the MOSFET turn-off instant. The slope of the saw tooth is determined by an external resistor connected at the MOT (maximum on time) pin. The voltage of the MOT pin is 1V and the slope is proportional to the current flowing output of the MOT pin. The maximum on time is determined when the output of the error amplifier is 5V. When a 13.7kΩ resistor is connected the maximum on time is 22.5us. As the resistance increases the maximum on time increases because the slope decreases. The MOSFET on time is zero when the output of the error amplifier is lower than 1V.

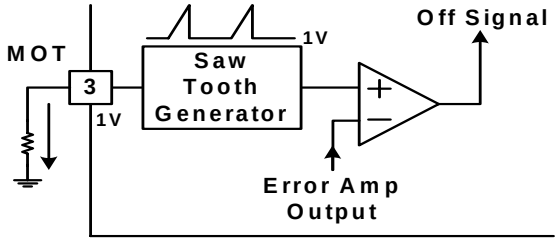

Figure 11. Saw tooth generator block

2.4 Over Current Protection Block

The MOSFET current is sensed using an external sense resistor for over current protection. If the CS pin voltage is higher than 0.8V, the over current protection comparator generates a protection signal to turn off the MOSFET. An internal R/C filter has been included to filter switching noise. This pin is sensitive to negative voltage lower than -0.3V. For proper operation, the stray inductance in the sensing path and the inductance of the sensing resistor must be minimized. If there is abnormal operation caused by negative voltage, connect a shottky diode between the CS pin and ground as shown in Fig. 12.

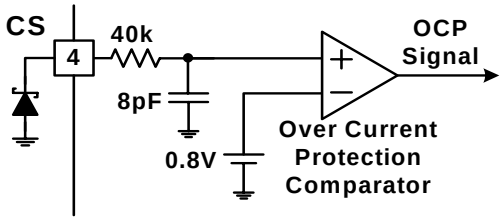

Figure 12. Over current protection block

2.5 Switch drive block

The FAN7528 contains a single totem-pole output stage designed specifically for a direct drive of a power MOSFET. The drive output is capable of up to 400mA peak current with a typical rise and fall time of 50ns with a 1.0nF load. Additional circuitry has been added to keep the drive output in a sinking mode whenever the UVLO is active. The output voltage is clamped to be 13V to protect MOSFET gate even the Vcc voltage higher than 13V.

3.Circuit Components Design

3.1 Power Stage Design

1) Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The minimum switching frequency has to be above the audio frequency (20kHz), to prevent audible noise. The switching period is maximum when the AC line is low and the load is maximum. The maximum switching period, $T_{S(max)}$ is a function of $V_{in(peak\_low)}$ and V_{o_low}, the output voltage, when the AC line is low. It can have maximum value at the highest input voltage or at the lowest input voltage according to V_{o_low}. Compare $T_{S(max)}$ at $V_{in(peak\_min\_low)}$ and $V_{in(peak\_max\_low)}$, and then select the higher value for the maximum switching period. The boost inductor value can be obtained by (6).

$$t_{on} = L\frac{I_{L(peak)}(t)}{V_{in(peak)}\sin(\omega t)} = L\frac{2I_{in(peak)}\sin(\omega t)}{V_{in(peak)}\sin(\omega t)} \quad (1)$$

$$= L\frac{2I_{in(peak)}}{V_{in(peak)}}$$

$$t_{off} = L\frac{I_{L(peak)}(t)}{V_O - V_{in(peak)}\sin(\omega t)} \quad (2)$$

$$= L\frac{2I_{in(peak)}\sin(\omega t)}{V_O - V_{in(peak)}\sin(\omega t)}$$

$$I_{in(peak)} = \frac{2V_O I_O}{\eta \cdot V_{in(peak)}} \quad (3)$$

$$T_S = t_{on} + t_{off}$$

$$= 2LI_{in(peak)}\left(\frac{1}{V_{in(peak)}} + \frac{\sin(\omega t)}{V_O - V_{in(peak)}\sin(\omega t)}\right) \quad (4)$$

$$= \frac{4LV_O I_O}{\eta}\left(\frac{1}{V^2_{in(peak)}} + \frac{\sin(\omega t)}{V_{in(peak)}(V_O - V_{in(peak)}\sin(\omega t))}\right)$$

$$T_{S(max)} = \frac{4LV_O I_{O(max)}}{\eta}\left(\frac{1}{V^2_{in(peak)}} + \frac{1}{V_{in(peak)}(V_O - V_{in(peak)})}\right) \quad (5)$$

$$L = \frac{\eta}{4f_{sw(min)}V_O I_{O(max)}\left(\frac{1}{V^2_{in(peak)}} + \frac{1}{V_{in(peak)}(V_O - V_{in(peak)})}\right)} \quad (6)$$

2) Auxiliary Winding Design

The auxiliary winding voltage is lowest at the highest line. So the turn number of the auxiliary winding can be obtained by (7). This voltage should be higher than the ZCD threshold voltage of 1.5V.

$$N_{aux} > \frac{1.5V \cdot N_P}{(V_O - \sqrt{2}V_{in(peak\_max)})} \quad (7)$$

3) Input Capacitor Design

The voltage ripple of the input capacitor is maximum when the line is lowest and the load is heaviest. If $f_{sw(min)} >> f_{ac}$, the input current can be assumed to be constant during a switching period.

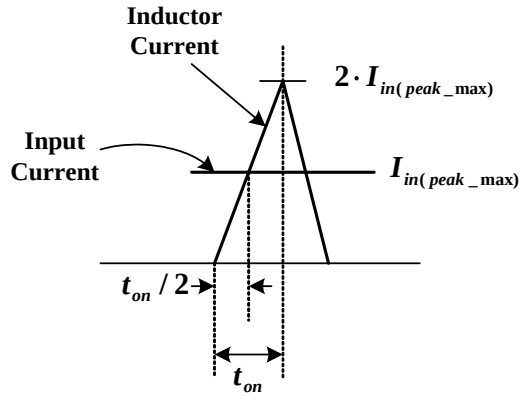

Figure 13. Input Current and Inductor Current Waveform During a Switch Cycle

$$C_{in} \geq \frac{2}{\Delta V_{in(max)}} \cdot \int_0^{\frac{ton}{2}} \left(I_{in(peak\_max)} - \frac{2 \cdot I_{in(peak\_max)}}{t_{on}}t\right)dt$$

$$\geq \frac{t_{on} \cdot I_{in(peak\_max)}}{2 \cdot \Delta V_{in(max)}} \quad (8)$$

$$\geq \frac{L \cdot I^2_{O(max)} \cdot V^2_O}{\Delta V_{in(max)} \cdot V^3_{in(peak\_min)}}$$

The input capacitor must be larger than the value calculated by (8). And the maximum input capacitance is limited by the input displacement factor (IDF), defined as IDF≡cosθ. As shown in Fig. 14, the input capacitor generates 90° leading current, which causes phase difference between the line current and the line voltage. The phase difference increases as the capacitance of the input capacitor increases. Therefore, the input capacitor must be smaller than $C_{in(max)}$ calculated by (12). $C_{in(max)}$ is the sum of all the capacitors connected at the input side.

$$V_a = V_A = V_{in(peak)}\cos(\omega t) \quad (9)$$

$$i_a = I_a\cos(\omega t)$$

$$i_A = i_a + i_c = I_a\cos(\omega t) - \omega C_{in}V_{in(peak)}\sin(\omega t) \quad (10)$$

$$\theta = \tan^{-1}\left(\frac{\omega C_{in}V_{in(peak)}}{I_a}\right) \quad (11)$$

$$C_{in(max)} = \frac{I_a}{\omega V_{in(peak)}}\tan(\cos^{-1}(IDF))$$

$$= \frac{2V_O I_O}{\omega V^2_{in(peak\_max)}}\tan(\cos^{-1}(IDF)) \quad (12)$$

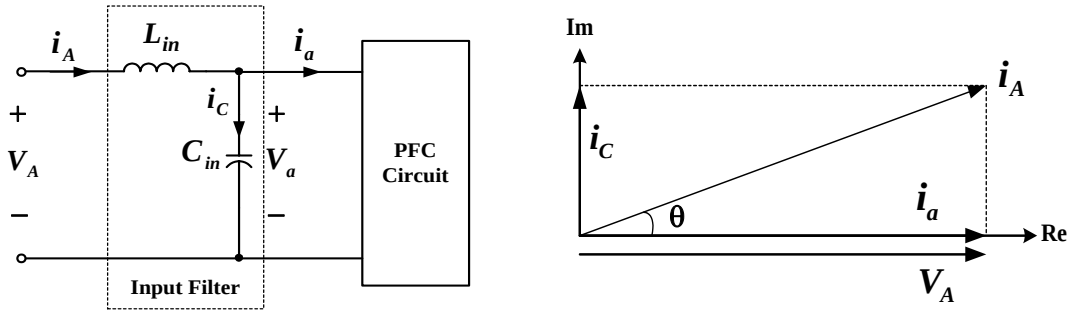

Figure 14. Input Voltage and Current Displacement Due to Input Filter Capacitance

4) Output Capacitor Design

The output capacitor is selected by the relation between the input power and the output power. As shown in Fig. 16, the minimum output capacitance is determined by (14).

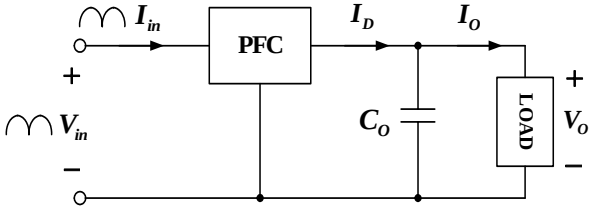

Figure 15. PFC Configuration

$$P_{in} = I_{in(rms)}V_{in(rms)}(1-\cos(2\omega t)) = I_D V_O$$

$$I_D = \frac{I_{in(rms)}V_{in(rms)}}{V_O}(1-\cos(2\omega t)) = I_O(1-\cos(2\omega t)) \quad (13)$$

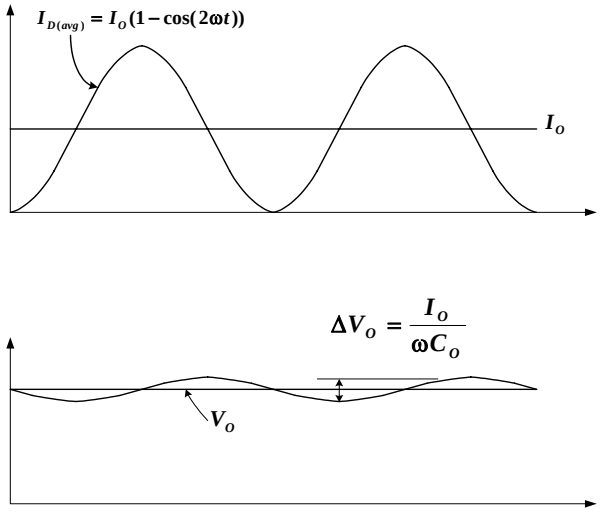

Figure 16. Diode Current and Output Voltage Waveform

$$C_{O(min)} \geq \frac{I_{O(max)}}{2\pi f_{ac} \cdot \Delta V_{O(max)}} \quad (14)$$

5) MOSFET and Diode Selection

The maximum MOSFET RMS current is obtained by (15) and the conduction loss of the MOSFET is calculated by (16). When MOSFET turns on, the MOSFET current rises from zero so the turn-on loss is negligible. The MOSFET turn-off loss and the MOSFET discharge loss are obtained by (17) and (18) respectively. The switching frequency of the critical conduction mode boost PFC converter varies according to the line condition and load condition. Thus, the switching frequency is the average value during a line period. The total MOSFET loss can be calculated by (19) and then a MOSFET can be selected considering the MOSFET thermal characteristic.

$$I_{Qrms} = I_{L(peak\_max)}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in(LL)}}{9\pi V_O}} = \frac{2\sqrt{2}\cdot V_O I_{O(max)}}{\eta V_{in(LL)}}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in(LL)}}{9\pi V_O}} \quad (15)$$

$$P_{on} = I^2_{Qrms} \cdot R_{DSon} \quad (16)$$

$$P_{turn-off} = \frac{1}{6}V_O I_{L(peak\_max)} \cdot t_f \cdot f_{sw} = \frac{\sqrt{2}}{3}\frac{V^2_O \cdot I_{O(max)}}{\eta V_{in(LL)}} \cdot t_f \cdot f_{sw} \quad (17)$$

$$P_{discharge} = \frac{4}{3}C_{oss.Vo} \cdot V^2_O \cdot f_{sw} \quad (18)$$

$$P_{MOSFET} = P_{on} + P_{turn-off} + P_{discharge} \quad (19)$$

The diode average current can be calculated by (20). The total diode loss can be calculated by (21) and then a diode can be selected considering diode thermal characteristic.

$$I_{Davg} = I_{O(max)} \quad (20)$$

$$P_{Diode} = V_f I_{Davg} \quad (21)$$

3.2 Control Circuit Design

1) Output Voltage Sensing Resistor and Feedback Loop Design

The output voltage sensing resistors, R_1 and R_2 are determined by the output voltage at the high line by (22). The output voltage sensing resistors cause power loss, therefore R_1 should be higher than 1MΩ. However, too high resistance can cause some delay of the OVP circuit because of the internal capacitance, Cp. Therefore the OVP level may be increased a little.

$$\frac{R_1}{R_2} = \frac{V_{o\_high} - 2.5}{2.5} \qquad (22)$$

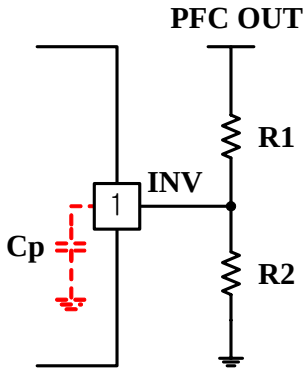

Figure 17. Output Voltage Sensing Circuit

The feedback loop bandwidth must be lower than 20Hz for the PFC application. If the bandwidth is higher than 20Hz, the control loop may try to reduce the 120Hz ripple of the output voltage, and the line current may be distorted decreasing power factor. Therefore a capacitor is connected between COMP and GND to eliminate the 120Hz ripple voltage by 40dB. If a capacitor is connected between the output of the error amplifier and the GND, the error amplifier works as an integrator and the error amplifier compensation capacitor can be calculated by (23). To improve the power factor, C_{comp} must be higher than the calculated value. However, if the value is too high, the output voltage control loop may become slow.

$$C_{comp} = gm \cdot \frac{R_2}{0.01 \cdot 2\pi \cdot 120Hz \cdot (R_1 + R_2)} \qquad (23)$$

To improve the output voltage regulation, a resistor and a capacitor can be added to a simple integrator as shown in Fig. 18. The resistor, R_{comp} increases mid-band gain and the capacitor, C_{filter} which is 1/10~1/5 of the C_{comp}, is used to filter high frequency noise. The gain of the error amplifier with the circuit in Fig. 18 is shown in Fig. 19.

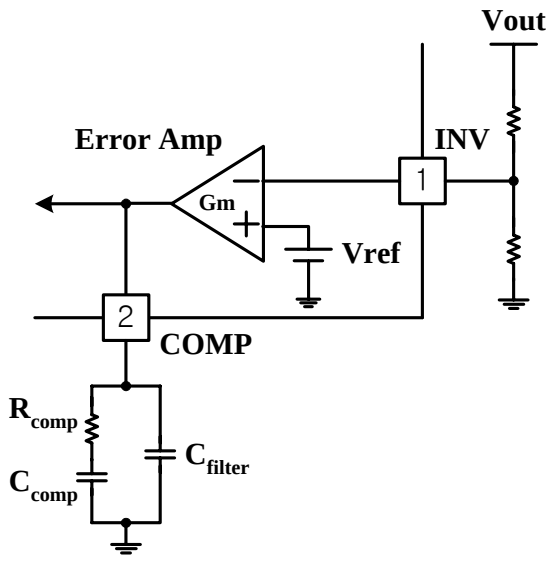

Figure 18. Error Amplifier Circuit

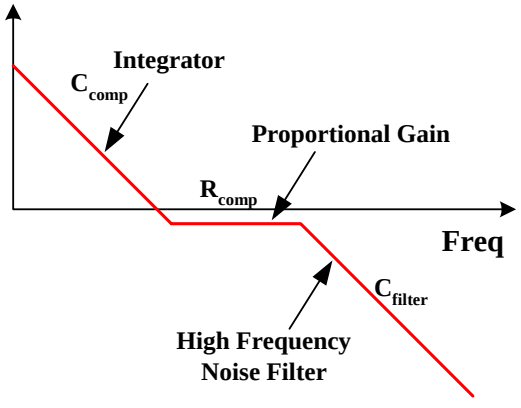

Figure 19. Gain of the Error Amplifier

2) Zero Current Detection Resistor Design

The ZCD current should be less than 10mA, therefore the zero current detection resistor, R_{ZCD} is determined by (24).

$$R_{ZCD} > \left(\frac{N_{aux} \cdot V_o}{N_P} - 6V\right) / (10mA) \qquad (24)$$

Because the ZCD pin has some capacitance, the ZCD resistor and the capacitor cause some delay for ZCD detection as shown in Fig. 20. Because of this delay, the MOSFET is not turned on when the inductor current reaches zero and the MOSFET junction capacitor and the inductor resonate. Then the inductor current changes its direction and flows negatively. The peak value of this negative current is determined by (25). As shown in (25), the negative current increases as the input voltage is close to zero and Coss increases. This negative current decreases average inductor current and causes zero crossing distortion near the zero crossing point

of the AC line as shown in Fig. 21. To minimize the zero crossing distortion, Coss must be minimized and a larger inductor should be used. But there is a limitation in minimizing Coss and using a large inductor, because a small MOSFET increases MOSFET conduction loss and a larger inductor is expensive.

$$I_{NEG} = \sqrt{\frac{C_{oss}}{L}}(V_o - V_{in}) \qquad (25)$$

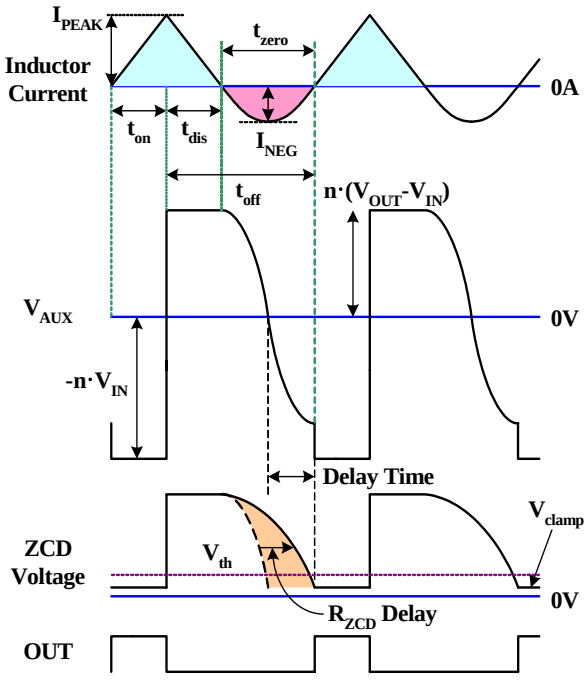

Figure 20. ZCD Waveforms

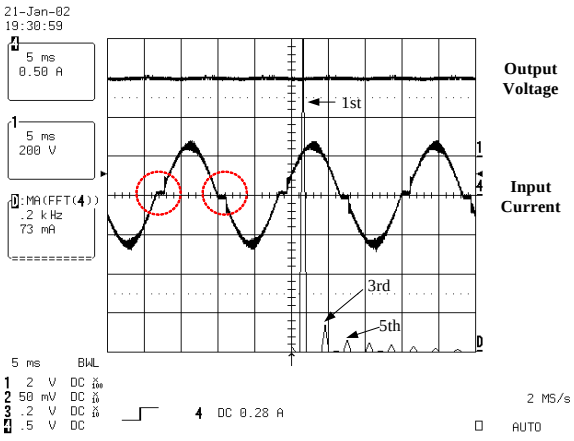

Figure 21. Zero Crossing Distortion

If the R_{ZCD} is selected appropriately, the MOSFET can be turned on when the V_{ds} voltage is minimum to reduce switching loss. But if the R_{ZCD} is designed to minimize the switching loss, the time of the negative current, t_{zero} will increase worsening the zero crossing distortion. To improve the zero crossing distortion, the MOSFET turn-on time should be increased near the AC line zero crossing point. If a resistor is connected between the MOT and the auxiliary winding as shown in Fig. 22, the function can be implemented easily. Because the auxiliary winding voltage is negatively proportional to the input voltage during the MOSFET turn-on time, the current I2 shown in Fig. 22 is proportional to the input voltage. Therefore the slope of the internal ramp changes according to input voltage as the current flowing out of the MOT changes as shown in Fig. 23. I2 current is maximum at the highest line voltage and the zero crossing improvement is best when I2 is 100% ~ 140% of I1.

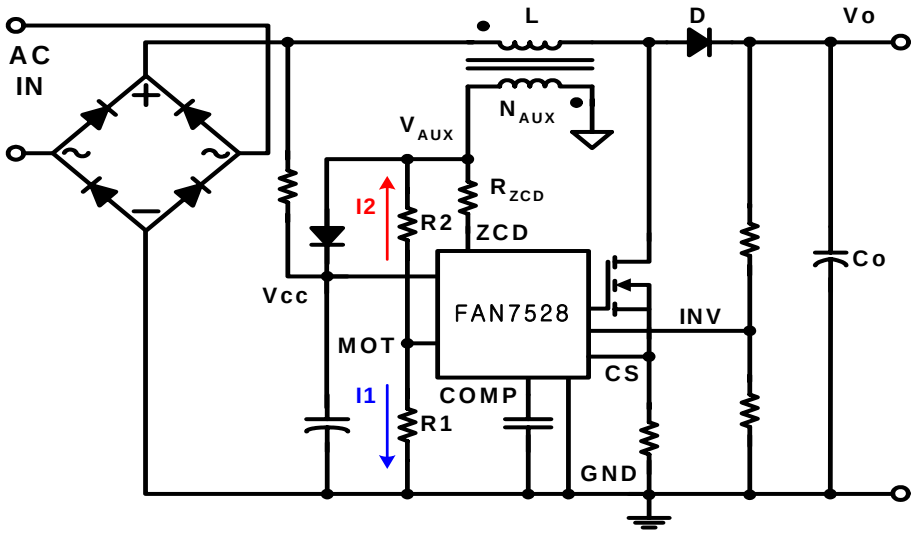

Figure 22. Zero Crossing Improvement Circuit

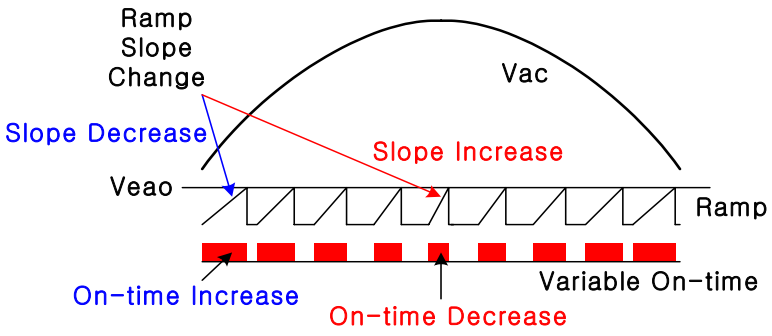

Figure 23. On-time Variation according to Vac

3) Start-up Circuit Design

To start up the FAN7528, the start-up current must be supplied through a start-up resistor. The resistor value is calculated by (26) and (27). The start-up capacitor must supply IC operating current before the auxiliary winding supplies IC operating current maintaining Vcc voltage higher than the UVLO voltage. Therefore the start up capacitor is determined by (28).

$$R_{ST} \le \frac{V_{in(peak\_min)} - V_{th(st)max}}{I_{STmax}} \quad (26)$$

$$P_{Rst} = \frac{V_{in(rms\_max)}^2}{R_{ST}} \le 1W \quad (27)$$

$$C_{ST} \ge \frac{I_{dcc}}{2\pi \cdot f_{ac} \cdot HY_{(ST)min}} \quad (28)$$

4) Current Sense Resistor Design

The CS pin voltage is highest when the AC line voltage is lowest and the output power is maximum. The current sense resistor is determined by (29) and (31) limiting the power loss of the resistor under 1W.

$$R_{sense} < \frac{0.8V}{I_{L(peak\_max)}} = 0.8V \frac{\eta V_{in(peak\_min)}}{4 V_o I_{o(max)}} \quad (29)$$

$$P_{Rsense} = 2\left(\frac{V_o I_{o(max)}}{\eta V_{in(peak\_min)}}\right)^2 \cdot R_{sense} < 1W \quad (30)$$

$$R_{sense} < \frac{1W}{2}\left(\frac{\eta V_{in(peak\_min)}}{V_o I_{o(max)}}\right)^2 \quad (31)$$

4. Design Example

A 100W converter is designed to illustrate the design procedure using a design excel file. If you enter the system parameters in the excel file, you can get the designed parameters. The system parameters are as follows:

- Maximum output power : 100W
- Input voltage range : 90Vrms~264Vrms
- Output voltage : 389V
- AC line frequency : 60Hz
- PFC efficiency : 90%
- Minimum switching frequency : 39kHz
- Input displacement factor (IDF) : 0.98
- Input capacitor ripple voltage : 24V
- Output voltage ripple : 8V

4.1 Inductor design

The boost inductor is determined by (6). Calculate it at both the lowest voltage and the highest voltage of the low line and choose the lower value. The calculated value is 402uH. To get the calculated inductor value, EI30 core is used and the primary winding is 44 turns. The air gap is 0.6mm at both legs of the EI core. The auxiliary winding is determined by (7), which is 6 turns.

4.2 Input Capacitor Design

The minimum input capacitance is determined by the input voltage ripple specification. The calculated minimum input capacitor value is 0.33uF. The maximum input capacitance is restricted by the IDF. The calculated value is 0.77uF. The selected value is 0.63uF (sum of all the capacitors connected to the input side, C1, C2, C3, C4, and C5).

4.3 Output Capacitor Design

The minimum output capacitor is determined by (14) and the calculated value is 85uF. The selected value for the capacitor is 100uF.

4.4 MOSFET and Diode Selection

By (15) ~ (19), 500V/13A MOSFET FQPF13N50C is selected, and 600V/1A diode BYV26C is selected by (20) ~ (21).

4.5 Output Voltage Sense Resistor and Feedback Loop Design

The upper output voltage sense resistor is chosen to be 2MΩ and the bottom output voltage sense resistor is 12.9kΩ.
The error amp compensation capacitance must be larger than 0.1uF by (23). Therefore, 1uF capacitor is used.

4.6 Zero Current Detection Resistor Design

The calculated value is 3.8kΩ and the selected value is 20 kΩ. A 47pF ceramic capacitor is connected between the ZCD pin and the ground to increase the delay time for the MOSFET minimum voltage turn-on.

4.7 Start-up Circuit Design

The maximum start-up resistor is 1.63MΩ, and the minimum is 140kΩ as determined by (26) ~ (27). Our selection is 330kΩ. And the Vcc capacitance must be larger than 7uF by (28). The selected value is 47uF.

4.8 Current Sense Resistor Design

The maximum current sense resistance is 0.23Ω by (31) and the selected value is 0.22Ω.

4.9 MOT Resistor Design

The MOT resistor is determined to get the maximum on-time when the AC line voltage is lowest and the output power is maximum. The calculated value is 6.7kΩ and the maximum on-time is 11.04us. To improve THD performance, a 10kΩ resistor is used for the MOT resistor and a 370kΩ resistor is connected between the MOT pin and the auxiliary winding.
The maximum on-time (MOT) is determined by (32) and the MOT resistor is determined by (33).

$$MOT = \frac{2 \cdot L \cdot P_O}{\eta \cdot V_{in(rms\_min)}^2} \qquad (32)$$

$$R_{MOT} > \frac{MOT}{1654} \times 10^6 \qquad (33)$$

Fig. 24 shows the designed application circuit diagram and Table 2 shows the 100W demo board components list.

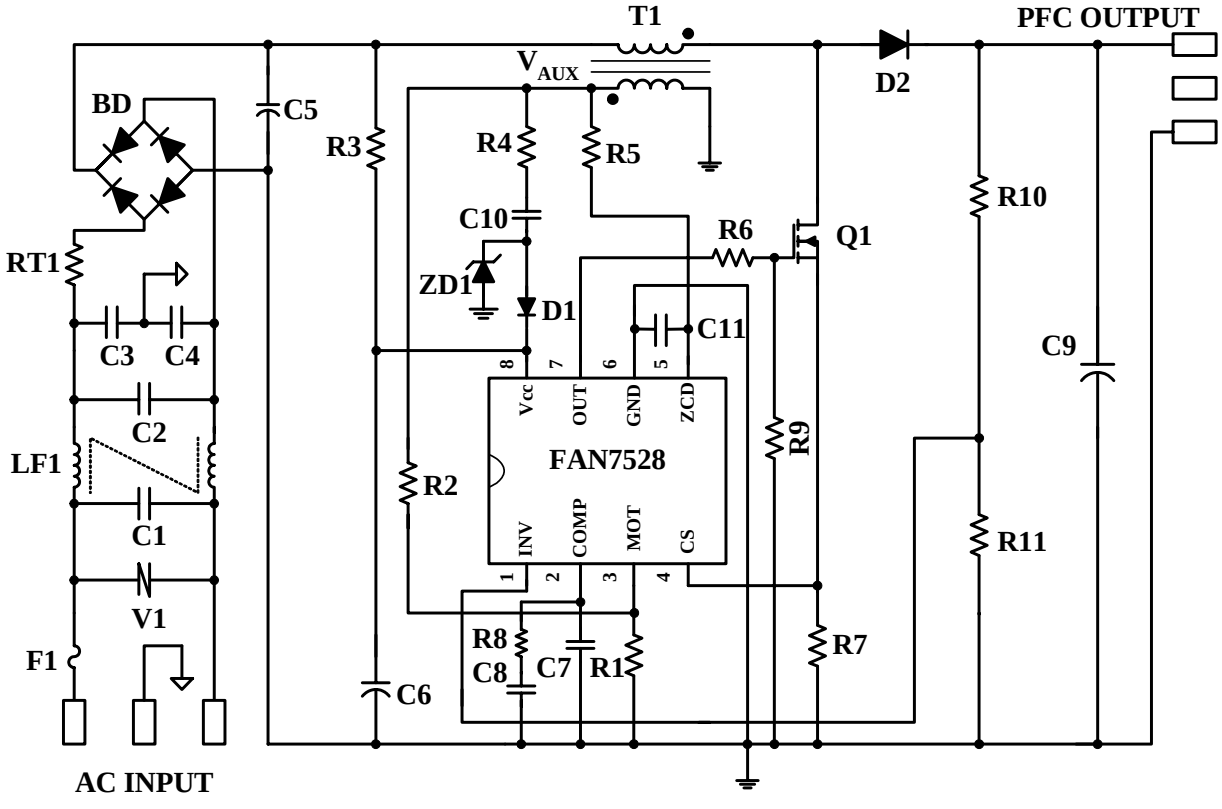

Figure 24. Application Circuit Schematic

Table 2. 100W Demo Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	250V/3A		C1	150nF/275Vac	Box Capacitor
TNR			C2	330nF/275Vac	Box Capacitor
V1	471	470V	C3,C4	2.2nF/3kV	Ceramic Capacitor
NTC			C5	150nF/630V	Film Capacitor
RT1	10D-9		C6	47uF/25V	Electrolytic Capacitor
Resistor			C7	47nF/50V	Ceramic Capacitor
R1	10kΩ	1/4W	C8	220nF	MLCC
R2	370kΩ	1/4W	C9	100uF/450V	Electrolytic Capacitor
R3	330kΩ	1/2W	C10	12nF/100V	Film Capacitor
R4	150Ω	1/2W	C11	47pF/50V	Ceramic Capacitor
R5	20kΩ	1/4W	Diode		
R6	10Ω	1/4W	BD	KBL06	600V/4A
R7	0.22Ω	1/2W	D1	1N4148	Fairchild
R8	10kΩ	1/4W	D2	BYV26C	600V/1A
R9	10kΩ	1/4W	D3	1N5819	Fairchild
R10	2MΩ	1/4W	D4	1N5819	Fairchild
R11	12.9kΩ	1/4W	ZD1	1N4746	18V
IC			Inductor		
IC1	FAN7528		T1	400uH(44T:6T)	EI3026
Line Filter			MOSFET		
LF1	32mH	Wire 0.45mm	Q1	FQPF13N50C	500V/13A

Table 3. Performance Data

		90Vac	110Vac	220Vac	264Vac
100W	PF	0.999	0.998	0.991	0.983
	THD	3.5%	3.7%	6.1%	7.3%
	Efficiency	92.7%	94.1%	94.7%	95.5%
50W	PF	0.997	0.996	0.971	0.947
	THD	5.1%	5.5%	11.1%	13%
	Efficiency	95%	94.2%	91.9%	92.9%

Nomenclature

$I_{L(peak)}$ (t): inductor current peak value during one switching cycle

$I_{L(peak)}$: inductor current peak value during one AC line cycle

$I_{L(peak\_max)}$: maximum inductor current peak value

I_L (t): inductor current

I_D: boost diode current

I_{in} (t): input current

$I_{in\ (peak)}$: input current peak value

$I_{in\ (peak\_max)}$: maximum of the input current peak value

$I_{in\ (rms)}$: input current RMS value

I_{Qrms}: MOSFET RMS current

I_{Drms}: diode RMS current

I_{Davg}: diode average current

I_O: output current

$I_{O\ (max)}$: maximum output current

V_{in} (t): input voltage

$\Delta V_{in\ (max)}$: maximum input voltage ripple

$V_{in\ (peak)}$: input voltage peak value

$V_{in\ (peak\_low)}$: input voltage peak value at low line

$V_{in\ (peak\_max)}$: maximum input voltage peak value

$V_{in\ (peak\_min)}$: minimum input voltage peak value

$V_{in\ (rms)}$: input voltage RMS value

$V_{in\ (rms\_max)}$: maximum input voltage RMS value

$V_{in\ (rms\_min)}$: minimum input voltage RMS value

$V_{in\ (LL)}$: low line RMS input voltage

$V_{in\ (HL)}$: high line RMS input voltage

V_O: output voltage

V_{O_low}: output voltage at low line

V_{O_high}: output voltage at high line

$\Delta V_{O\ (max)}$: maximum output voltage ripple

P_O: output power

$P_{O(max)}$: maximum output power

P_{in}: input power

η: converter efficiency

t_{on}: switch on time

t_{off}: switch off time

t_f: MOSFET current falling time

T_S: switching period

f_{ac}: AC line frequency

ω: AC line angular frequency

f_{sw}: switching frequency

$f_{sw(max)}$: maximum switching frequency

$f_{sw(min)}$: minimum switching frequency

L: boost inductance

C_O: output capacitance

C_{in}: input capacitance

N_{aux}: auxiliary winding turn number

N_P: boost inductor turn number

C_{comp}: compensation capacitance

R_{zcd}: zero current detection resistance

R_{ST}: start-up resistance

R_{sense}: current sense resistance

I_{STmax}: maximum start-up supply current

C_{ST}: start-up capacitance

$HY_{(ST)min}$: minimum UVLO hysteresis