AN-8025

Design Guideline of Single-Stage Flyback AC-DC Converter Using FAN7530 for LED Lighting

Summary

This application note describes the single-stage power factor correction (PFC) and presents the design guidelines of a 75W universal-input, single-stage PFC for LED lighting applications. Flyback converter topology controlled by the critical conduction mode control IC, FAN7530 is applied and several functions; such as CV/CC mode feedback circuits, cycle-by-cycle current limit, soft-starting function, and so on, are considered for LED lighting applications.

Introduction

Despite large output voltage ripple, single-stage AC-DC conversion is a more attractive solution than two-stage conversion from the standpoint of the cost and power density. Especially in applications like battery chargers, Plasma Display Panel (PDP)-sustaining power supplies, and LED lighting; low frequency, 100Hz or 120Hz, large output voltage ripple is inconsequential.

Single-stage AC-DC converter directly converts AC input voltage to the DC output voltage without a pre-regulator, as shown in Figure 1.

This application note presents a 75W single-stage AC-DC converter for LED lighting. As a power-conversion topology, flyback converter is normally chosen because it doesn't need an inductive output filter; the main transformer works as an inductive filter itself.

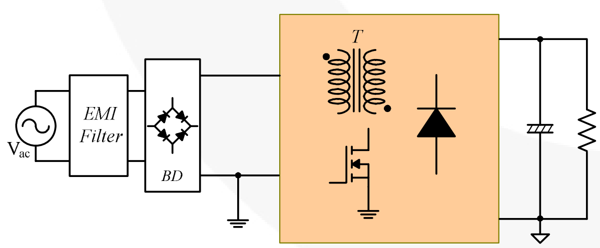


Figure 1. Single-Stage AC-DC Converter

Figure 2 shows the circuit diagram of a flyback AC-DC converter. FAN7530 is used as a controller and both CV (constant voltage) and CC (constant current) mode feedback circuits are applied to prevent overload and over-voltage conditions. In LED lighting, the output is always full-load condition and the forward voltage drop of LED decreases if the junction temperature of LED increases. Therefore the output should be controlled by CC mode in the normal state while CV mode only works as over voltage protection.

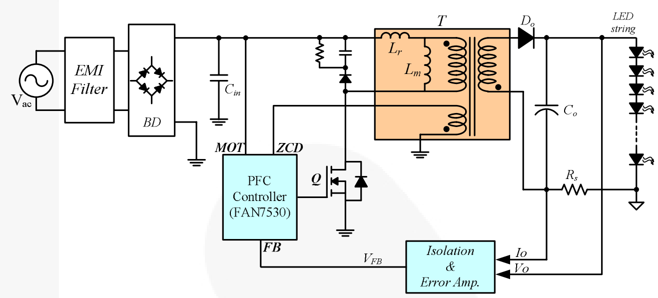


Figure 2. Flyback AC-DC Converter

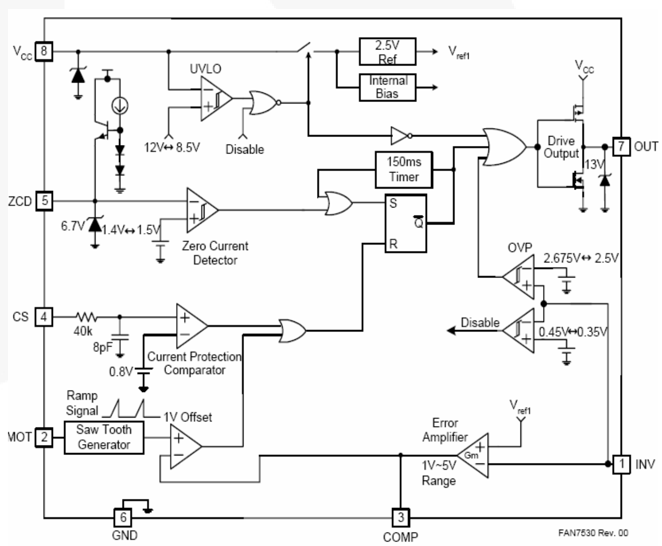


Figure 3. Block Diagram of FAN7530

Figure 3 shows the block diagram of FAN7530. Its major features are:

- Fixed On Time CRM PFC Controller
- Zero Current Detector (ZCS) & Valley Switching
- MOSFET Over-Current Protection
- Low Startup (40µA) and Operating Current (1.5mA)
- Totem Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current

FAN7530 is a voltage-mode CRM PFC controller; the turn-on time of switch is fixed while the turn-off time is varied during the steady state. Therefore, the switching frequency varies in accordance with the input voltage variation shown in Figure 4.

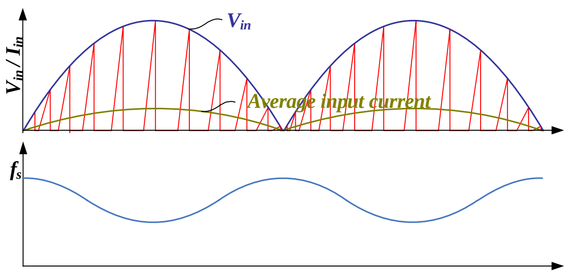


Figure 4. Switching Frequency Variation

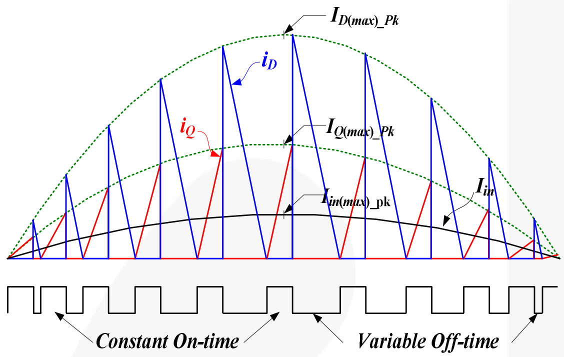


Figure 5. Theoretical Waveforms

Figure 5 illustrates the theoretical waveforms of the primary-side switch current, the secondary-side diode current, and gating signal. MOSFET Q turns on and Fast Recovery Diode (FRD) D_o turns off under zero-current condition, while Q turns off and D_o turns on under the hard-switching condition.

Design Example

A design guideline of 75W single-stage flyback AC-DC converter using FAN7530 is presented. The applied system parameters are shown in Table 1.

Table 1. System Parameters

Parameter	Value
Output Power	75W
Input Voltage Range	85~265V_{AC}
Output Voltage	45V
Output Limit Voltage	50V
Duty Ratio at $I_{in(max)\_pk}$, $D_{@\ Iin(max)\_pk}$	0.6
Minimum Switching Frequency, f_{s_min}@ V_{in_min}	50kHz
Efficiency, η	85%

1. Flyback Transformer Design

In flyback converter, the transformer is easily saturated because the transformer is only utilized in the first quadrant of B-H loop. Moreover, if it works under the critical conduction mode, the peak current is much higher than that of the continuous conduction mode. Therefore, air-gap should be inserted to prevent saturation of the transformer.

A proper turn ratio, N_1/N_2, should also be considered in a flyback single-stage AC-DC converter because the maximum voltage rating of the MOSFET and Fast Recover Diode (FRD) strongly relates to the turn ratio of transformer. There is a trade-off relationship between the drain-to-source voltage rating, V_{dss}, of MOSFET and the reverse voltage rating, V_R, of the FRD in accordance with the turn ratio of the transformer. A larger turn ratio (N_1/N_2) requires a higher V_R of FRD while V_{dss}, of MOSFET is decreased. In contrast, a lower turn ratio causes a higher voltage stress on the MOSFET, while V_R of the FRD is decreased. Figure 6 shows the trade-off relationship between V_{dss} of the MOSFET and V_R of the FRD.

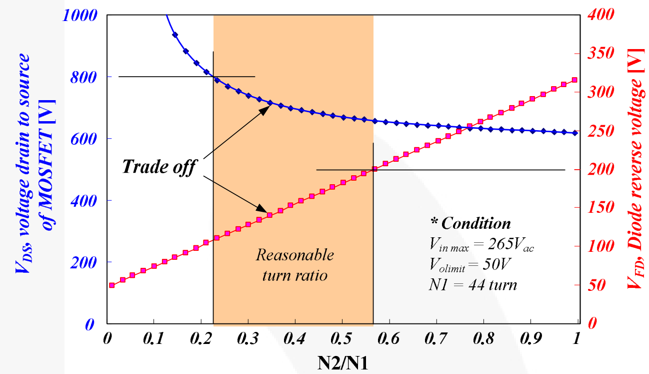


Figure 6. Trade-Off Between V_{DS} and V_R

From $P_o=\eta V_{in} I_{in}$, the maximum line current $I_{in(\max)}$ = $P_o/\eta V_{in(\min)}$. If switching frequency f_s is much higher than the AC line frequency, f_{ac}, the input current can be assumed to be constant during one switching period.

To define the magnetizing inductance of transformer, the largest period must be defined. The largest switching period occurs at the peak of input current, $I_{in(max)\_pk}$, when the minimum input voltage is applied. It can be defined as:

$$I_{in(\max)\_pk} = \frac{1}{T}\int_0^{DT} \frac{I_{Q(\max)\_pk}}{DT} t\, dt = \frac{DI_{Q(\max)\_pk}}{2} \tag{1}$$

$$I_{Q(\max)\_pk} = \frac{2}{D} I_{in(\max)\_pk} \tag{2}$$

where $D = D_{@\ Iin(\max)\_pk}$, $I_{in(\max)\_pk} = \sqrt{2} I_{in(\max)}$, and $V_{in(\min)\_pk} = \sqrt{2} V_{in(\min)}$, respectively.

The transformer primary-side voltage, V_T, is defined as:

$$V_T = L_m \frac{\Delta I}{\Delta T} = L_m \frac{I_{Q(\max)\_pk} f_{s(\min)}}{D_{@\ \mathrm{Iin(max)\_pk}}} \tag{3}$$

Therefore, the magnetizing inductance is calculated by:

$$L_m \geq \frac{D_{@ I_{in(\max)\_pk}}{}^2 \cdot V_{in(\min)}}{2 I_{in(\max)} f_{s(\min)}} = \frac{0.6^2 \times 85}{2 \times 1.04 \times 50 \times 10^{-3}} \tag{4}$$
$$= 294.8uH$$

From Equation (4) and Table 1, the calculated magnetizing inductance is 294µH.

There are several methods defining the turn number for the desirable inductance, but using the AL-value is the most

common and the easiest. The turn number can be obtained with AL-value as:

$$N = \sqrt{\frac{L}{AL - value}} \tag{5}$$

However, if air-gap is inserted into the magnetic core, a designer should find the AL-value. To obtain AL-value, wind several turns into a bobbin and measure the inductance, then calculate AL-value with the equation:

$$AL - value = \frac{L}{N^2} \tag{6}$$

Once the AL-value is obtained, calculate the turn number using Equation (6).

Applying coil dummy EER3435 with 0.33mm of air gap for the transformer and 14.9µH is measured when 10 turns are winded into the core and 0.149×10^{-6} of AL-value is obtained. Therefore, the calculated primary-side turn number is 44.5 from Equation (6) and finally determines 44 as the primary-side turn number. (The actual inductance is measured as 330µH.)

The secondary-side turn number is obtained as 17 turns by following equation:

$$N_2 = \frac{\pi N_1 V_o (1 - D_{max})}{2\sqrt{2} D_{max} V_{in(min)}} = \frac{\pi \times 44 \times 45 (1 - 0.6)}{2\sqrt{2} \times 0.6 \times 85} = 17 \tag{7}$$

2. MOSFET and FRD

The voltage stress of MOSFET is calculated as:

$$\begin{aligned} V_{ds(max)} &= V_{in(max)\_pk} + V_{sn(max)} \\ &= V_{in(max)\_pk} + V_f + V_{Lk} \end{aligned} \tag{8}$$

where V_{sn} is the maximum capacitor voltage of the snubber circuit; V_f is the flyback voltage; and V_{Lk} is the ringing voltage at the leakage inductance of the transformer. V_f is derived by N_1V_o/N_2 and V_{Lk} is normally estimated as 1.5 times the flyback voltage, V_f. Therefore, the maximum voltage of MOSFET is obtained as:

$$\begin{aligned} V_{ds(max)} &= \sqrt{2} V_{in(max)} + 2.5 n V_o = \sqrt{2} \times 265 \times 2.5 + \frac{44}{17} \times 45 \\ &= 665.94V \end{aligned} \tag{9}$$

The maximum rms current and the peak current are:

$$I_{in(max)} = \frac{P_o}{\eta V_{in(min)}} = \frac{75}{0.85 \times 85} = 1.04A \tag{10}$$

and

$$I_{Q(max)\_pk} = \frac{2\sqrt{2} P_o}{\eta D_{@\ Iin(max)\_pk} V_{in(min)}} = \frac{2\sqrt{2} \times 75}{0.85 \times 0.6 \times 85} = 4.89A \tag{11}$$

respectively.

Therefore, an N-Channel enhancement-mode MOSFET, FQPF8N80C (800V, 8A, R_{DS_ON} = 1.55Ω), is chosen in consideration of the margins.

The maximum reverse voltage and the forward peak current of the FRD are:

$$\begin{aligned} V_{R(max)} &= V_{o\_Limit} + \frac{N_2}{N_1} V_{in(max)\_pk} \\ &= 50 + \frac{17}{44} \times \sqrt{2} \times 265 = 195V \end{aligned} \tag{12}$$

$$I_{R\_pk} = \frac{2}{(1 - D_{@\ Iin(max)\_pk})} I_o = \frac{2}{(1 - 0.6)} \times \frac{75}{45} = 8.33A \tag{13}$$

respectively. Therefore, the Ultra-Fast Rectifier Diode (UFRD), F06UP20S (200V, 6A, V_F=1.15V), is finally chosen in consideration of the margins.

3. Snubber Circuit Design

In flyback converter, the resonant between L_{leak} and C_{oss} causes an excessively high voltage surge that causes damage to the MOSFET during turn-off. This voltage surge must be suppressed and a snubber circuit is therefore necessary to prevent MOSFET failures.

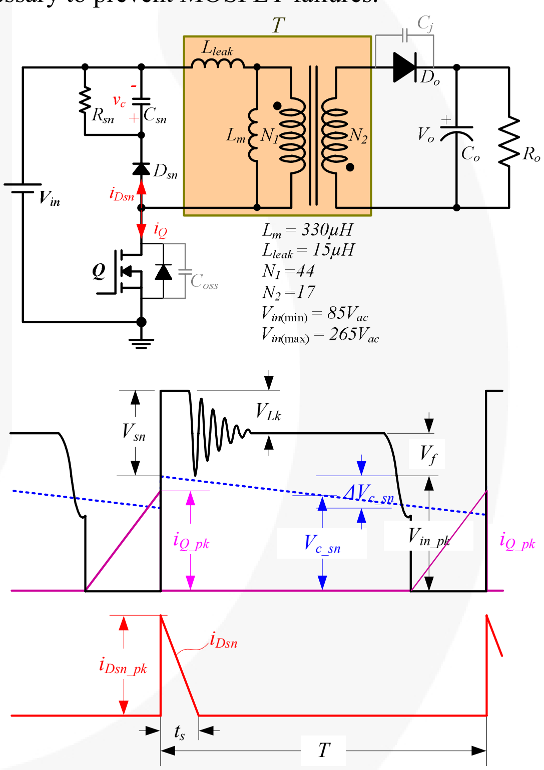


Figure 7. Snubber Circuit

The clamping voltage by snubber is:

$$V_{sn} = V_f + L_{leak} \frac{\Delta i}{\Delta t} = V_f + L_{leak} \frac{I_{Dsn\_pk}}{t_s} \tag{14}$$

Therefore:

$$t_s = \frac{L_{leak} \cdot I_{Dsn\_pk}}{V_{sn} - V_f} \tag{15}$$

The maximum power dissipation of the snubber circuit is determined by:

$$P_{sn} = \frac{1}{T} \int_0^{t_s} V_{sn} \cdot \frac{I_{Dsn\_pk}}{t_s} t\, dt = \frac{1}{2} L_{leak} I_{Dsn\_pk}{}^2 \frac{V_{sn}}{V_{sn} - V_f} f_s \tag{16}$$

The maximum power dissipation is:

$$P_{sn(\max)} = \frac{1}{2} L_{leak} I_{Dsn\_pk}{}^2 \frac{V_{sn}}{V_{sn} - V_f} f_{s@v_{in\_max}} = \frac{V_{sn}{}^2}{R_{sn}} \quad (17)$$

where $V_{sn}=V_f+V_{Lr}$

Therefore, the resistance, R_{sn}, is determined by:

$$R_{sn} = \frac{V_{sn}{}^2}{\frac{1}{2} L_{leak} I_{Dsn\_pk}{}^2 \frac{V_{sn}}{V_{sn} - V_f} f_{s@v_{in\_max}}} \quad (18)$$

The maximum ripple voltage of the snubber circuit is obtained by:

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_{s@v_{in\_max}}} \quad (19)$$

The larger snubber capacitor results, the lower voltage ripple, but the power dissipation increases. Consequently, selecting the proper value is important. In general, it is reasonable to determine that the surge voltage of snubber circuit, V_{sn}, is two to three (2~3) times the flyback voltage, V_f, and the ripple voltage, Δv_c, is 50V. In this application note, the snubber voltage is 2.5 times of the flyback voltage. Thus, the snubber resistor and capacitor are determined by the following equations:

$$\begin{aligned} I_{Dsn\_pk@V_{in}=265V} &= \frac{2\sqrt{2}P_o}{\eta D_{\min} V_{in}} \\ &= \frac{2\sqrt{2}\times 75}{0.85\times 0.33\times 265} = 2.85A \end{aligned} \quad (20)$$

$$V_{sn} = V_f + V_{Lk} = 2.5V_f = 2.5\times\frac{44}{17}\times 45 = 291.17V \quad (21)$$

$$t_s = \frac{L_{leak}\cdot I_{Dsn\_pk}}{V_{sn} - V_f} = \frac{15\times 10^{-6}\times 2.85}{291.17 - \frac{44}{17}\times 45} = 245.03n\sec \quad (22)$$

$$\begin{aligned} f_{s@v_{in\_max}} &= \frac{D_{\min} V_{sn}}{L_{m(measured)} I_{Dsn\_pk@V_{in}=265V}} \\ &= \frac{0.33\times 291.17}{330\times 10^{-6}\times 2.85} = 102.03kHz \end{aligned} \quad (23)$$

$$\begin{aligned} R_{sn} &= \frac{291.17^2}{\frac{1}{2}\times 15\mu\times 2.85^2\times\frac{291.17}{291.17-(44/17)45}\times 102.03k} \\ &= 8.16k\Omega \end{aligned} \quad (24)$$

$$\begin{aligned} C_{sn} &= \frac{V_{sn}}{\Delta V_{sn} R_{sn} f_{s@v_{in\_max}}} \\ &= \frac{291.17}{50\times 8.16k\times 102.03k} = 6.99nF \end{aligned} \quad (25)$$

where the minimum duty ratio is obtained as:

$$\begin{aligned} D_{\min} &= \frac{V_o}{\frac{N_2}{N_1} V_{iavg(\max)} + V_o} \\ &= \frac{45}{\frac{17}{44}\times\left(\frac{2\sqrt{2}}{\pi}\times 265\right) + 45} = 0.33 \end{aligned} \quad (26)$$

Even though the calculated R_{sn} is 8.16kΩ, the actual resistance value should be increased because large power dissipation in the snubber circuit is expected due to small resistance. In practice, it is reasonable to choose the resistance about two times of the calculated value.

4. Sensing Resistor

The CS pin of FAN7530 limits the peak current and protects the MOSFET during transient state or over load condition. Normally, it is reasonable to limit to 1.5 times the switching peak current. The limiting level of switching peak current and the sensing resistor are obtained as:

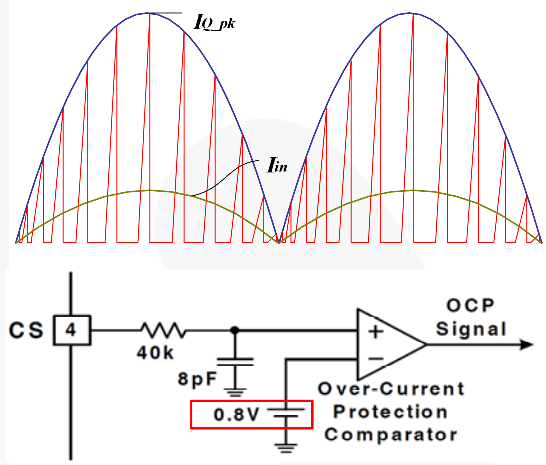


Figure 8. Switching Current Limit

$$\begin{aligned} I_{Q\_Limit} &= 1.5 I_{Q(\max)\_pk} = 1.5\times\frac{2}{D_{\max}}\left(\sqrt{2}\frac{P_o}{\eta V_{in(\min)}}\right) \\ &= 1.5\times\frac{2}{0.6}\left(\sqrt{2}\frac{75}{0.85\times 85}\right) = 7.4A \end{aligned} \quad (27)$$

$$R_s \le \frac{0.8}{I_{Q\_Limit}} = \frac{0.8}{7.4} = 0.11\Omega \quad (28)$$

5. Soft-starting Circuit

Since the FAN7530 is designed for a non-isolated boost PFC circuit, some circuits are added externally. The internal disable amplifier can be used as soft-start function when FAN7530 is applied to non-isolated PFC circuit. However, the disable amplifier cannot participate in the operation if it is applied to isolated single stage PFC circuit because the initial voltage at Pin 1 is zero and FAN7530 cannot start. To exclude the disable amplifier from operation, over 0.5V of voltage must be applied through a blocking diode, as shown in Figure 9(a).

The initial V_{FB} is approximately defined as:

$$V_{FB\_initial} = \frac{R_1 R_{FB}}{R_{FB}(R_1+R_2)+R_1R_2}\cdot VCC \quad (29)$$

To prevent MOSFET failure due to the initial excessive switching current, an external soft-start function is necessary. The circuit shown in Figure 9(b) makes the output voltage of E/A increase slowly and, consequently,

the converter can be smoothly started in accordance with the gradual increase of the on time.

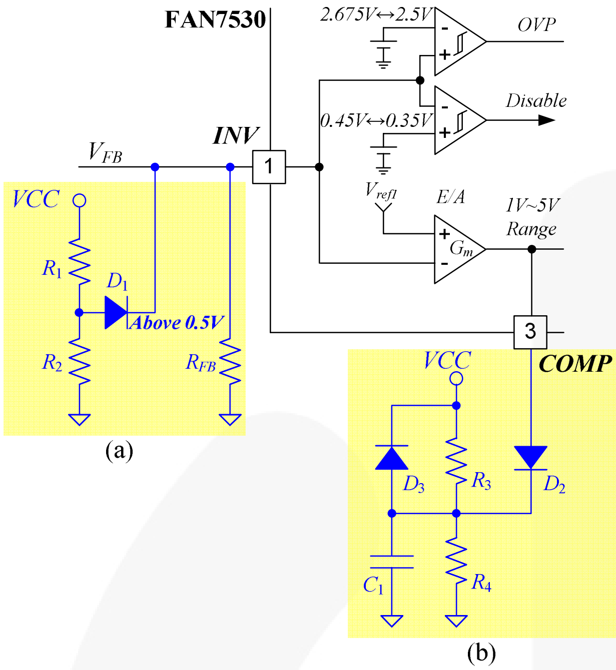


Figure 9. Soft-Starting Circuit

6. Voltage and Current Feedback

Power supplies for LED lighting must be controlled by constant current (CC) mode as well as a constant voltage (CV) mode. Because the forward voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged.

Figure 10 shows an example of a CC and CV mode feedback circuit. During normal operation, CC mode is dominant and CV mode only acts as OVP for abnormal modes.

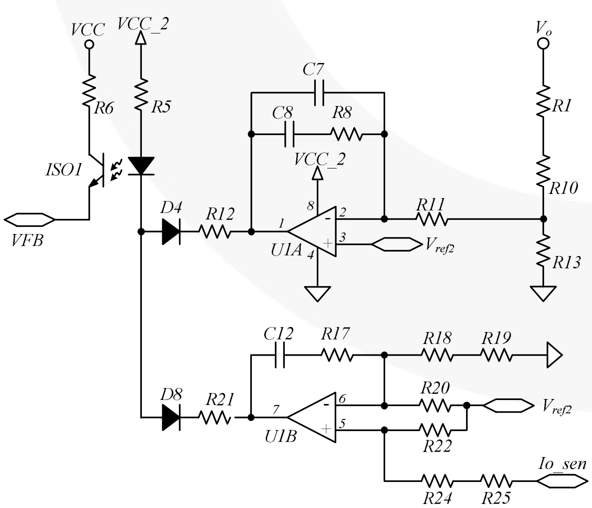


Figure 10. Example of CC & CV Feedback Circuit

Experimental Results

To verify the validity of the design guideline in this application note, a prototype test set-up was built and tested. The design parameter and component values are shown in the appendix.

Figure 11shows the input voltage and current at $110V_{AC}$ input and $220V_{AC}$ input conditions. The power factors at $110V_{AC}$ and $220V_{AC}$ condition are measured as 0.997 and 0.955, respectively.

Figure 12 shows the waveforms of the switching voltage and current, which shows the switching current waveforms following the shape of the input voltage well. The switch is turned on at zero current condition.

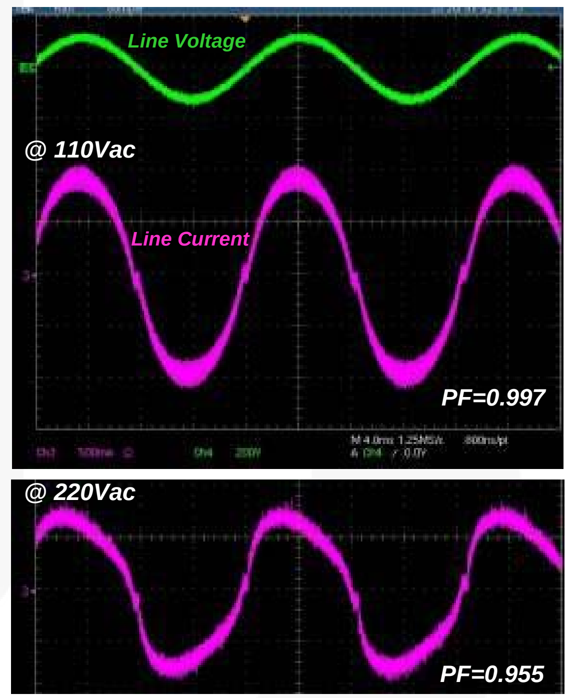
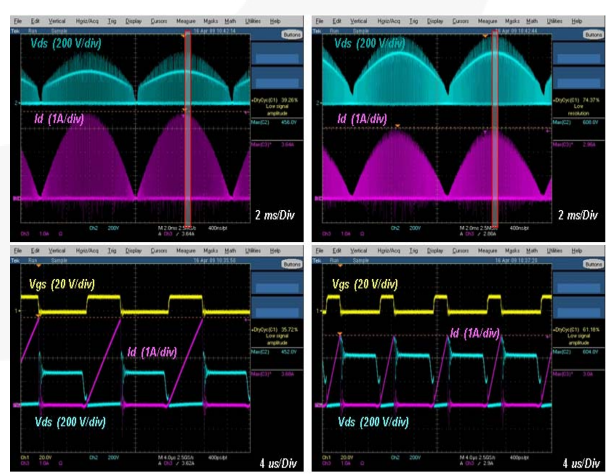


Figure 11. Input Voltage and Current



(a) at 110 V_{ac} Input **(b) at 220 V_{ac} Input**

Figure 12. Switching Voltage and Current

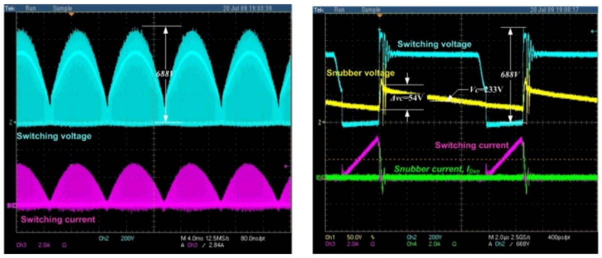


Figure 13. Drain-Source Voltage and Switching Current at 265V$_{AC}$ Input Condition

Figure 13 shows the waveforms of the drain-source voltage and current of 265V of input line voltage, the maximum input voltage, is applied. The voltage ripple of snubber circuit is measured at 54V and the maximum voltage stress is 688V. Since the maximum voltage is 688V, 800V rating MOSFET is needed for wide input voltage range.

The efficiency characteristics according to the load variation for 110 V_{ac} and 220 V_{ac} of the input conditions are plotted in Figure 14. In the case of 110V_{ac} input, the maximum efficiency is measured as 85.17% at 45W load condition.

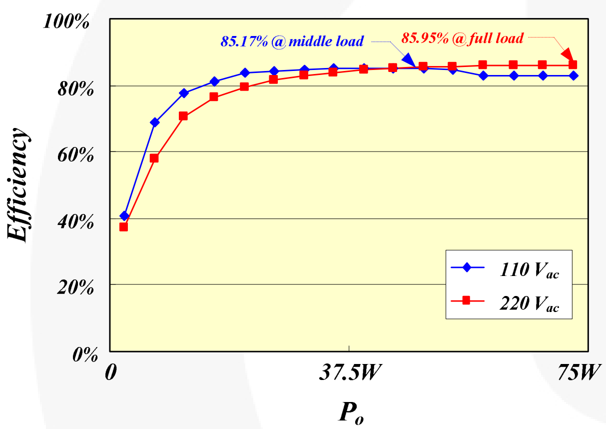


Figure 14. Efficiency Comparison

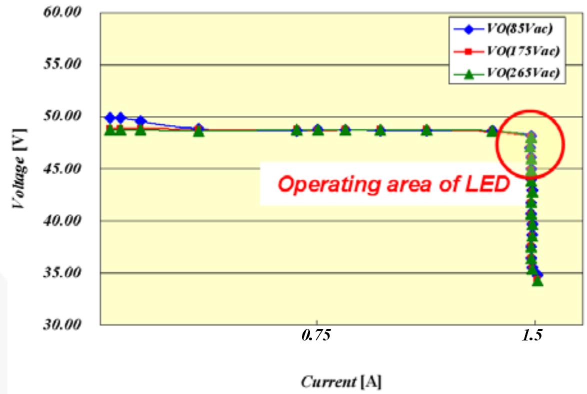


Figure 15. Output V-I Characteristic

In the case of 220V_{ac} input, the maximum efficiency is measured as 85.95% at full-load condition 75W.

In LED lighting, LED strings are driven by the rating current and the power supply should be operated under the full-load condition. Therefore, the power supply is controlled by constant current during normal condition. Figure 15 shows the V-I characteristics of the prototype experimental set-up. The result verifies that the output is driven well by the constant current control for whole input voltage condition.

Schematic

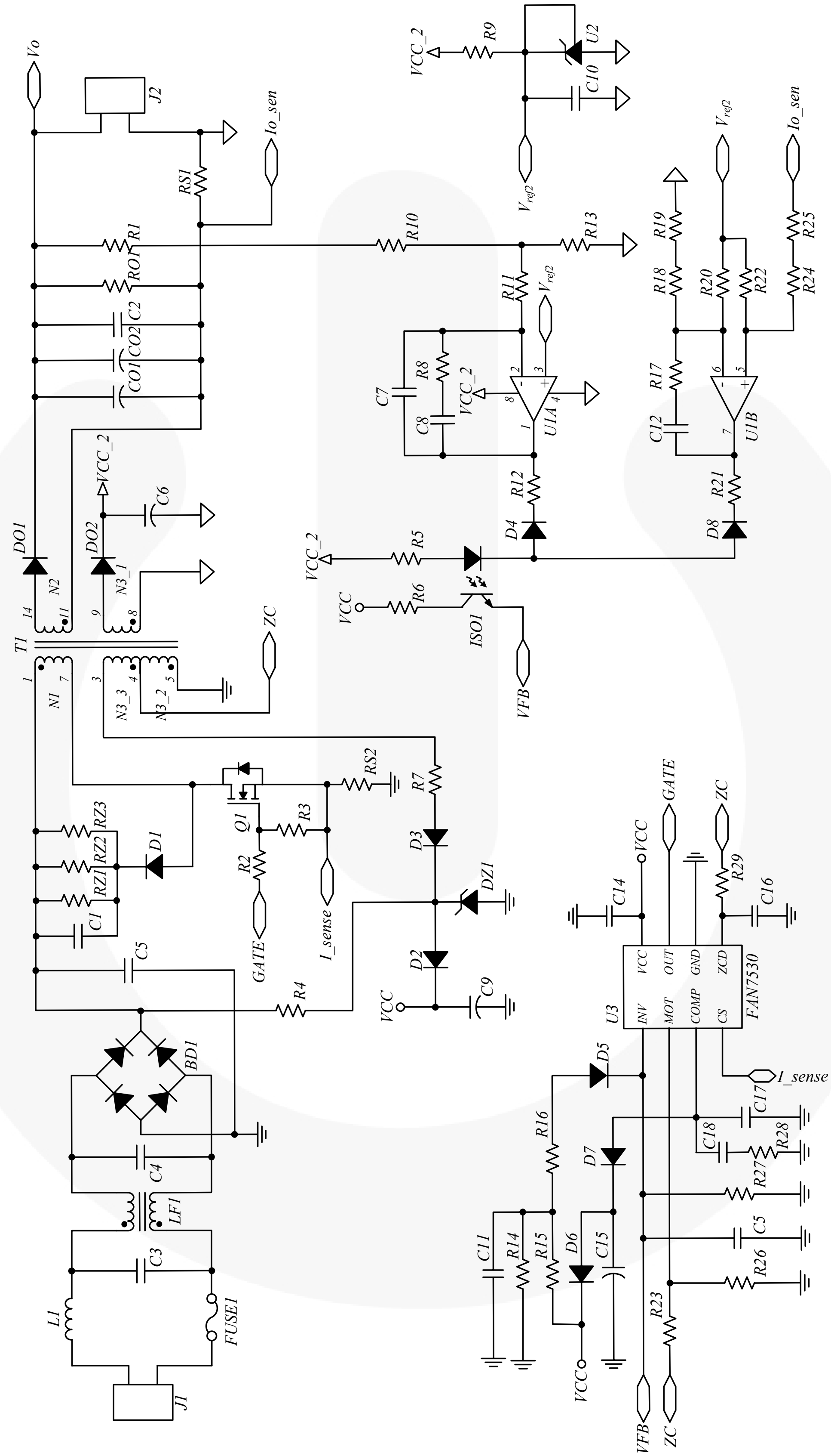


Figure 16. Schematic

Part List

Component	Symbol	Value/Part Number	Component	Symbol	Value/Part Number
Rectifier	BD1	GBU8J	Resistor	R1	49.9kΩ
Capacitor	C1	472/1kV		R2	15Ω
	C2	104		R3	1.5kΩ
	C3	220nF		R4	56kΩ/2Watt
	C4	440nF		R5	3.3kΩ
	C5	474/NP/630V		R6	11kΩ
	C6	33µ/35V		R7	1.5/1W
	C7	473		R8	100kΩ
	C8	224		R9	1.2kΩ
	C9	33µ/35V		R10	47kΩ
	C10	100p		R11	50kΩ
	C11	224		R12	11kΩ
	C12	155		R13	5.1kΩ
	C13	106		R14	1.2kΩ
	C14	105		R15	10kΩ
	C15	683		R16	33Ω
	C16	56p		R17	10kΩ
	C17	473		R18	2kΩ
	C18	224		R19	10Ω
	C19	105		R20	2kΩ
	CO1	2200µ/63V		R21	8.2kΩ
	CO2	2200µ/63V		R22	2kΩ
Diode	D1	UF4005		R23	330kΩ
	D2	RGF1J		R24	2.1kΩ
	D3	UF4005		R25	33Ω
	D4	1N4148		R26	30kΩ
	D5	1N4148		R27	5.1kΩ
	D6	1N4148		R28	100kΩ
	D7	1N4148		R29	47kΩ
	D8	1N4148		RO1	56kΩ/2Watt
	DO1	F06UP20S		RS1	0.05Ω/5Watt
	DO2	UF4005		RS2	0.1Ω/5Watt
Zener diode	DZ1	1N4746(18V)		RZ1	56kΩ/2Watt
Fuse	FUSE1	FUSE		RZ2	56kΩ/2Watt
Opto-coupler	ISO1	PC817		RZ3	56kΩ/2Watt
Connector	J1	CON4	Transformer	T1	EER3435
	J2	CON4	Op-Amp.	U1A,B	KA358
Inductor	L1	330µH	Regulator	U2	KA431
Chock-coil	LF1	EMI_CHOCK	PFC IC	U3	FAN7530
MOSFET	Q1	FQPF8N80C			

Related Datasheets

FAN7527 — Boundary Mode PFC Control IC

FAN7528 — Dual-Output Critical Conduction Mode PFC Controller

FAN7529 — Critical Conduction Mode PFC Controller

FAN7530 — Critical Conduction Mode PFC Controller

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