AN-8018: FAN9612 400W 4-Layer Evaluation Board User Guide (FEB-279)

Featured Fairchild Product: FAN9611 / FAN9612

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The following user guide supports the FAN9612 400W evaluation board for interleaved boundary-conduction mode power factor corrected supply. It should be used in conjunction with the FAN9612 datasheet as well as the Fairchild application note *AN-6086 Design Considerations for Interleaved Boundary-Conduction Mode PFC using FAN9612.* Please visit Fairchild's website at www.fairchildsemi.com for information.

1. Overview of the Evaluation Board

The FAN9612 interleaved dual Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) controller operates two parallel-connected boost power trains 180º out of phase. Interleaving extends the maximum practical power level of the control technique from about 300W to greater than 800W. Unlike the continuous conduction mode (CCM) technique often used at higher power levels, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be smaller due to ripple current cancellation between the power trains and effective the effective doubling of the switching frequency.

The advanced line feedforward with peak detection circuit minimizes the output voltage variation during line transients. To guarantee stable operation with less switching loss at light load, the maximum switching frequency is clamped at 600kHz. Synchronization is maintained under all operating conditions.

Protection functions built-in include output over-voltage, over-current, open-feedback, under-voltage lockout, brownout protection, and redundant latching over-voltage protection. The FAN9612 is available in a lead-free 16-lead SOIC package.

The FAN9612 evaluation board is a four-layer board. It is designed for 400W (400V/1A) rated power. Thanks to the phase management, the efficiency is maintained above 96% at low-line and high-line, even down to 10% of the rated output power. The efficiencies for full-load condition are 96.4% and 98.2% at line voltages of $115V_{AC}$ and $230V_{AC}$, respectively.

2. Key Features

- Low Total Harmonic Distortion, High Power Factor
- 180° Out-of-Phase Synchronization
- Automatic Phase Disable at Light Load
- 1.8A Sink, 1.0A Source, High-Current Gate Drivers
- Transconductance (g_M) Error Amplifier for Reduced Overshoot
- Voltage-Mode Control with $(V_{IN})^2$ Feedforward
- Closed-Loop Soft-Start with Programmable Soft-Start Time for Reduced Overshoot
- Minimum Restart Timer Frequency to Avoid Audible Noise
- Maximum Switching Frequency Clamp
- Brownout Protection with Soft Recovery
- Non-Latching OVP on FB Pin and Second-Level Latching Protection on OVP Pin
- Open-Feedback Protection
- Over-Current and Power-Limit Protection for Each Phase
- Low Startup Current: 80µA Typical
- Works with DC, 50Hz to 400Hz AC Inputs

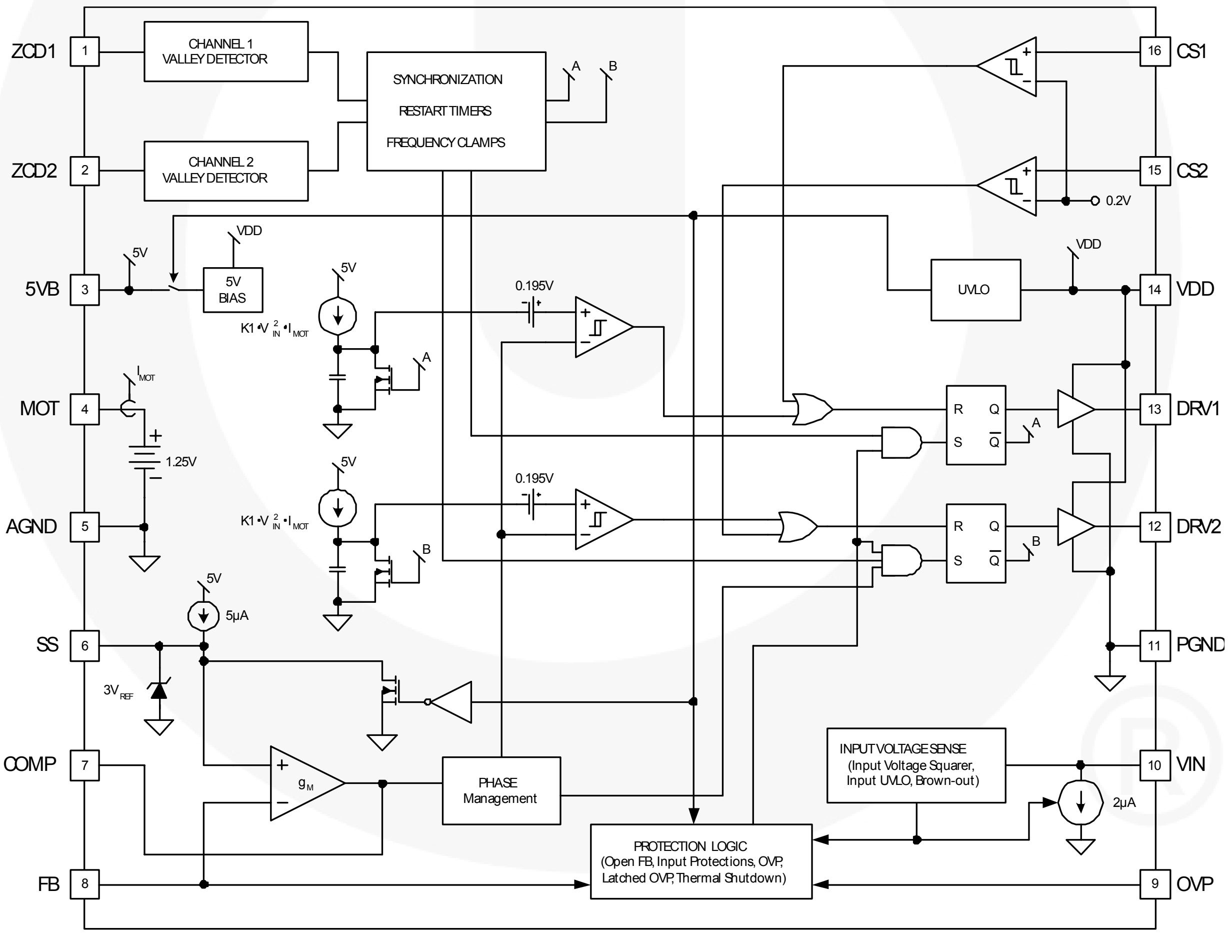


Figure 1. Block Diagram

3. Specifications

This board has been designed and optimized for the following conditions:

Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
V_{IN} Nominal : 85~265V_{AC} V_{DD} Supply : 13V_{DC}~18V_{DC}	400W	400V-1A

Note:
1. Minimum output voltage during 20ms hold up time is 330V_{DC}

- V_{LINE} = 85~265V_{AC}
- V_{OUT} = 400V
- f_{SW} > 50kHz
- Efficiency > 96% down to 20% load (115V_{AC})
- Efficiency > 97% down to 20% load (230V_{AC})
- PF > 0.98 at full load

The trip points of the built-in protections are set as below in the evaluation board.

- The non-latching output OVP trip point is set at 108% of the nominal output voltage.
- The latching output OVP trip point is set at 117% of the nominal output voltage.
- The line UVLO (brownout protection) trip point is set at 70V_{AC} (10V_{AC} hysteresis).
- The line OVP trip point is set at 267V_{AC}.
- The pulse-by-pulse current limit for each MOSFET is set at 9.1A.

The maximum power limit is set at around 130% of the rated output power. The phase management function permits phase shedding at 30% of the limited maximum power (around 150W). The two-channel interleaving operation comes back when the output power exceeds 40% of the limited maximum power (around 200W).

4. Test Procedure

Before testing the board; DC voltage supply for V_{DD}, AC voltage supply for line input, and DC electric load for output should be connected to the board properly.

1. Supply V_{DD} for the control chip first. It should be higher than 13V *(refer to the specification for V_{DD} turn-on threshold voltage).*
2. When V_{DD} is supplied, a "click" sound from the relay is heard. This is normal. Since the inrush current limit relay is turned on by 5V reference (pin #3), the relay turns on when FAN9612 comes out of UVLO by supplying V_{DD} higher than 13V.

Table 1. Specifications Excerpt from Datasheet

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
I_{START_UP}	Startup Supply Current	$V_{DD} = V_{ON} - 0.2V$		80	110	μA
I_{DD}	Operating Current	Output Not Switching		2.5	4.0	mA
I_{DD_DYM}	Dynamic Operating Current	f_{SW} = 50 kHz; C_{LOAD} = 2nF		3	5	mA
V_{ON}	UVLO Start Threshold Voltage	V_{DD} Increasing	12.0	12.5	13	V
V_{OFF}	UVLO Stop Threshold Voltage	V_{DD} Decreasing	7.0	7.5	8.0	V
	UVLO Hysteresis			5.0		V

3. Connect the AC voltage (85~265V_{AC}) to start the FAN9612. Since FAN9612 has brownout protection and line OVP, any input voltages out of operation range trigger protections.
4. Change load current (0~1A) and check the operation. The board is designed to go into phase shedding for output power below around 150W. It goes back to two-channel interleaving operation for output power above around 200W.
5. Q4 and D11 in the Figure 2 allow the evaluation board to run at low V_{DD} voltage, down to 8.5V. When line voltage is applied with low V_{DD} voltage (8.5~12V), Q4 is turned off initially and V_{DD} is charged up to V_{DD} turn-on threshold voltage through diode D11, which allows the converter to startup with low V_{DD} voltage. Once the controller starts up, Q4 is turned on and D11 is reverse biased.

5. Schematic

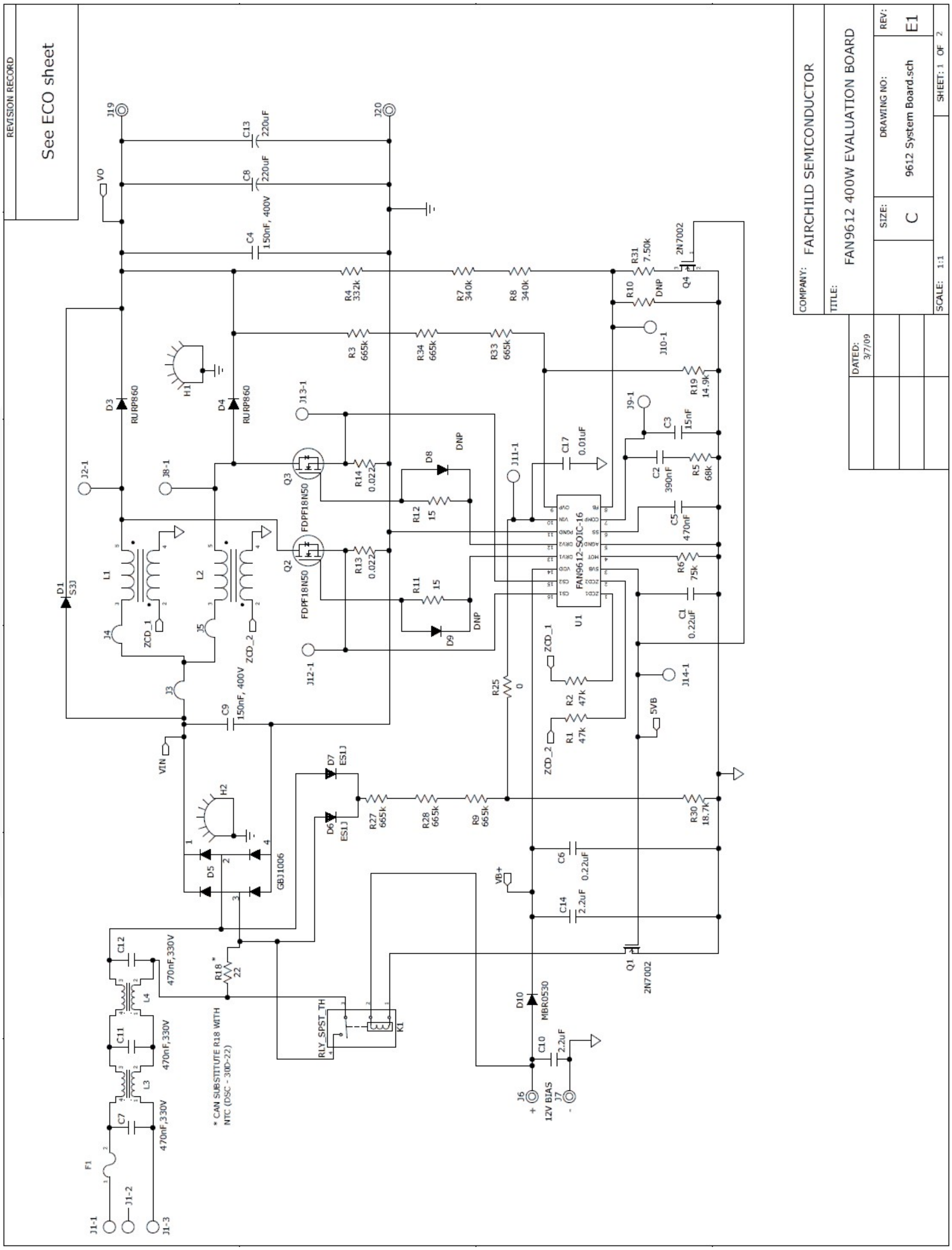


Figure 2. 400W Evaluation Board Schematic

6. Boost Inductor Specification

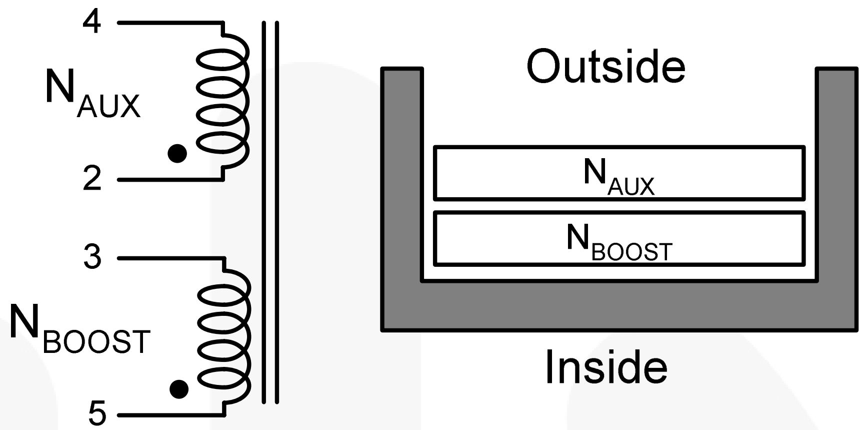
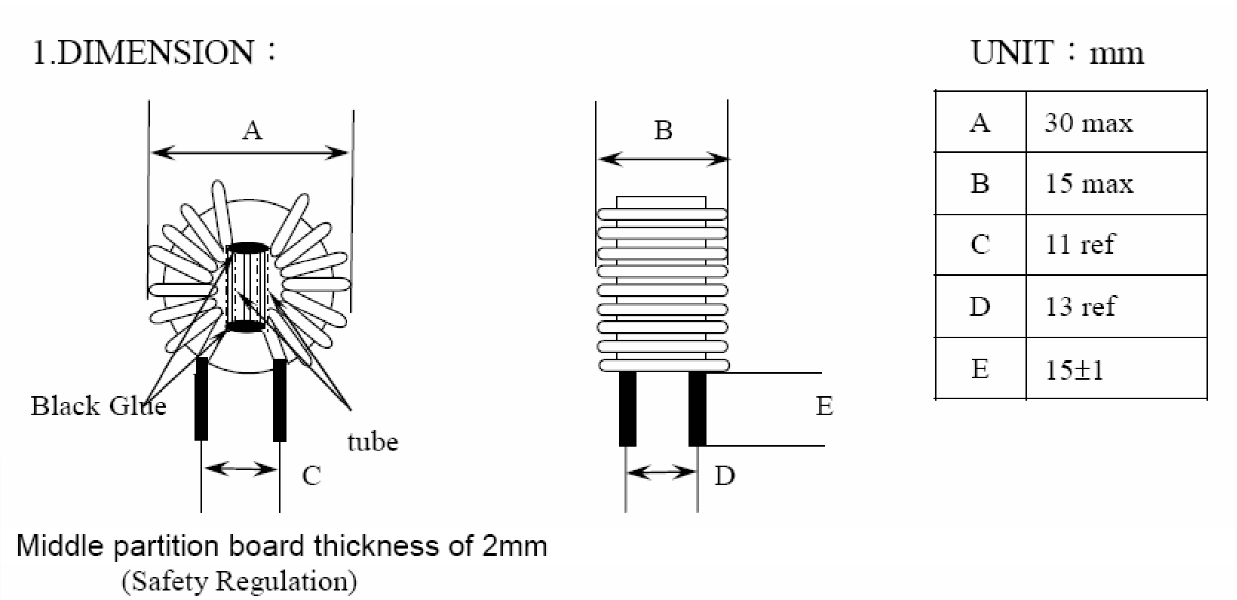


Figure 3. Boost Inductor used in the Evaluation Board

	Pin	Diameter / Thickness	Turns
N1	5 → 3	0.1mm × 100 (Litz Wire)	30
Insulation Tape		0.05mm	3
N2	2 → 4	0.2mm	3
Insulation Tape		0.05mm	3

Core : PQ3230 (Ae=161mm^2)
Bobbin: PQ3230
Inductance : 200µH

7. Line Filter Inductor Specification



2. ELECTRICAL SPECIFICATION: at 1KHz, 1V
   - 2.1 INDUCTANCE : L1=L2 :9.0mH min
   - 2.2 DC RESISTANCE : L1=L2: 0.05Ohm max
   - 2.3 TURN & WIRE : L1=L2: Φ0.9 x 30.5Tsx2

Figure 4. Line Filter Inductor Specification

Table 2. Materials List

Component	Material	Manufacturer	UL File Number
Core	T22x14x08	Core T22x14x08, TOMITA	
Wire	THFN-216	Ta Ya Electric Wire Co,. Ltd.	E197768
	UEWN/U	PACIFIC Wire and cable Co., Ltd.	E201757
	UEWE	Tai-1 Electric Wire & Cable Co., Ltd.	E85640
	UWY	Jang Shing Wire Co., Ltd.	E174837
Solder	96.5%, Sn, 3%, Ag, 0.5% Cu	Xin Yuan Co., Ltd.	

8. BOM

Qty	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	C1, C6		0.22µF	CAP, SMD, CERAMIC, 25V, X7R	805	Vishay
2	C10, C14		2.2µF	CAP, SMD, CERAMIC, 25V, X7R	1206	Vishay
1	C17		0.01µF	CAP, SMD, CERAMIC, 25V, X7R	805	Vishay
1	C2		390nF	CAP, SMD, CERAMIC, 25V, X7R	805	Vishay
1	C3		15nF	CAP, SMD, CERAMIC, 25V, X7R	805	Vishay
2	C4, C9	ECW-F4154JL	150nF, 400V	Cap, 400V, 5%, Polypropylene	Thru-hole	Panasonic-ECG
1	C5		470nF	CAP, SMD, CERAMIC, 25V, X7R	805	Vishay
3	C7, C11-12	B32914A3474	470nF,330V	Cap, 330V_{AC}, 10%, Polypropylene	Thru-hole	EPCOS
2	C8, C13	KMH450V220uF	220µF	Cap, Alum, Elect.	Thru-hole	Samyoung
1	D1	S3J		Diode, 600V, 3A, Std Recovery	SMC	Fairchild Semiconductor
2	D3-4	RURP860		Diode, Ultra-Fast, 600V 8A	T0-220AC	Fairchild Semiconductor
1	D5	GBJ1006		Bridge Rectifier, 600V, 10A	Thru-hole	Diodes Inc.
2	D6-7	ES1J		DIODE FAST REC 1A 600V	SMA	Fairchild Semiconductor
3	D8-9	MBR0530[(3)]		DIODE SCHOTTKY 30V 500mA SOD123	SOD-123	Fairchild Semiconductor
3	D10	MBR0530		DIODE SCHOTTKY 30V 500mA SOD123	SOD-123	Fairchild Semiconductor
1	F1	31.8201		Fuseholder, 5x20mm, 250V_{AC}, 10A	PCB mount, Thru-hole	Schurter Inc
1	Fuse	0217010.HXP	10A	Fuse, 250V, IEC, FA, LBC, 5x20, 10A, Fast	Cartridge	Littlefuse Inc.
2	H1-2			Heatsink		
1	J1	ED100/3DS		Terminal Block, 5MM Vert., 3 Pos.	Thru-hole	On Shore Technology, Inc.
8	J2, J8-14			Generic 1-Pin Connector (PROBE)		
3	J3-5			Jumper Wire, #16, Insulated, for Current Probe Measurement	Thru-hole	
4	J6-7, J19-20	108-0740-001		Connector, Banana Jack, Un-insulated, Panel Mount	Thru-hole	Emerson Network Power Connectivity Solutions
1	K1	PB134012		RELAY PWR SPST-NO 10A 12VDC PCB	Thru-hole	Tyco
2	L1-2	Custom Inductor		Coupled Inductor, Pri-30T, Sec-3T, BPQ3230-1112CP	Thru-hole	TDK
2	L3-4	TRN-0197		Common Mode Choke	Thru-hole	SEN HUEI INDUSTRIAL CO.,LTD
2	Q1, Q4	2N7002		MOSFET N-CH 60V 300mA	SOT-123	Fairchild Semiconductor
2	Q2-3	FDPF18N50		MOSFET, NCH, 500V, 18A, 0.265Ω	TO-220	Fairchild Semiconductor

Continued on following page…

BOM (Continued)

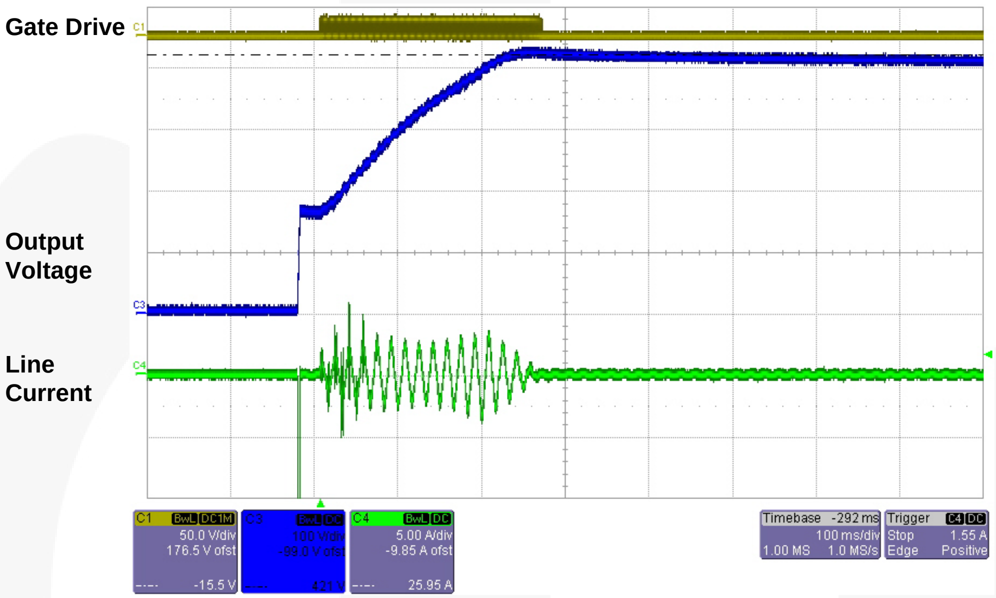
Qty	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	R1-2		47k	RES, SMD, 1/8W	805	Vishay
6	R3, R9, R27-28, R33-34		665k	RES, SMD, 1/8W	805	Vishay
1	R4		332k	RES, SMD, 1/8W	805	Vishay
1	R5		68k	RES, SMD, 1/8W	805	Vishay
1	R6		75k	RES, SMD, 1/8W	805	Vishay
2	R7-8		340k	RES, SMD, 1/8W	805	Vishay
3	R10		7.5k(3)	RES, SMD, 1/8W	805	Vishay
2	R11-12		15	RES, SMD, 1/8W	805	Vishay
2	R13-14		0.022	RES, SMD, 1/2W	1812	Vishay
1	R18		22	RES BODY:250 CENTERS:800	Thru-hole	Vishay
1	R19		14.9k	RES, SMD, 1/8W	805	Vishay
1	R25		0	RES, SMD, 1/8W	805	Vishay
1	R30		18.7k	RES, SMD, 1/8W	805	Vishay
1	R31		7.5k	RES, SMD, 1/8W	805	Vishay
1	U1	FAN9612		Interleaved Dual BCM PFC Controller	SOIC-16	Fairchild Semiconductor

Note:
3. Do not populate.

9. Test Results

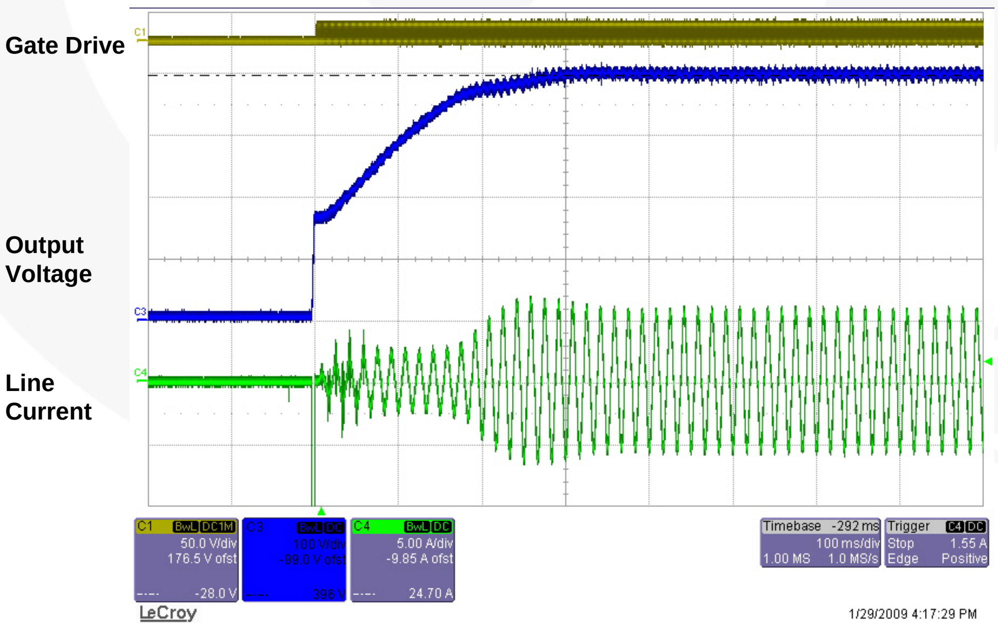
9.1. Startup

Figure 5 and Figure 6 show the startup operation at 115V_{AC} line voltage for no-load and full-load condition, respectively. Due to the closed-loop soft-start, only 21V overshoot is observed (5% of nominal output voltage) for no-load startup. Almost no overshoot is observed for full-load startup.



CH1: Channel 1 Gate Drive Voltage (20V/div), CH3: Output Voltage (100V/div), CH4: Line Current (5AV/div), Time (100ms/div)

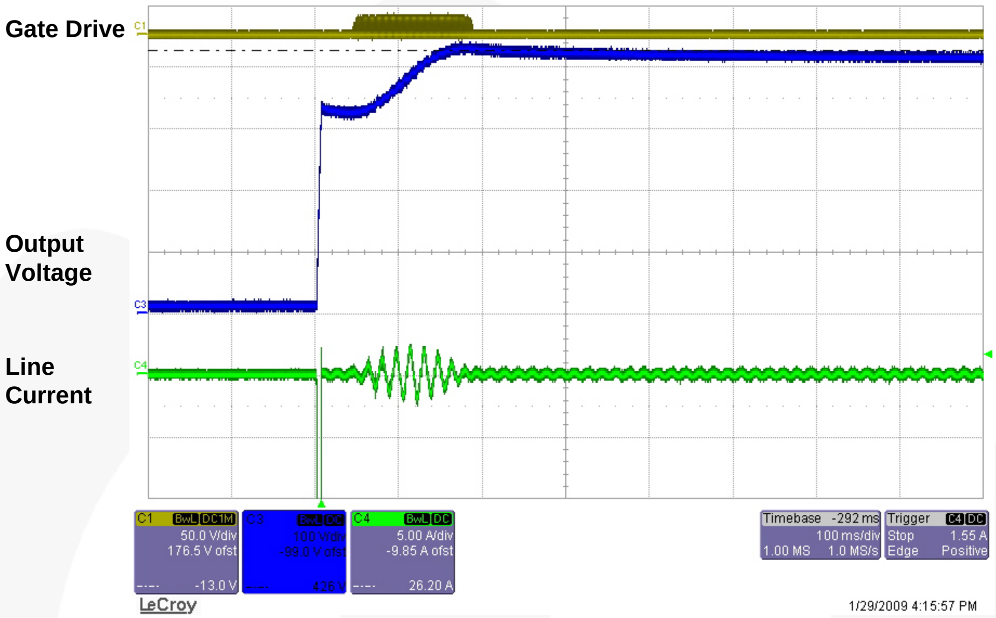
Figure 5. No-Load Startup at 115V_{AC}



CH1: Channel 1 Gate Drive Voltage (20V/div), CH3: Output Voltage (100V/div), CH4: Line Current (5AV/div), Time (100ms/div)

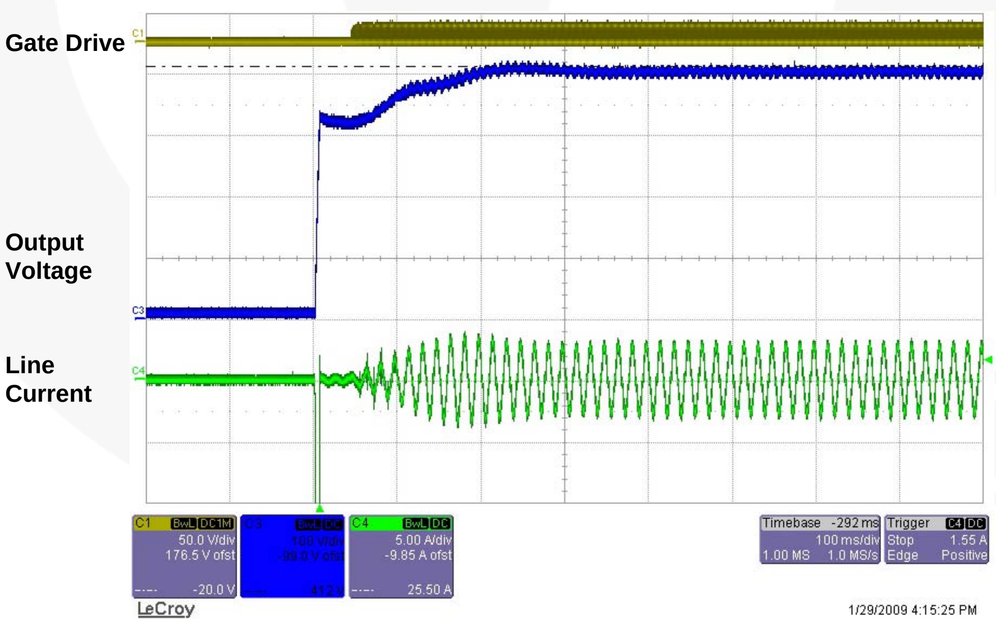
Figure 6. Full-Load Startup at 115V_{AC}

Figure 7 and Figure 8 show the startup operation at $230V_{AC}$ line voltage for no-load and full-load conditions, respectively. Due to the closed-loop soft-start, only 26V overshoot is observed (6.5% of nominal output voltage) for no-load startup and only 12V (3% of nominal output voltage) overshoot is observed for full-load startup.



CH1: Channel 1 Gate Drive Voltage (20V/div), CH3: Output Voltage (100V/div), CH4: Line Current (5AV/div), Time (100ms/div)

Figure 7. No-Load Startup at $230V_{AC}$

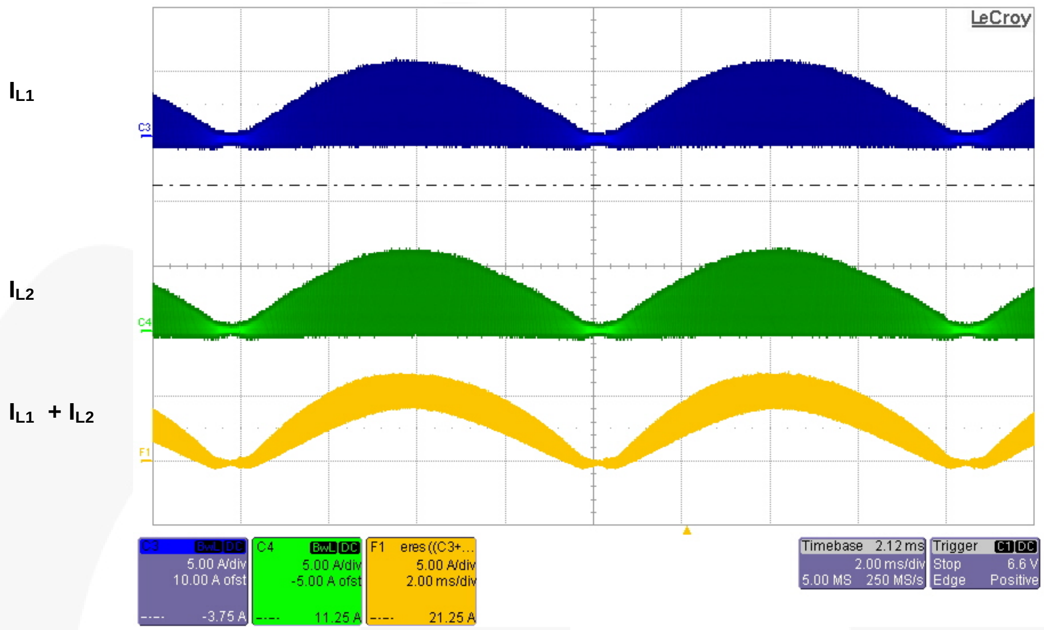


CH1: Channel 1 Gate Drive Voltage (20V/div), CH3: Output Voltage (100V/div), CH4: Line Current (5AV/div), Time (100ms/div)

Figure 8. Full-Load Startup at $230V_{AC}$

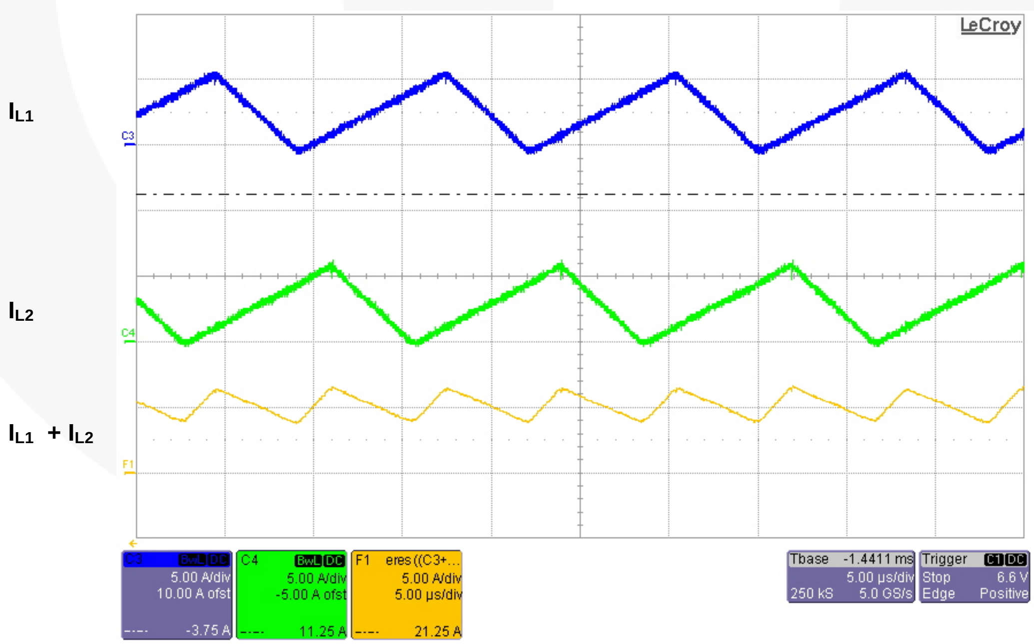
9.2. Normal Operation

Figure 9 and Figure 10 show the two inductor currents and sum of two inductor currents at 115V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (5A/div), CH4: Inductor L2 Current (5A/div),
F1: Sum of Two Inductor Current (5AV/div), Time (2ms/div)

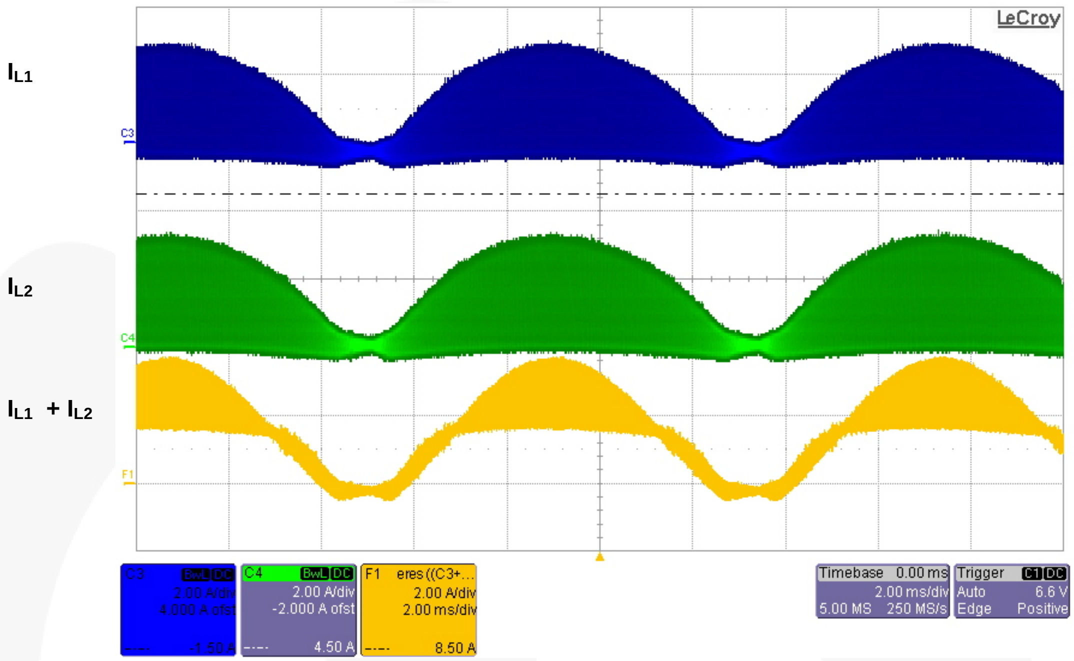
Figure 9. Inductor Current Waveforms at Full-Load and 115V_{AC}



CH3: Inductor L1 Current (5A/div), CH4: Inductor L2 Current (5A/div),
F1: Sum of Two Inductor Current (5AV/div), Time (5µs/div)

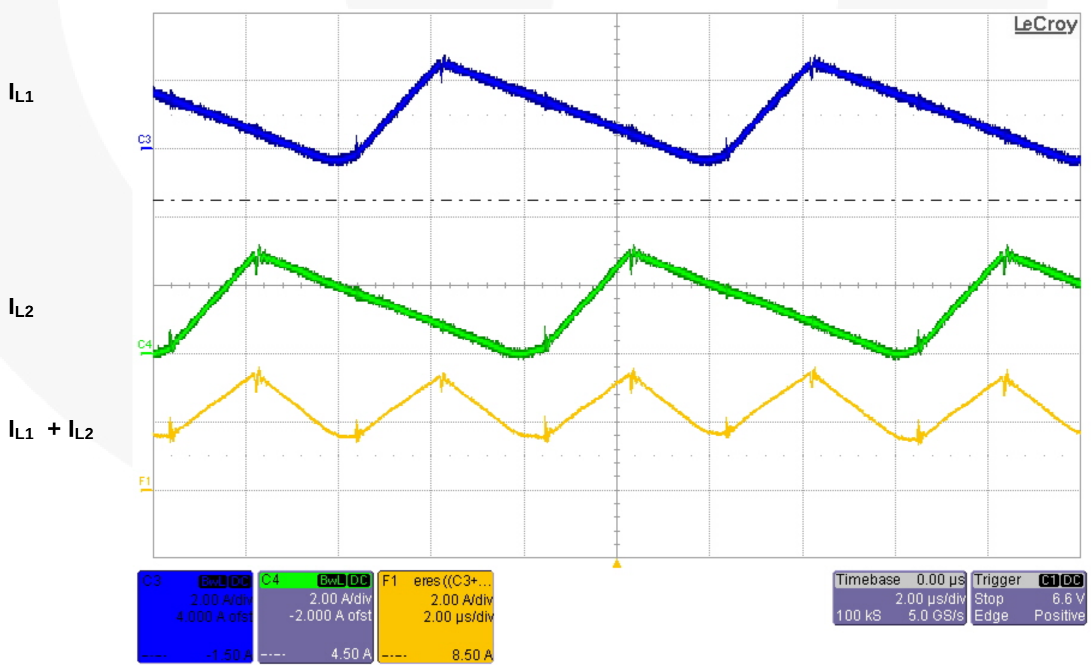
Figure 10. Zoom of Inductor Current Waveforms of Figure 11 at Peak of Line Voltage

Figure 11 and Figure 12 show the two inductor currents and sum of two inductor currents at 230V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (2A/div), CH4: Inductor L2 Current (2A/div),
F1: Sum of Two Inductor Current (2AV/div), Time (2ms/div)

Figure 11. Inductor Current Waveforms at Full-Load and 230V_{AC}

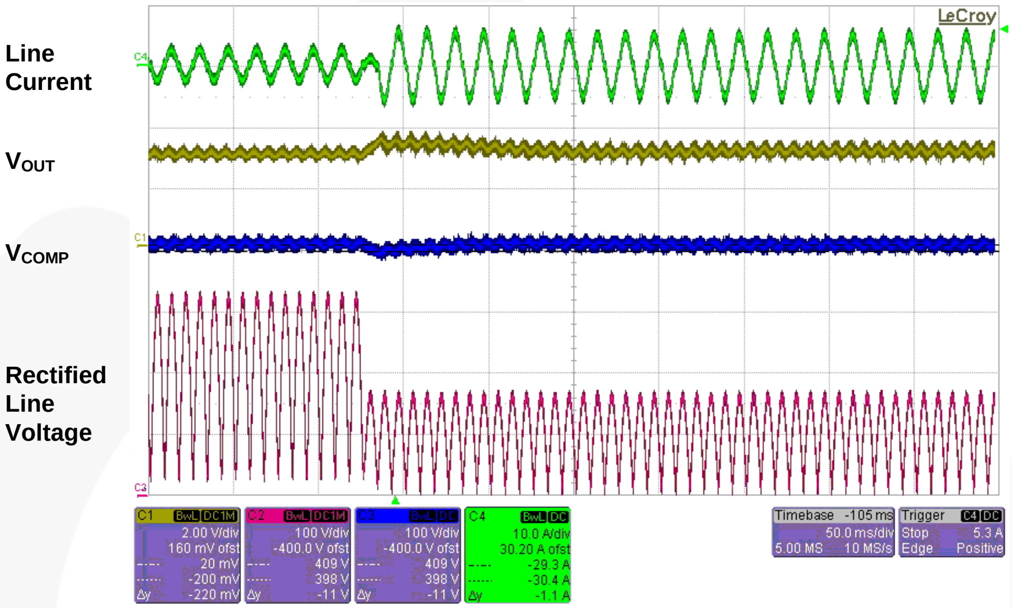


CH3: Inductor L1 Current (2A/div), CH4: Inductor L2 Current (2A/div),
F1: Sum of Two Inductor Current (2AV/div), Time (2µs/div)

Figure 12. Zoom of Inductor Current Waveforms of Figure 13 at Peak of Line Voltage

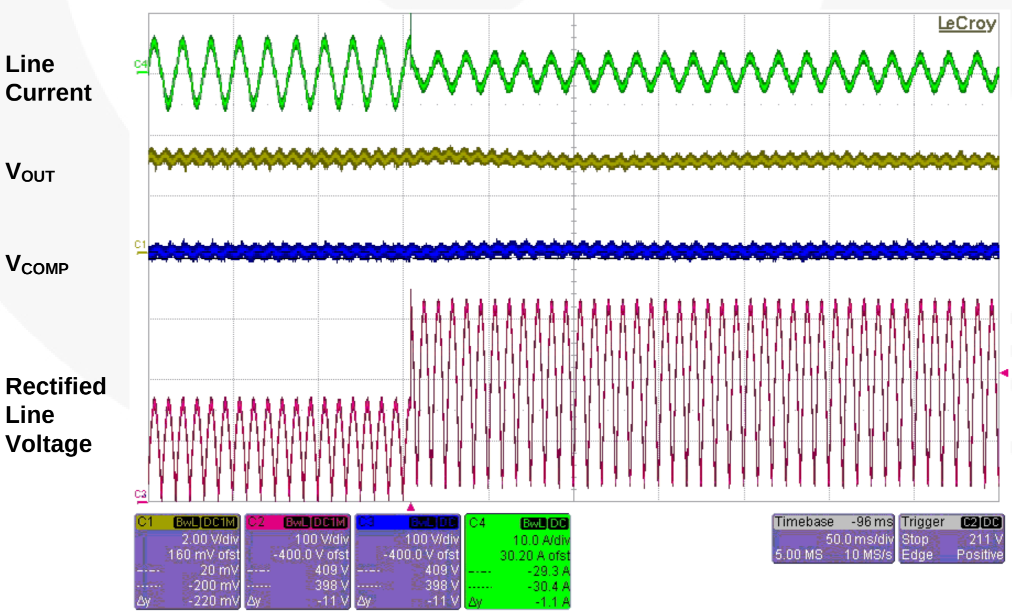
9.3. Line Transient

Figure 13 and Figure 14 show the line transient operation and minimal effect on output voltage due to the line feedforward function. When the line voltage changes from $230V_{AC}$ to $115V_{AC}$, 11V (2.8% of nominal output voltage) voltage undershoot is observed. When the line voltage changes from $115V_{AC}$ to $230V_{AC}$, almost no voltage undershoot is observed.



CH1: COMP Pin Voltage (2V/div), CH2: Rectified Line Voltage (100V/div)
CH3: Output Voltage (100V/div), CH4: Line Current (10AV/div), Time (50ms/div)

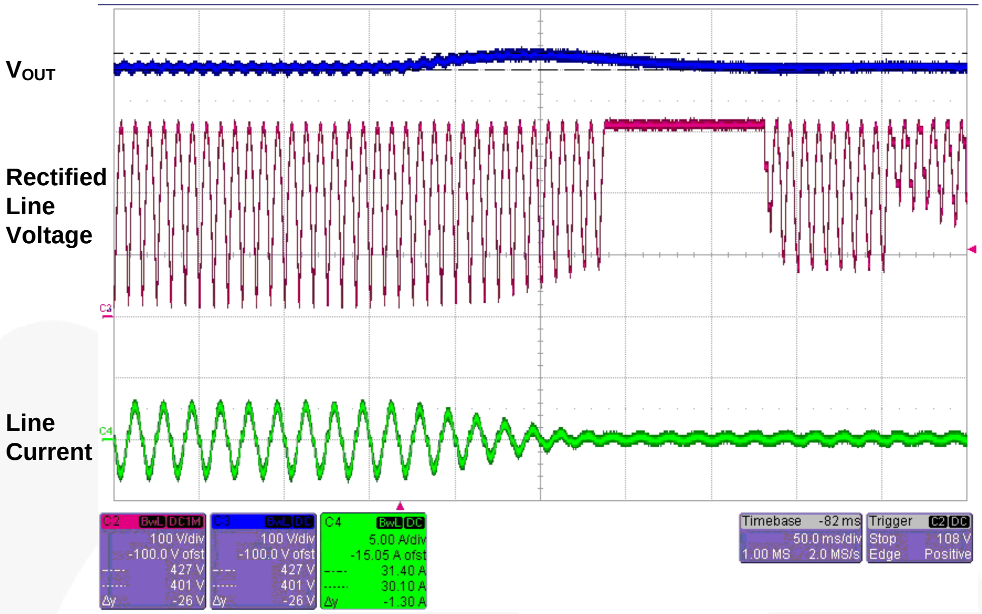
Figure 13. Line Transient Response at Full-Load Condition ($230V_{AC}$ → $115V_{AC}$)



CH1: COMP Pin Voltage (2V/div), CH2: Rectified Line Voltage (100V/div)
CH3: Output Voltage (100V/div), CH4: Line Current (10AV/div), Time (50ms/div)

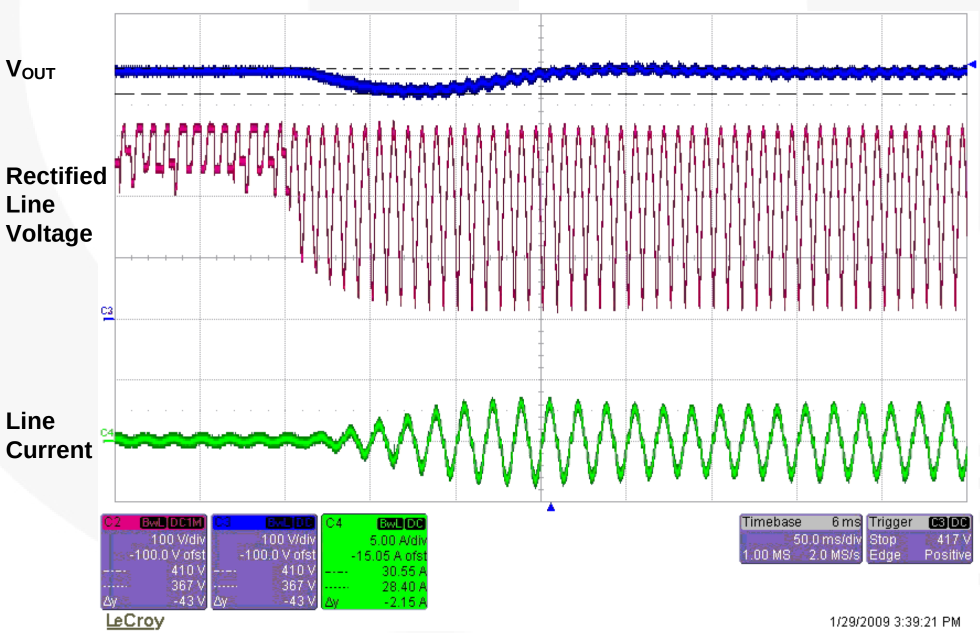
Figure 14. Line Transient Response at Full-Load Condition ($115V_{AC}$ → $230V_{AC}$)

Figure 15 and Figure 16 show the load-transient operation. When the output load changes from 100% to 0%, 26V (6.5% of nominal output voltage) voltage overshoot is observed. When the output load changes from 0% to 100%, 43V (11% of nominal output voltage) voltage undershoot is observed.



CH2: Rectified line voltage (100V/div), CH3: Output voltage (100V/div),
CH4: Line current (10AV/div), Time (50ms/div)

Figure 15. Load Transient Response at 230V_{AC} (Full-Load → No-Load)

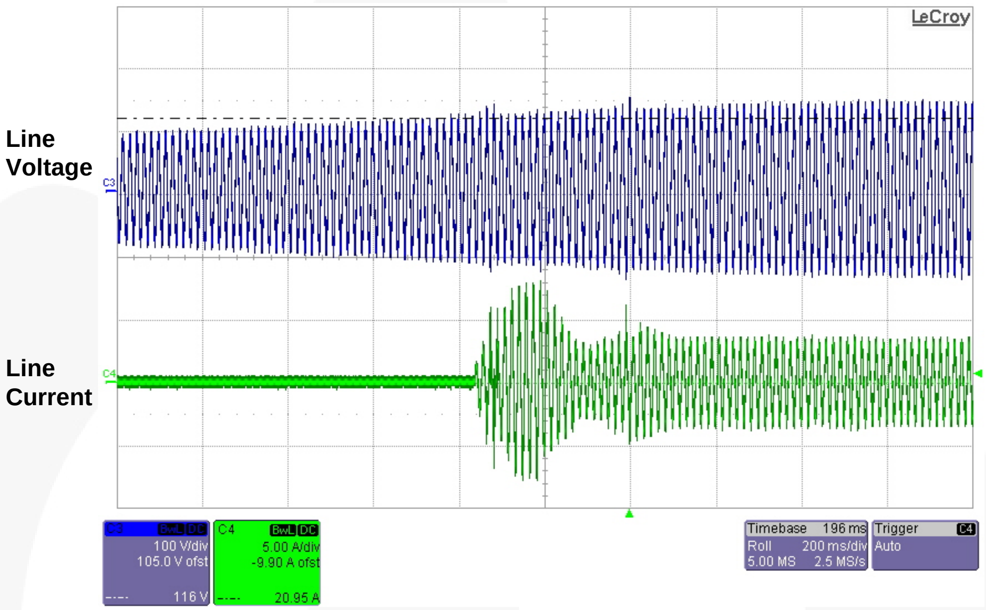


CH2: Rectified Line Voltage (100V/div), CH3: Output Voltage (100V/div),
CH4: Line Current (10AV/div), Time (50ms/div)

Figure 16. Load Transient Response at 230V_{AC} (No-Load → Full-Load)

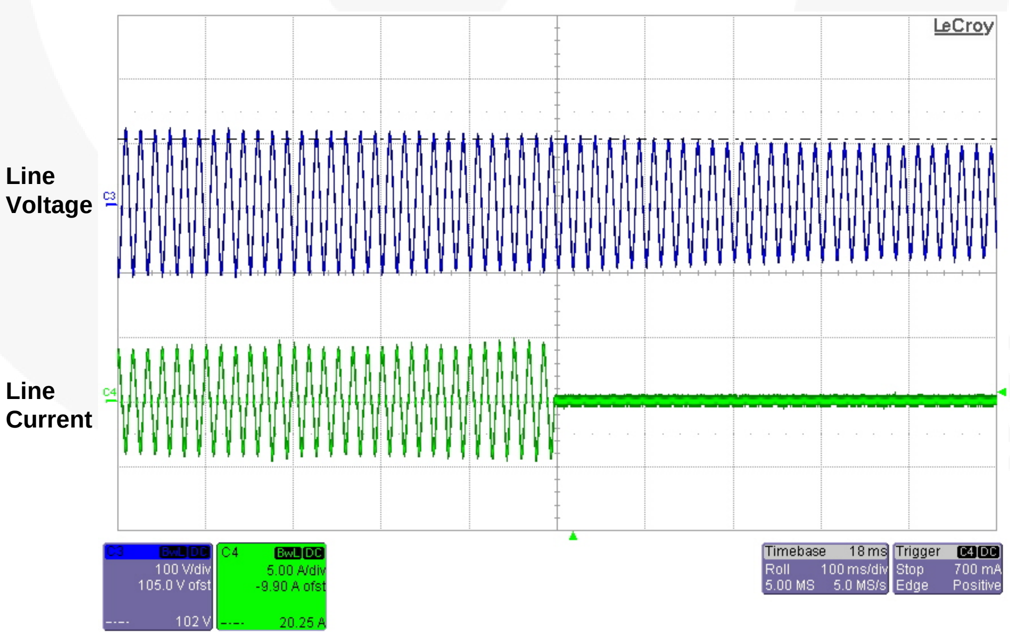
9.4. Brownout Protection

Figure 17 and Figure 18 show the startup and shutdown operation at slowly increasing and decreasing line voltage, respectively. The power supply starts up when the line voltage reaches around $80V_{AC}$ and shuts down when line voltage drops below $70V_{AC}$.



CH3: Line Voltage (100V/div), CH4: Line Current (5AV/div), Time (100ms/div)

Figure 17. Startup when Slowly Increasing the Line Voltage

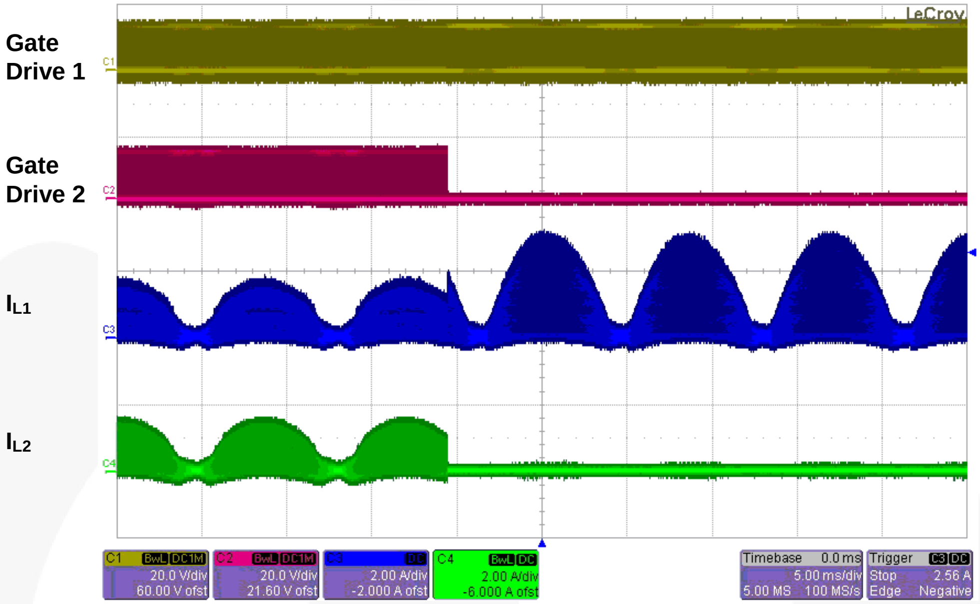


CH3: Line Voltage (100V/div), CH4: Line Current (5AV/div), Time (200ms/div)

Figure 18. Shutdown when Slowly Decreasing the Line Voltage

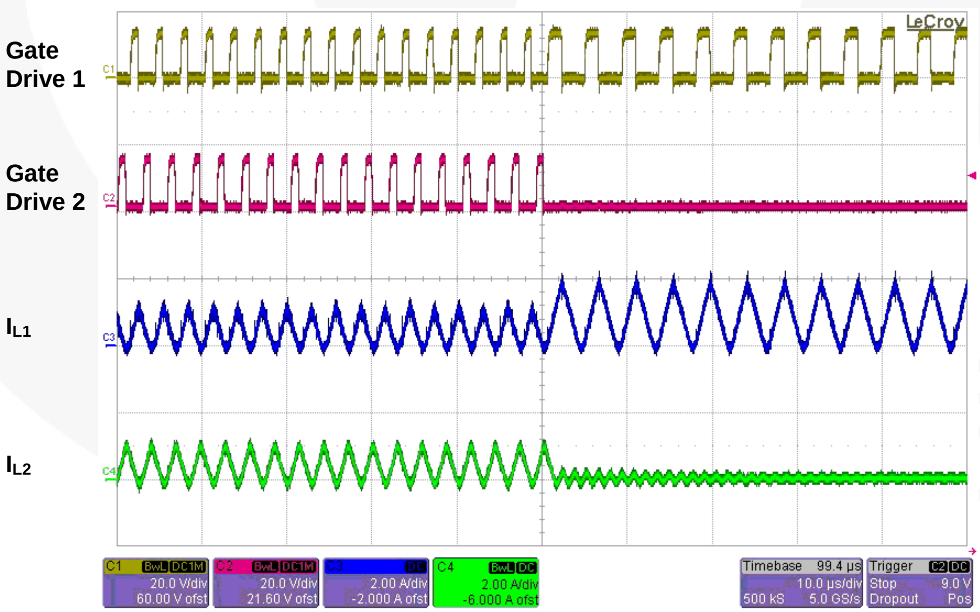
9.5. Phase Management

Figure 19 and Figure 20 show the phase-shedding waveforms. As observed, the duty cycle of Channel 1 gate drive signal is doubled when the other channel gate drive signal is disabled to minimize the line current glitch.



CH1: Channel 1 Gate Drive Voltage (20V/div), CH2: Channel 2 Gate Drive Voltage (20V/div), CH3: Inductor L1 Current (5AV/div), CH4: Inductor L2 Current (5AV/div), Time (5ms/div)

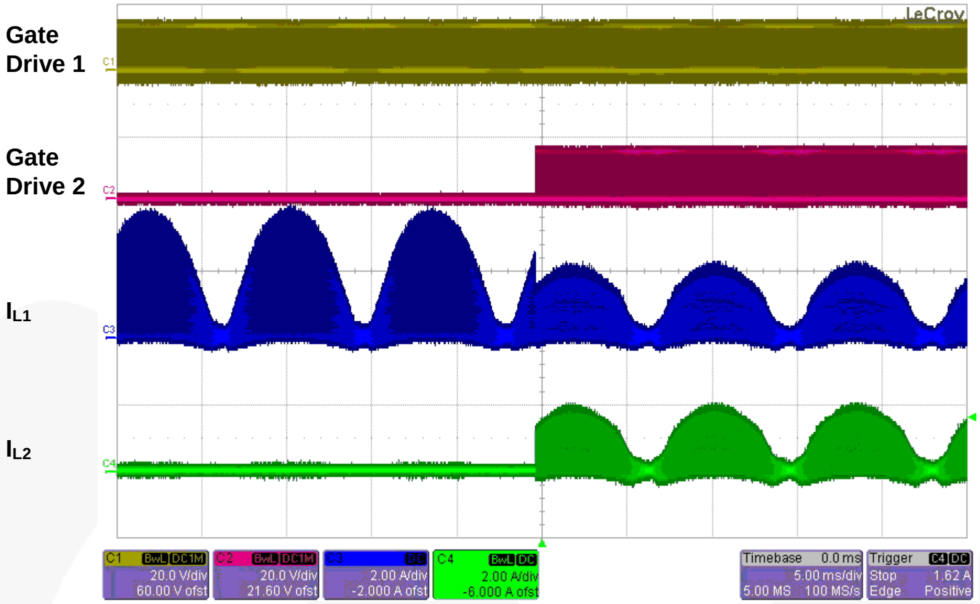
Figure 19. Phase-Shedding Operation



CH1: Channel 1 Gate Drive Voltage (20V/div), CH2: Channel 2 Gate Drive Voltage (20V/div), CH3: Inductor L1 Current (5AV/div), CH4: Inductor L2 Current (5AV/div), Time (10µs/div)

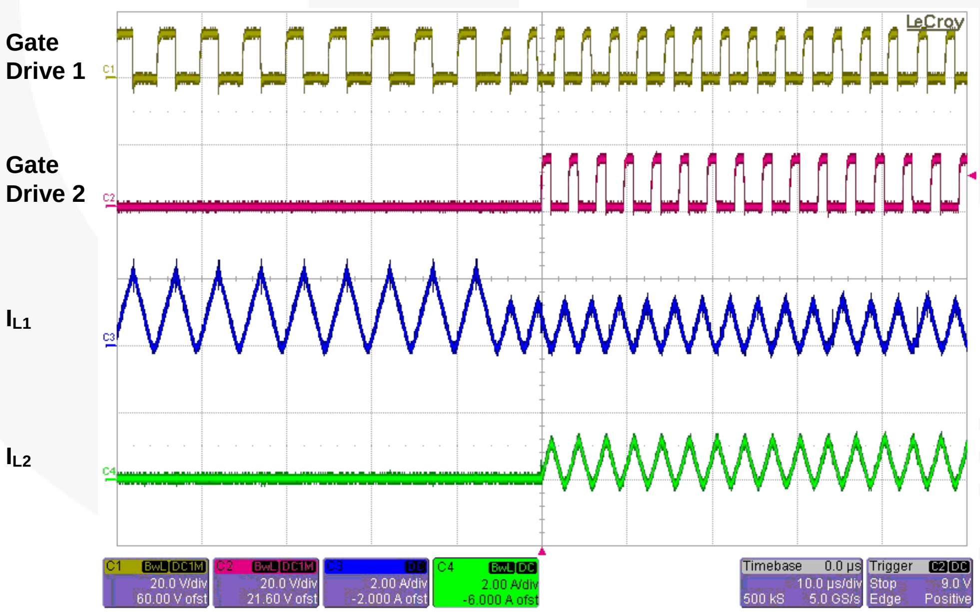
Figure 20. Phase-Shedding Operation

Figure 21 and Figure 22 show the phase-adding waveforms. As observed, the duty cycle of Channel 1 gate drive signal becomes half just before the other channel gate drive signal is enabled to minimize the line current glitch.



CH1: Channel 1 Gate Drive Voltage (20V/div), CH2: Channel 2 Gate Drive Voltage (20V/div), CH3: Inductor L1 Current (5AV/div), CH4: Inductor L2 Current (5AV/div), Time (5ms/div)

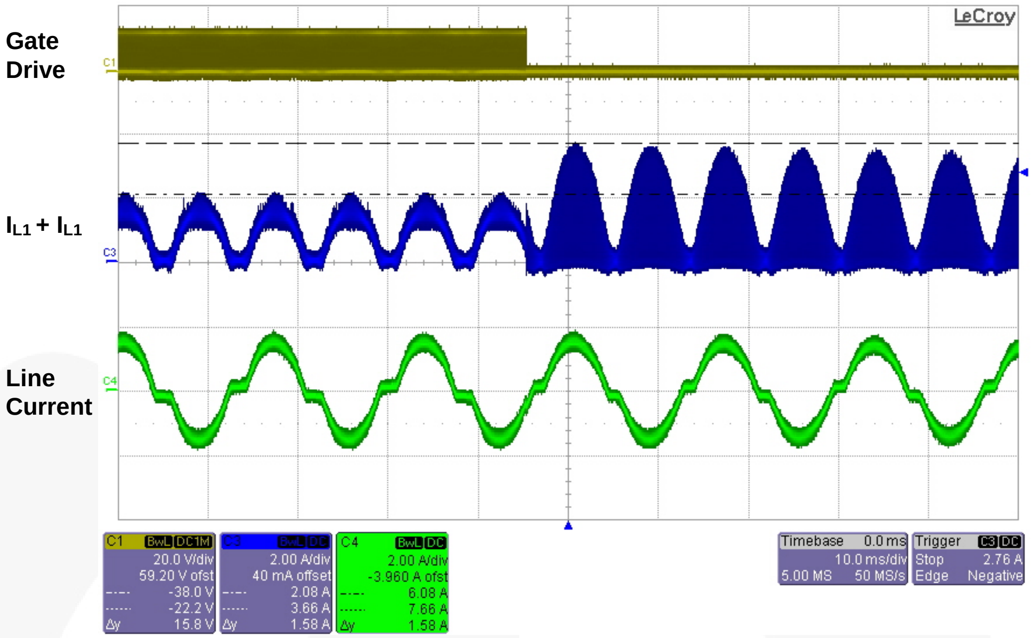
Figure 21. Phase-Adding Operation (Zoom-In)



CH1: Channel 1 Gate Drive Voltage (20V/div), CH2: Channel 2 Gate Drive Voltage (20V/div), CH3: Inductor L1 Current (5AV/div), CH4: Inductor L2 Current (5AV/div), Time (10µs/div)

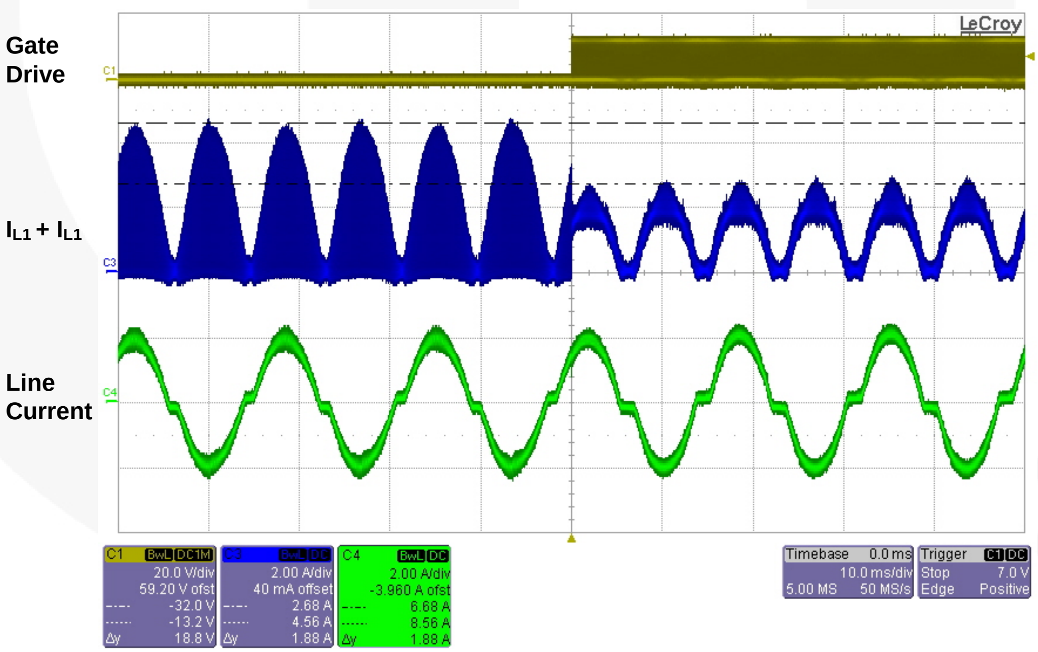
Figure 22. Phase-Adding Operation (Zoom-In)

Figure 23 and Figure 24 show the sum of two-inductor current and line current for phase shedding and adding, respectively. As shown, the phase management causes no visible change in the line current waveforms.



CH1: Channel 2 Gate Drive Voltage (20V/div), CH3: Sum of Two Inductor Currents (2A/div), CH4: Line Current (2AV/div), Time (10ms/div)

Figure 23. Phase Shedding and Line Current



CH1: Channel 2 Gate Drive Voltage (20V/div), CH3: Sum of Two Inductor Currents (2A/div), CH4: Line Current (2AV/div), Time (10ms/div)

Figure 24. Phase Adding Operation and Line Current

9.6. Efficiency

Figure 25 and Figure 26 show the measured efficiency of the evaluation board with and without phase management at input voltages of $115V_{AC}$ and $230V_{AC}$, respectively. These plots show that phase management improves the efficiency at light load by 1% up to 7%, depending on the line voltage and load condition. Since phase shedding reduces the switching loss by effectively decreasing the switching frequency at light load, a greater efficiency improvement is achieved at high line where switching losses are more. Relatively less improvement is obtained for low line since the MOSFET is turned on with zero voltage and switching losses are negligible.

Since an external power supply is used for V_{DD}, the power consumption of the control IC is not included, but is minimal (<1W).

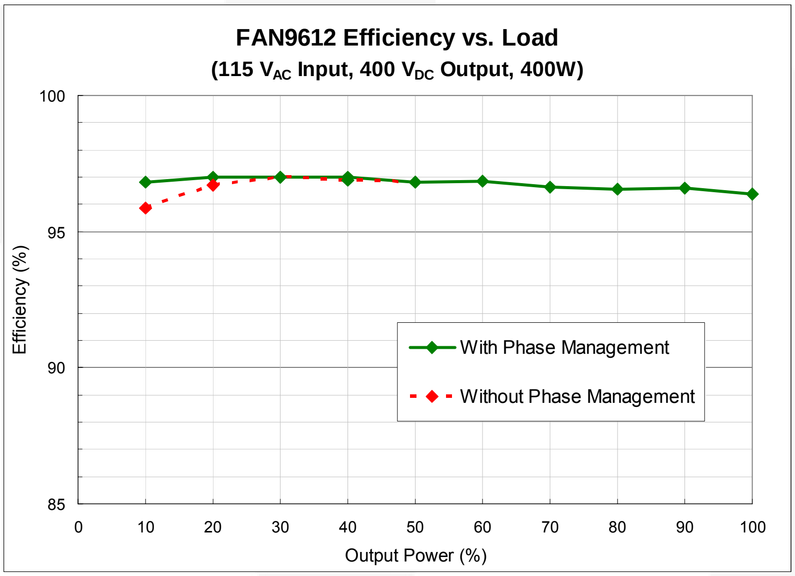


Figure 25. Measured Efficiency at $115V_{AC}$

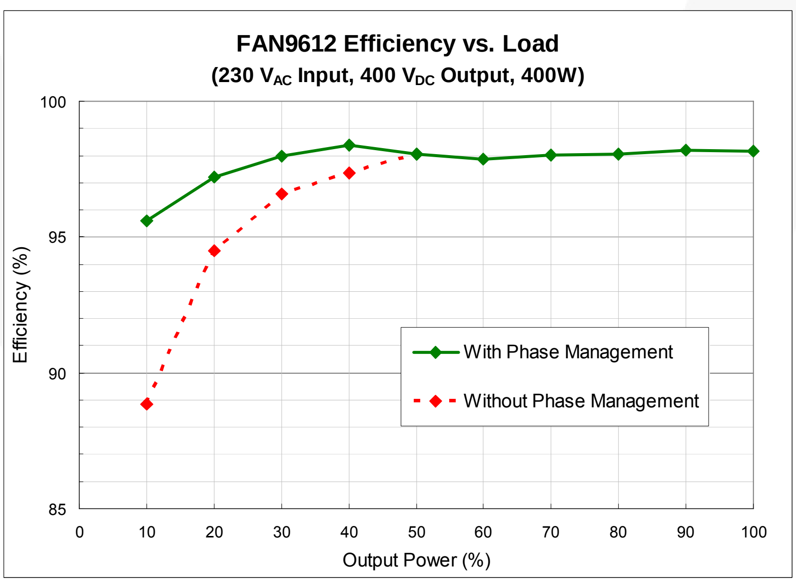


Figure 26. Measured Efficiency at $230V_{AC}$

9.7. Harmonic Distortion and Power Factor

Figure 27 and Figure 28 compare the measured harmonic current with EN61000 class D and C, respectively, at input voltage of $115V_{AC}$ and $230V_{AC}$. Class D is applied to TV and PC power, while Class C is applied to lighting application. As can be observed, both regulations are met with sufficient margin.

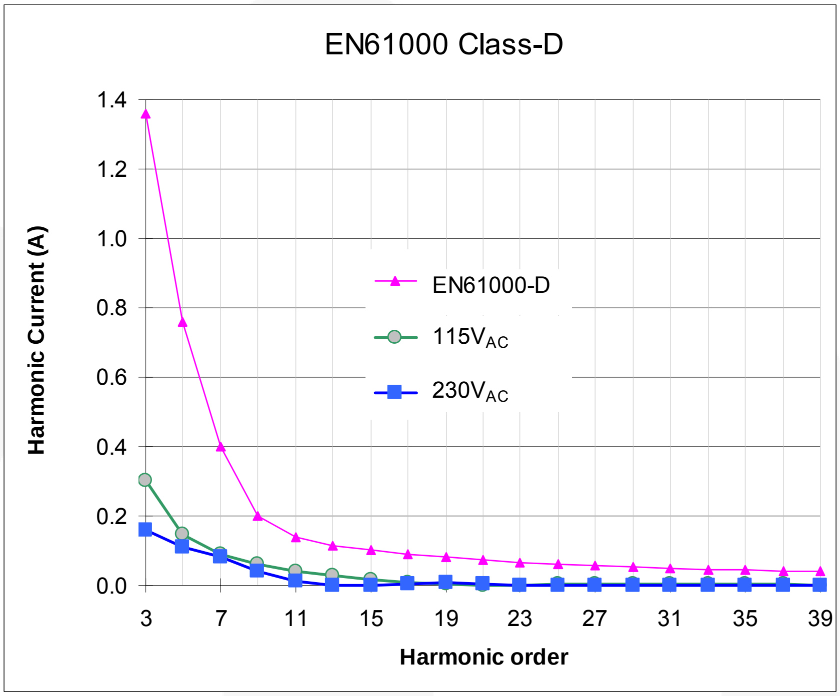


Figure 27. Measured Harmonic Current and EN61000 Class D Regulation

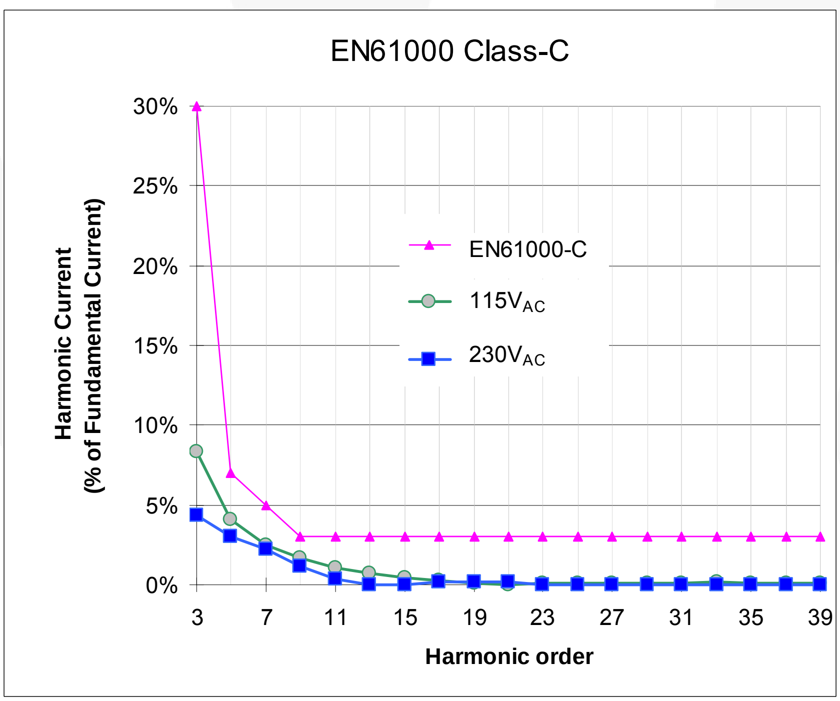


Figure 28. Measured Harmonic Current and EN61000 Class C Regulation

Figure 29 shows the measured power factors at input voltage of $115V_{AC}$ and $230V_{AC}$. As observed, high power factor above 0.98 is obtained from 100% to 50% load. Table 3 shows the total harmonic distortion at input voltages of $115V_{AC}$ and $230V_{AC}$.

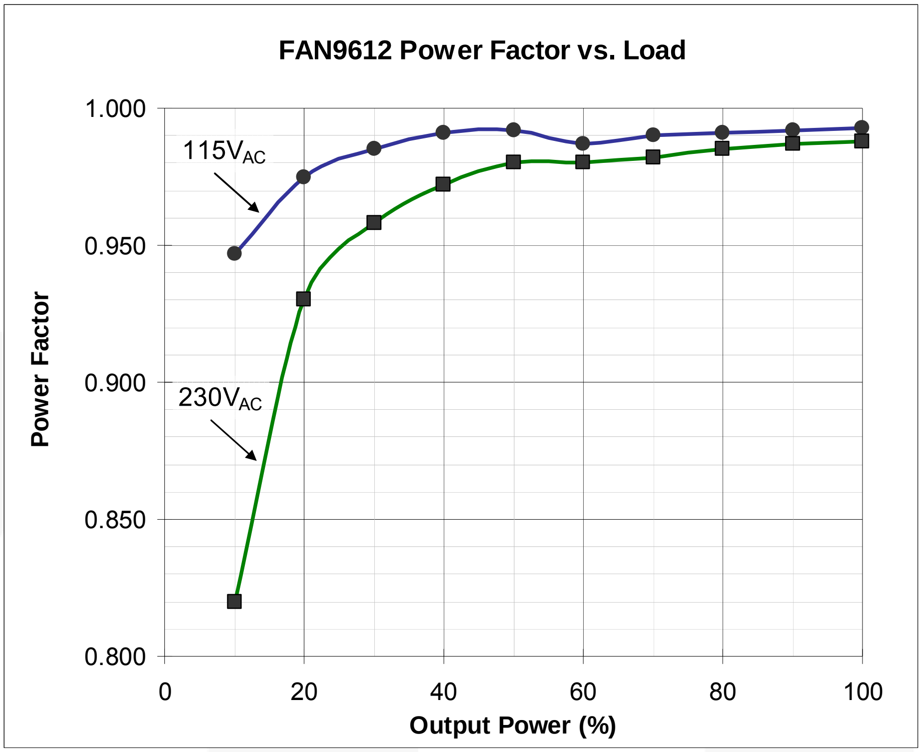


Figure 29. Measured Power Factor

Table 3. Total Harmonic Distortion (THD)

Line Voltage	100 % Load	75 % Load	50 % Load
$115V_{AC}$	9.9%	12.3%	16.35%
$230V_{AC}$	11.98%	13.82%	16.29%

10. References

FAN9611 / FAN9612 — Interleaved Dual BCM PFC Controller

AN-6086 — Design Consideration for interleaved Boundary Conduction Mode (BCM) PFC using FAN9612

11. Ordering Information

Orderable Part Number	Description
FEB279	FAN9611 / FAN9612 400W Evaluation Board

12. Revision History

Date	Rev. #	Description
Feb-20-2009	0.0.1	Initial release
Apr-07-2009	0.0.2	Schematic & BOM update
Apr-09-2009	0.0.3	Correction
March 2010	0.0.4	Correction in screen shot Warning & Diclaimer update
May 2010	0.0.5	Title change for clarity
June 2010	0.0.6	Updating to include FAN9611

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