AN-7536

FCS Fast Body Diode MOSFET for Phase-Shifted ZVS PWM Full Bridge DC/DC Converter

Sampat Shekhawat, Mark Rinehimer and Bob Brockway
Discrete Power Group, Fairchild Semiconductor

Introduction

Efficiency, power density, reliability, and cost are important for the switched mode power supply market. Attaining high transistor switching frequencies is important in reducing the size and cost of the power supply. However, the high transistor switching frequencies increase the total switching loss and lower the supply efficiency. Therefore, zero voltage or zero current switching topologies allow for high frequency switching while minimizing the switching loss. The ZVS topology operating at high frequency can improve the efficiency and reduce the size and cost of the power supply resulting in higher power densities. ZVS also reduces the stress on the semiconductor switch, which improves the converter reliability. The Phase-Shifted ZVS Full Bridge DC/DC Converter has become a very popular topology due to above advantages. The disadvantage of the phase-shifted bridge is that one of the legs loses the ZVS condition at light loads. Therefore, its switches enter a hard-switching condition and switching losses rise. Moreover, the power switch may lose gate control if the body diode is not designed sufficiently. The body diode of the switch conducts current so the diode reverse recovery characteristics are very important. The conventional power MOSFET body diode can cause device failure during switching due to left over minority carriers. The fast recovery body diode MOSFET (FRFET) introduced by Fairchild Semiconductor, will overcome the potential diode reverse recovery problem. This is accomplished by designing fast and robust body diode MOSFET. Following are the main applications of this Phase-Shifted ZVS PWM Full Bridge DC/DC Converter

- **Telecom power supply**
- **Main Frame Computer and server**
- **Welding**
- **Steel cutting**

The load generally stays non-fluctuating in nature for telecom and main frame computer but for welding and steel cutting industry it is highly fluctuating and demands good dynamic behavior of the power source. This power source should meet the following characteristics.

- Open circuit to short circuit operation (fast variations in load)
- Current controlled operation
- Rapid change of load current

Topology Description

A simplified schematic of phase shifted full-bridge zero-voltage switched (ZVS) pulse width modulated (PWM) converter operating in excess of 100 kHz is shown in figure 2. Figure 3 is provided to aid in the understanding of how ZVS is achieved. The conventional full-bridge topology is switched off under hard switching conditions where switch voltage stress is also high. The conventional full bridge topology has been modified in two ways to achieve ZVS.

First, modulation is done by phase shifting two overlapping constant frequency square waves by using leading-leg and lagging-leg.

Second, ZVS is achieved to minimize or reduce the switching losses.

The primary difference between this topology and the traditional full-bridge topology is switching method as shown in figure 1. In contrast to turning on the diagonally opposite switches of the bridge simultaneously (i.e. Q1 & Q4, Q2 & Q3), a phase shift is introduced between the switches in the left leg (leading-leg Q1 & Q2) and those in the right leg (lagging-leg Q3 & Q4) as shown in Figure 2 and Figure 3. The phase shift determines the operating duty cycle of the converter. The DC bus voltage is applied to transformer primary and power is transferred when two diagonal MOSFETs are on simultaneously. When two high side switches or two low side switches are on simultaneously (called freewheel state) the transformer primary is shorted. This results in zero voltage across primary and secondary. The transformer primary current rising edge slope as well as the falling edge slope reduces the duty cycle of the secondary voltage. This reduces the output voltage of the DC/DC converter so transformer turns ratio is effected and hence the secondary side power devices voltage. L1 and L2 affect this so their values should be selected properly and effect should be analyzed.

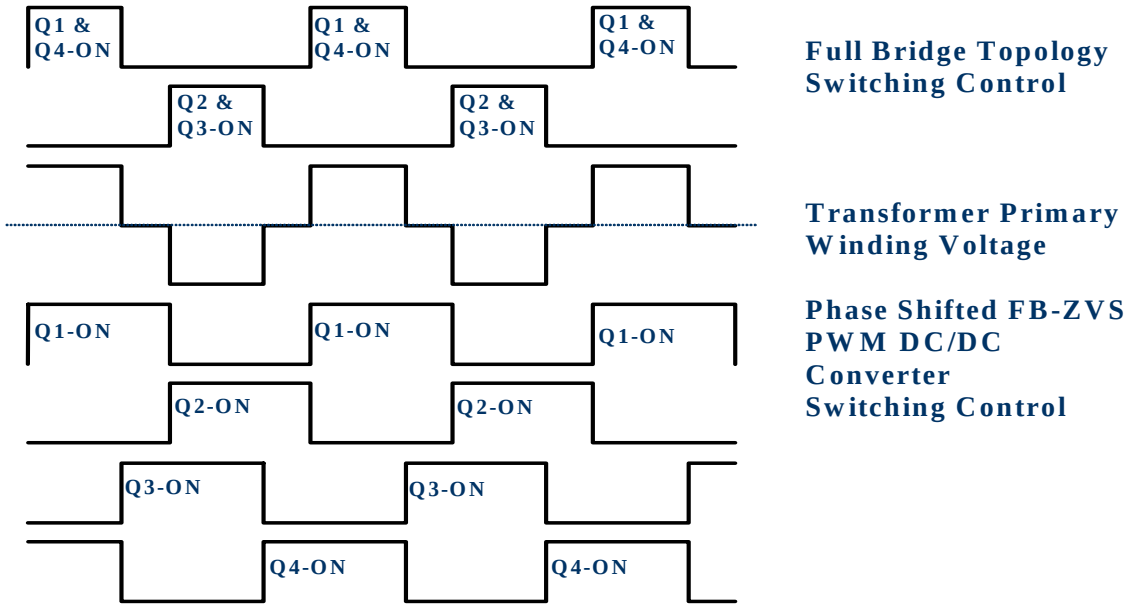

Figure 1. The difference between regular Full Bridge and PH-Full Bridge ZVS PWM DC/DC converter topologies control switching

ZVS process

Zero-voltage turn-on is achieved by using the energy stored in the leakage and series inductance of the transformer to discharge the output capacitance of the switches through resonant action. The resonance forces the body diode into forward conduction prior to gating on the switch. Two different mechanisms exist which provide ZVS [3] for the lagging-leg and leading-leg.

1) During light loads, very little energy is stored in the primary side inductance L1 (sum of the transformer leakage inductance and external inductance in series with the primary of the transformer). This causes the lagging-leg to turn on under a hard switching condition. As the load increases the energy stored in inductor L1 increases. This energy is used to charge the output capacitance of the devices that are turning off, and to discharge the output capacitance of the complementary device, thus forward biasing the free-wheeling diode. Full output capacitive discharge is necessary to cause the lagging-leg to start turning-on under the ZVS condition. The turn-off under the ZVS condition closely mimics that of resistive turn-off.

A switch with low output capacitance helps to achieve ZVS process at light load, improving the efficiency. Hard switching occurs when the output capacitance of the switch requires more energy than is available in the inductance L1 to fully charge and discharge the switches.

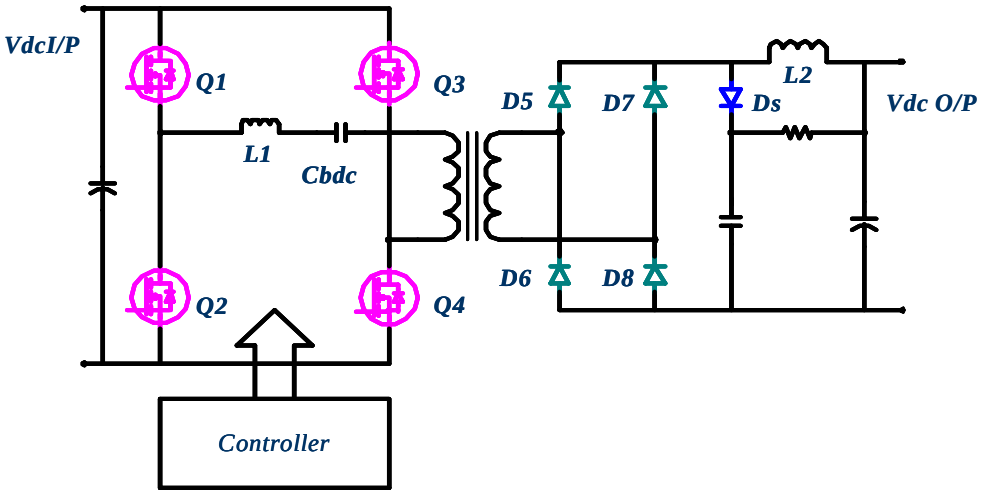

Figure 2. Phase shifted PWM full bridge ZVS DC/DC topology

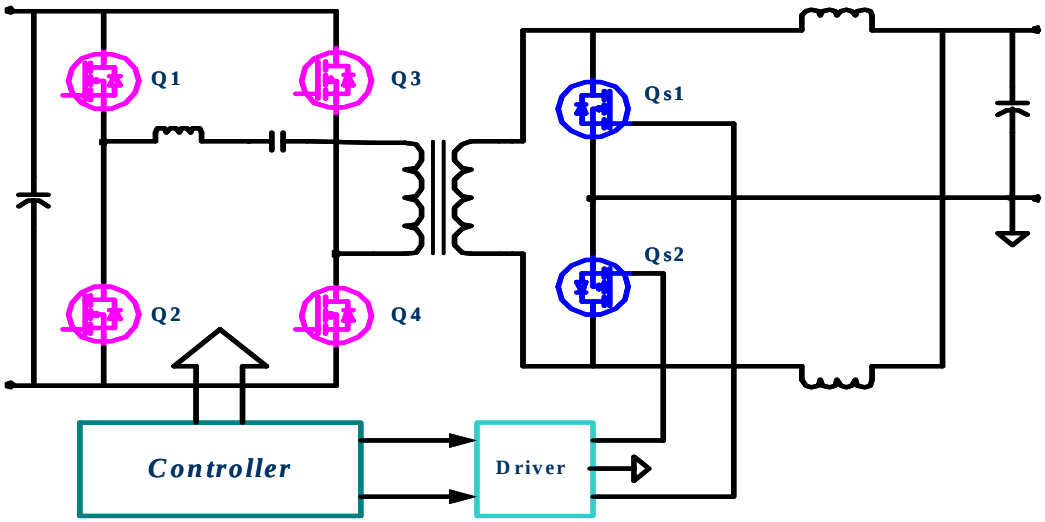

Figure 3 Phase shifted PWM full bridge ZVS DC/DC topology using synchronous MOSFETs for secondary side current doubler

To achieve soft turn-on and turn-off of the lagging leg, the following equation should be satisfied.

$0.5L1(Ip1)^2 > 0.5(Coe3+ Coe4)\ X\ (Vin)^2 + 0.5C_{TRW}\ X\ (Vin)^2$

Where: Coe3 & Coe4=Effective output capacitance of the power switches Q3 & Q4

Ip1 = Primary transformer current at turn-on and turn-off for Q3 and Q4.

C_{TRW} = Transformer winding capacitance

The lagging leg switch transition occurs due to resonance. The primary current during this transition is sinusoidal with peak amplitude occurring at the start. Coe and L1 form the resonant tank and its oscillating frequency is given as follows

$$\omega r = \frac{1}{\sqrt{L1 \times Coe}}$$

2) For the leading-leg switches (Q1& Q2), a different process provides the ZVS as explained below. Before Q1 turns off, the current in the primary reaches its peak value of the reflected filter inductor (L2) current. When Q1 is turned off, the energy available to charge the output capacitance of Q1 and to discharge the output capacitance of Q2 is the sum of the energy stored in the output filter inductor L2 and the primary side inductor L1. The energy stored in filter inductor L2 is available because the filter inductor current does not freewheel through the diode until the voltage across the secondary has fallen to zero. Accordingly, for soft turn-on and turn-off of the leading leg the following equation should satisfy.

$0.5\ (L2_p+L1) * (I_p)^2 > 0.5(C_{oe1}+C_{oe2}) * (V_{in})^2 + 0.5C_{TRW} * (V_{in})^2$

Where: Coe1 & Coe2 = Effective output capacitance of the power switches Q1 & Q2.

$$Coe = \frac{4}{3} xCoes$$

$L2_p$ is the output filter inductance referred to primary.

Since the stored energy in the output filter inductor is large when compared to that required to charge and discharge the output capacitances of the leg and capacitance of the transformer windings, **the switch capacitance is charged and discharged at a linear rate.** The resulting leading leg transition time in liner ramp is given as

Ip = Coe.dv/dt or dt = Coe.dv/Ip

Where as dv = Vdc input to the bridge and dt = Switch transition time

In this mode, even at lighter loads, much more stored energy is available to turn-on and turn-off the leading-leg switches than is available for the lagging-leg switches. Therefore, the body diode in the leading-leg, turn-on before the FRFET is gated on even at light loads. **Since the energy stored in output filter is so high that a small snubber capacitor can be put across leading leg switches and these devices can be turned off under real ZVS condition.** This will reduce the turn-off loss of these switches. The leading-leg free wheeling diode (FWD) conduction duty cycle is higher than lagging led diodes so leading-leg diodes will also dissipate a fair amount of power. The energy

stored available to turn-on lagging-leg the diode is very small so its conduction time is very small even at full load.

From figure 2 and figure 3 at t=t1 when Q1 is turned-on shortly after Q2 is turned -off the current free wheels through D1 and Q3. The primary current through Q3 (lagging-leg switch) decreases and when this switch turns-off at t=t2 the turn-off energy is much less for the switch Q3. The switch Q3 is turned-off by charging its output capacitance and discharging the output capacitance of Q4 due to energy stored in primary winding leakage inductance and its series inductance L1. The energy stored in the output filter inductor was freewheeling through the output rectifier diodes so the energy stored in the output filter inductor does not affect the lagging-leg switches. Once the output capacitance of the Q4 discharges D4 turns-on and then Q4 can be turned-on at ZVS. Secondary side rectifiers are free wheeling from t1 to t4 so output filter has no effect on primary side. From t2 to t3 the body diodes of Q1 and Q4 conduct and also their channel carry reverse (third quadrant) current. At t= t3 Q4 and Q1 channels start to carry current in forward direction. At t=t4 secondary side free wheeling ends.

At t=t5, when Q1 is turned-off, the energy stored in the output filter inductor L2 and primary side inductor L1 is available to charge Q1 output capacitance and discharge Q2 output capacitance.Since the filter inductor current freewheeling has not yet started, the energy stored in L2 is available. The output filter inductor value is high. So, even at light load, the energy stored in L2 is high enough to turn-on Q1 and turn-off Q2 and vice versa under a ZVS condition. Once the output capacitance of Q1 is charged and the output capacitance of Q2 is discharged, there is still enough energy available to forward bias the diode D2. Once D2 is on, the leading-leg switch can be gated-on. If the switch Q2 is now commanded to turn-on, the diode D2 continues to carry current for a long period of time due to the energy stored in L1 and output inductance L2.

In order to avoid shoot through and ensure that Q4 will turn-on with ZVS a dead time is needed between the turn-off of Q3 and turn-on of Q4 and also make sure that diode D4 has started conducting. The resonance between L1, Coe and C_{TRW} provides sinusoidal voltage across Q3 and D3 and this voltage peaks at one fourth of the resonant period

$$\tau_{Peak} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L1xC}$$

Where as C = Coe + C_{TRW}

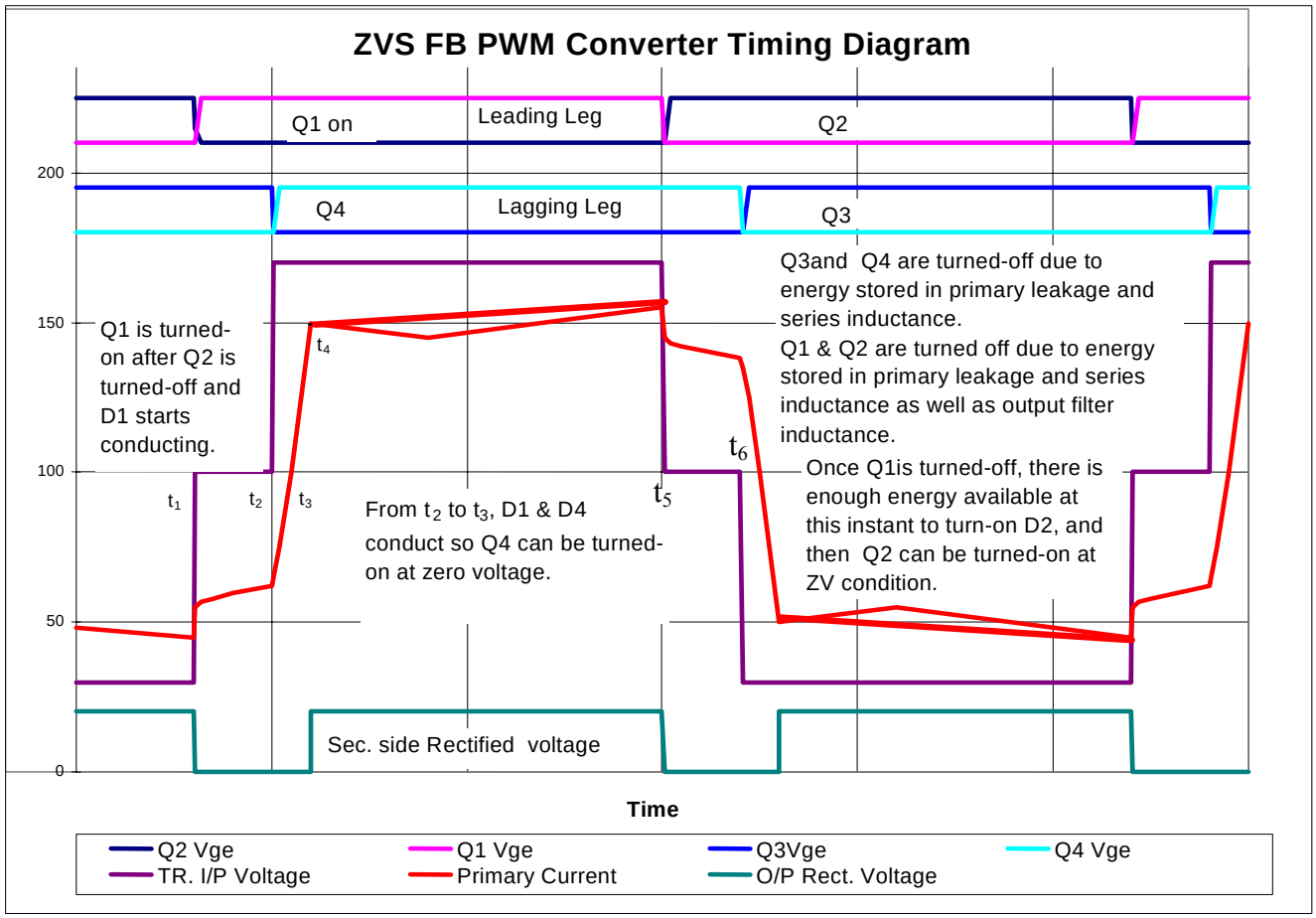

Figure 4. ZVS Waveforms

The energy stored in L1 increases by a square law as load current increases. Therefore, the stored energy in L1 increases rapidly at loads higher than the minimum load required for ZVS. The large amount of available charging energy causes the switch drain-source voltage to rise and fall at a linear rate. Under the ideal condition, the primary current will split between the on-coming and out-going switch. This condition will produce the corresponding dv/dt as given by:

$$\frac{dv}{dt} = \frac{Ip}{2Coe}$$

The turn-off current through MOSFET has three components as follows:

1. $I_{Co} = C_{oe}\frac{dv}{dt}$, Current flowing through output capacitance

2. $I_{Cf} = C_{fe}\frac{dv}{dt}$, Current flowing through Miller capacitance.

3. $I_{CHANNEL} = Ip - I_{Co} - I_{Cf}$, Current flowing through MOSFET channel.

$$I_g = C_{afe}\frac{dv}{dt} \quad \text{or} \quad \frac{dv}{dt} = \frac{Ig}{C_{fe}}$$

The current flow through power MOSFETs and gate resistance dissipates real loss during turn-off. The turn-off loss increases with load current. In order to achieve real ZVS turn-off one has to put snubber capacitor across power MOSFETs or IGBTs. For lagging-leg it will be harmful at turn-on, since the part of this capacitor stored energy will be dissipated back in the power switch especially at light loads.

The MOSFET body diode conducts after the discharge of its output capacitance. The MOSFET is turned on after a dead time equal to T_{Peak} (one fourth of resonant period). Once the MOSFET is turned on its channel conducts reverse current in parallel with body diode and should satisfy the following equation.

$$V_N + I_D R_D = R_C(IPO - I_D)$$

Importance of free wheeling diode for this topology:

The MOSFET body diode must not be taken lightly in the ZVS topology. Even with the reduced switching stress on the MOSFET, failure may occur because of a poor diode recovery. The failures have been reported [1, 2] at no or light load conditions. These failures result from the lagging-leg losing ZVS at turn-on and turn-off forcing a hard switching condition**.**

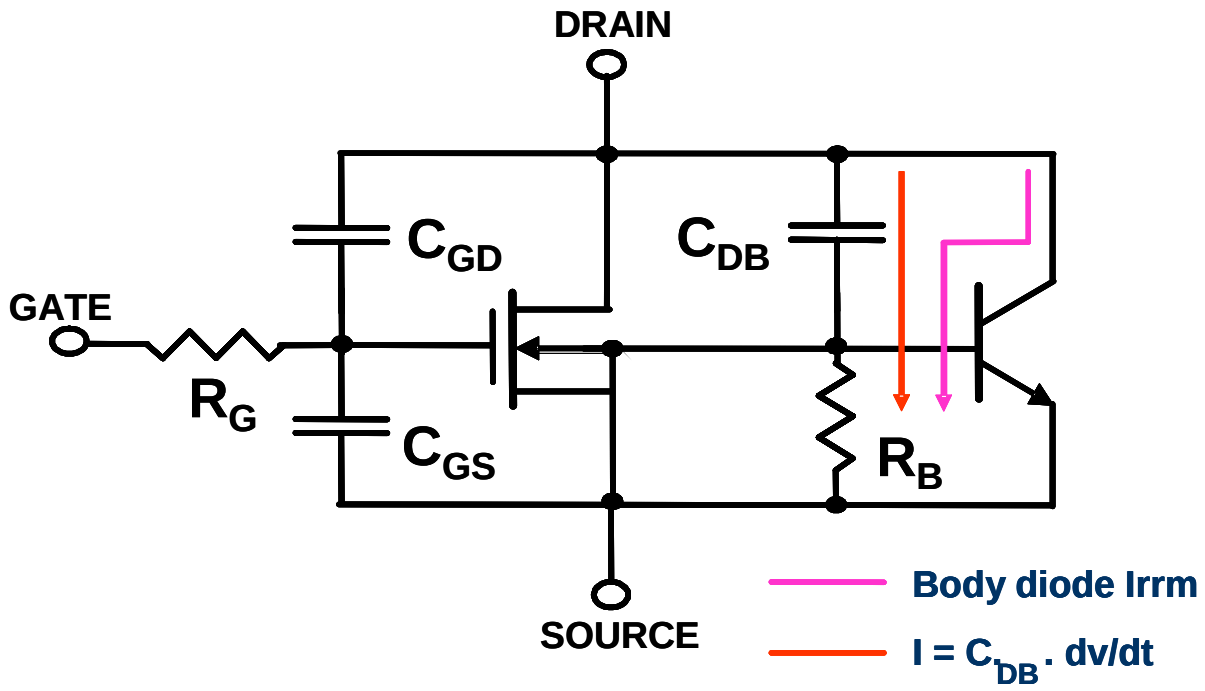

Figure5. MOSFET Equivalent Circuit

One potential failure mechanism is due the $C_{GD}dV_{DS}/dt$ current. The resulting C_{GD}*dV_{DS}/dt current can cause VGS to charge above VTH (re-applied dV_{DS}/dt). A shoot through condition will exist where both of the MOSFETs in the lagging-leg can turn-on and cause the leg to fail.

In a ZVS topology, the intrinsic body diode of the MOSFET is forced to conduct current before the channel of the device is turned on (Figure 6A). As current flows through the body diode, minority carriers are generated in both the N- epi and P body regions of the device (Figure 7A). When the gate of the MOSFET is turned on, a portion of the total current is diverted in the third-quadrant mode through the series path including the MOS channel, the parasitic JFET, and the drift region resistance. In this mode, source-to-drain conduction occurs through both the body diode and the associated channel regions of the device (Figure 6B). The addition of this parallel current path begins to reduce injection of minority carries into the N- region of the body diode.

As the current in the primary transformer changes direction (ex.: t=t3 in Figure 4), current flowing through the associated channel regions also changes direction to a first-quadrant mode of conduction. This forces a small amount of reverse current in the body diode (Figure 6C), the small magnitude of the current being proportional to the low reverse voltage across the body diode. Since the injecting P body / N- junction is in parallel with the low resistance channel regions, the effective reverse voltage across the diode is only on the order of 2-5V. This results in minimal removal of minority carriers from the heavily modulated N- region of the diode structure. In the absence of sufficient voltage to force significant carrier removal, only a relatively small reduction in minority carrier concentration due to lifetime-controlled recombination mechanisms occurs (Figure 6D).

When the MOSFET is turned off (ex.: t=t5 in Figure 4), the high reverse voltage results in the rapid removal of excess carries as the drift region begins to support the applied bias. Minority carries in the drift region at this time are swept across the P body / N- junction (Figure 6E). This rapid depletion results in a significant current density flowing through the P body region, a portion of which extends beneath the source of the MOSFET structure. The resistance of P doped region directly beneath the source of a conventional MOSFET structure is represented as Rb in Figure 7. If the magnitude of the current passing through Rb is sufficiently large to cause injection across the P-body / N+ source junction, the parasitic bipolar transistor may become active. This uncontrolled state of operation usually results in the destruction of the device.

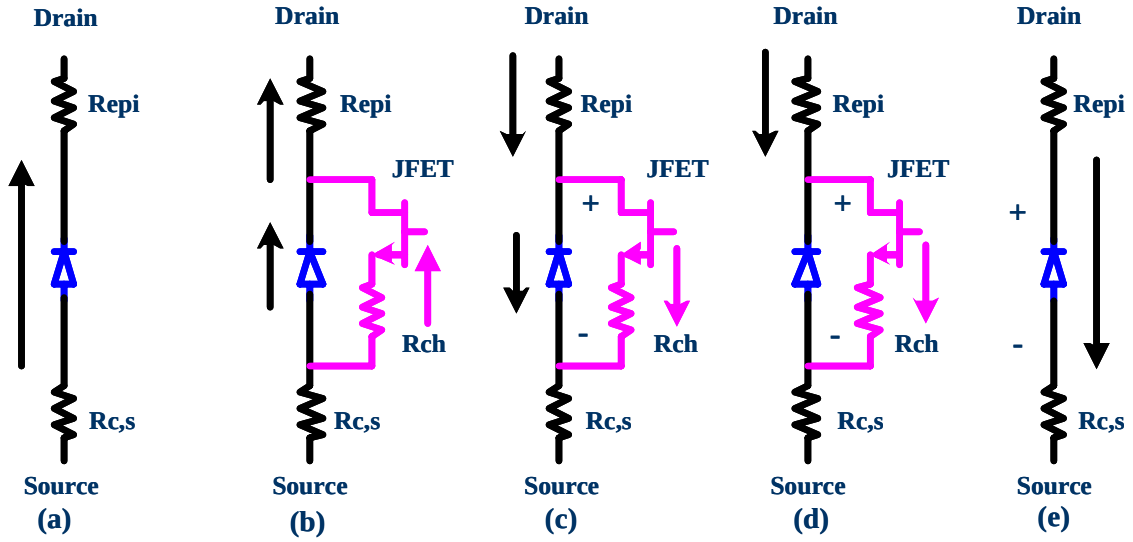

Figure6. (a) Forward current through body diode, (b) Forward current through body diode & JFET & channel, (c) Reverse current through body diode and forward current through JFET & channel, (d) Forward current through JFET & channel and (e) Reverse current through body diode

If the applied dv/dt is also high then an additional current also flows through this Rb due to $C_{DB}dv/dt$ and the turn-on chances of intrinsic bipolar transistor are more.

Advantages of this topology

1.Reduced heat sink size

2.ZVS switching so switching loss is reduces

3.Reduced EMI

4.Reduced switch (MOSFET or IGBT) stress compared to quzi-resonant topologies

5.Fixed frequency control & fixed duty factor

FRFET for ZVS Topology

The reliability problems of the PS-PWM-FB-ZVS topology have been documented. The problems can also be over-come by using the FRFET series MOSFET. The C_{GD}*dV_{DS}/dt immunity of these MOSFETs is increased by reducing Q_{GD}, the Q_{GD}/Q_{GS} ratio, and the internal gate resistance (ESR) and increasing $V_{GS(TH)}$. A MOSFET used for this topology should also have a fast intrinsic body diode. The diode should have a low Qrr, Irrm and Trr to overcome the problem discussed above.

The Qrr and Trr of the body diode should be low enough to provide complete minority carrier removal before the device turns-off. If this does not occur, the turn-off dV_{DS}/dt of this device could turn-on the parasitic NPN transistor and forcing the transistor into secondary breakdown. The possibility of this failure occurring increases as the frequency is increased. The intrinsic body diode of the FRFET MOSFET has been improved by reducing the Qrr and Trr as shown in Figure 7. The Trr of the FRFET MOSFET has been reduced to 20%, Irrm has been reduced to 38% and Qrr has been reduced to about 15%.

Following are the switch requirements for this topology

- Low body diode Q_{RR} and T_{RR}
- Low Q_{GD}
- Low Q_{GD} to Q_{GS} ratio
- Low Coss
- High Threshold (V_{TH}) voltage
- Low conduction losses
- Low internal gate ESR
- Low output capacitance

Test Conditions: Vr = 20V, If = 10A, di/dt = 160A/usec & TJ = 25°C

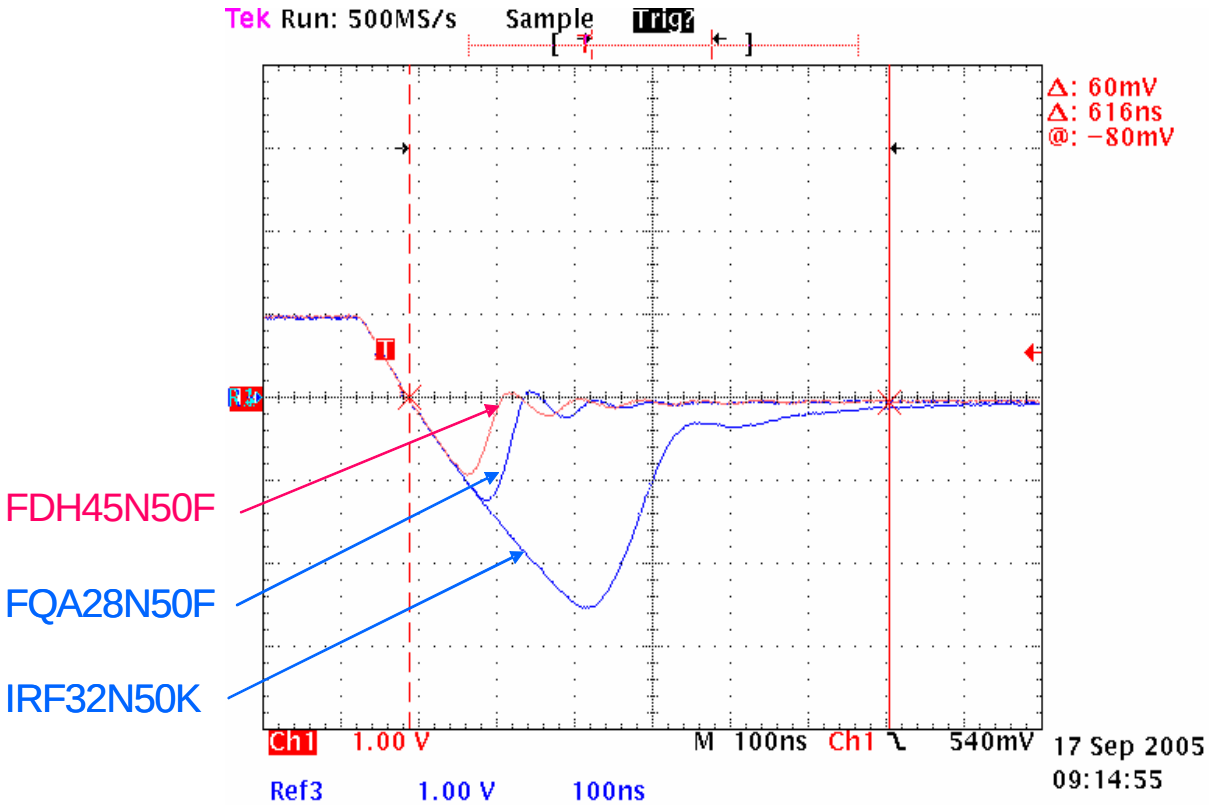

Figure 7. Reverse Recovery Waveforms

Selection of switching frequency L1, L2 and duty cycle for regulation:

The transformer primary current rising edge slope as well as the falling edge slope reduces the duty cycle of the secondary voltage. This reduces the output voltage of the DC/DC converter. L1 and L2 affect this so their values should be selected properly and effect should be analyzed.

The slope of primary current from t_1 to t_2 is given by :

$$Slope = \frac{Vo}{L2}$$

The slope of primary current from t_2 to t_4 is given by :

$$Slope = \frac{Vi}{L1}$$

The slope of primary current from t_4 to t_5 is given by :

$$Slope = \frac{Vi - Vo}{L1 + L2}$$

$$\frac{Vo}{Vin} = \frac{Ns}{Np} * Ds$$

Where as Ds is the duty cycle of secondary voltage

Transformer primary side voltage duty cycle D is set by the controller and is given by following equation.
D = Ds + Dl

Where as Dl is loss of the duty cycle due to rising and falling edges slopes of the primary current

$$D = \frac{1 + \frac{4L1^* fs}{Rp} - \frac{L1}{L2p}}{\frac{1}{Ds} - \frac{L1}{L2p}}$$

Where as Rp = R1($^{Np}/_{Ns}$)^2 and L2p = L2($^{Np}/_{Ns}$)^2

$$Ds = \frac{D}{1 + \frac{4L1\,fs}{Rp} - \frac{L1}{L2p}(1 - D)}$$

, the term $\frac{L1}{L2p}(1 - D)$ can be neglected and then we have

$$Ds = \frac{D}{1 + \frac{4L1\,fs}{Rp}}$$

These equations can be used to design the transformer and values of L1 and L2.

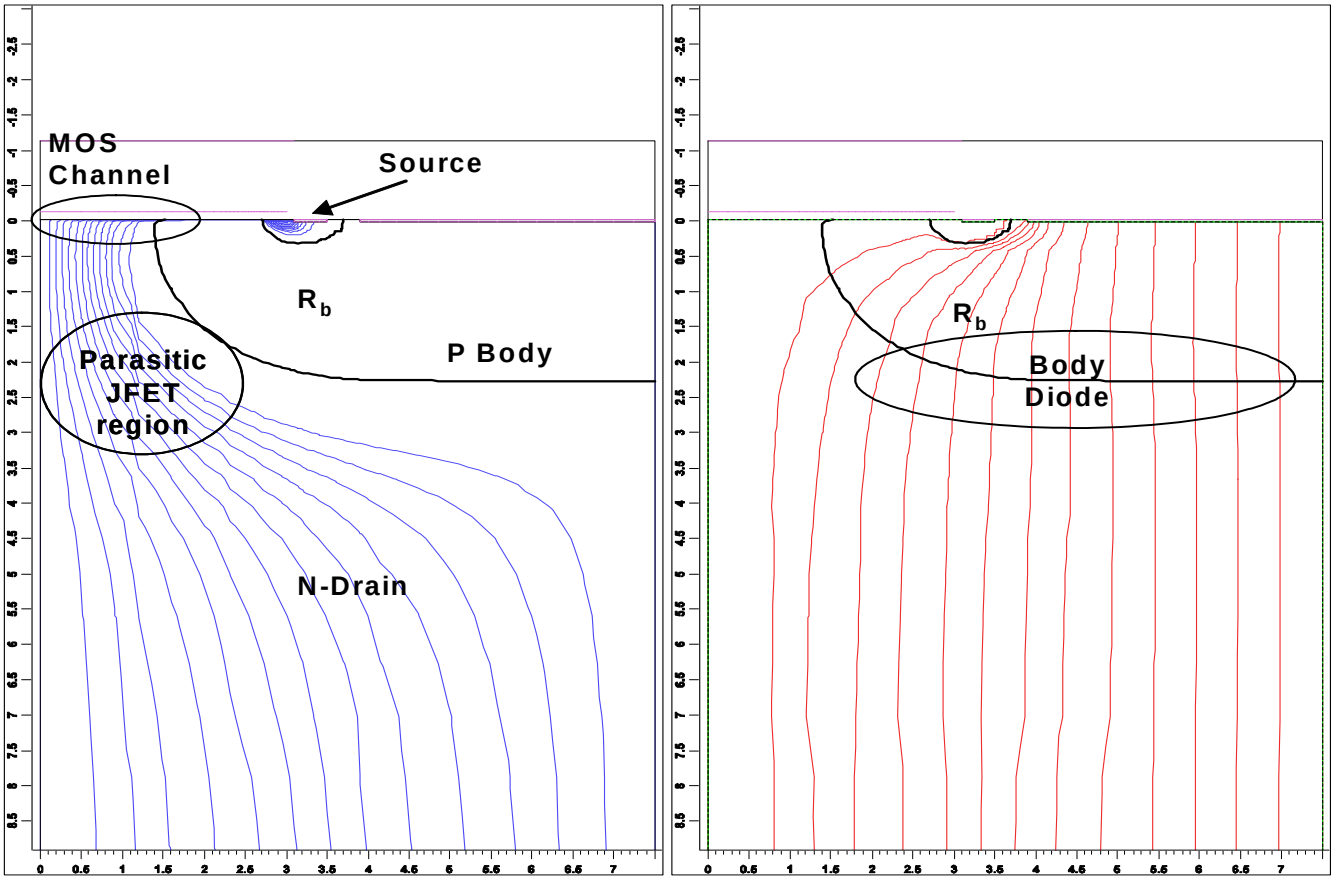

Figure 7(a) Conduction of current through MOS channel, series JFET & drift regions
Figure 7(b) Conduction of current through integrated body diode

[1] H. Aigner, et al., “Improving the Full-Bridge Phase –shift ZVT Converter for Failure-free Operation under Extreme Conditions in Welding and Similar Applications” IEEE proceedings of IAS Society Annual Meeting, St. Louis, 1998.

[2] L. Saro, et al., “High-Voltage MOSFET Behavior in Soft-Switching Converter: Analysis and Reliability Improvements,” International Tel-communication Conference, San Francisco, 1998.

[3] J. A. Sabate, et al., “Design considerations for high-voltage high power full-bridge zero-voltage-switched PWM converter,” in Proc. IEEE APEC, 1990, pp. 275-284

[4] K. Shenai, et al., “Soft-Switched, Phase-Shifted Topology Cuts MOSFET Switching Stress in FBCs,” PCIM Magazine, May 2001.