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FSTU - Undershoot Protected Fairchild Switch Family

Introduction

Fairchild Switch (FST) Bus Switch products have become powerful tools in the modern personal computer as well as increasing in popularity in telecommunications and data communications applications. The Fairchild Switch Family has a number of positive attributes over the standard bus transceivers. FST parts introduce virtually no propagation delay into the line, consume a negligible amount of power, and introduce none of the noise issues associated with the typical high-drive bus transceiver. In most applications, use of FST Bus Switches will alleviate the problems of the bus transceiver without creating new ones.

In the presence of large amounts of system signal undershoot voltage on I/O ports, the typical NMOS bus switch can malfunction. Usually concern with undershoot voltages pertains to latch-up. This is not a concern with FST products. FST Bus Switches have been characterized for latch-up and exceed the 500 mA upper limit of the latch-up tester. The real issue is the potential coupling of data from input to output when the switch device is intended to be disabled (OPEN).

This application note will describe how undershoot can cause data corruption, various methods for undershoot hardening (protection), and proprietary Undershoot Hardening Circuit (UHC®) design that is now available in Fairchild's FSTU Undershoot Hardened Bus Switches.

The Undershoot Condition

In the application of Figure 1, the bus switch is used to isolate data on Bus A from the data on Bus B. When the pin from $\overline{OE}$ is HIGH, Bus B is expected to be isolated with any activity that occurs on the Bus A.

Undershoot conditions can occur on busses that are poorly terminated, on signals with very fast edge rates, or on busses that allow hot-swapping. The first solution to undershoot events is to ensure proper termination of transmission lines. Some systems are designed to be reflective-wave and therefore rely on the impedance mismatch to increase signal levels at the receiver. The PCI Bus is an example of an intentionally reflective-wave bus. It is reflected-wave architecture that minimizes the amount of drive required for PCI devices. Yet these reflections can also cause undershoot conditions.

Another potential source of undershoot are the early voltages present during the hot-swapping of boards in applications such as servers and telecommunications systems. Changes are continuing to be made to hot-swap sequencing and electrical requirements within standards specifications such as CompactPCI®. These changes make it even more critical to ensure that bus switches do not malfunction under such conditions.

For the example in Figure 1, assume that $\overline{OE}$ is a HIGH and Bus A is switching as data is written from one device to another. If Bus A transitions from a 0V to 5V, and is poorly terminated, the end of the bus will try to double to 2 * 5V. This positive excursion, while poor for the system, will not affect the NMOS bus switch. A LOW-going transition, however, is a different story. In the LOW-going transition case, 5V to 0V, the voltage swing will attempt to double to –5V. This undershoot may cause problems with standard NMOS bus switch devices. Although on standard bus switch devices, there exists a P-N diode on the input of the bus switch that will clamp the undershoot voltage to approximately –650 mV, by then data corruption on the bus may have already occurred.
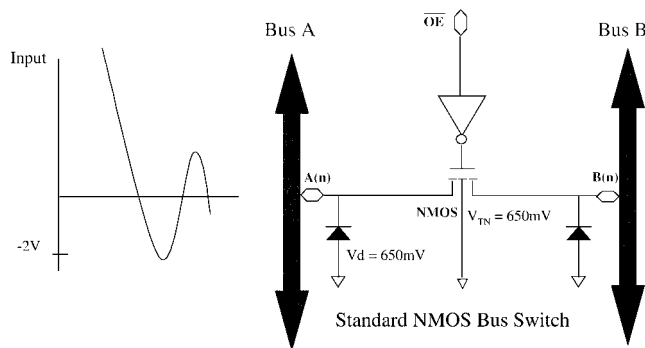

FIGURE 1. Typical Bus Switch Application

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Undershoot Physics

For most functions found in Fairchild's Logic Products databooks, a path from input to output exists where the signal must propagate through any number of inverters or complex logic gates. The bus switch is special in that its path is exceedingly simple. The data passes through a simple, but large, NMOS pass transistor. In addition to this NMOS transistor, there exists a parasitic NPN bipolar transistor (with a beta of approximately 10 on today's processes) created by the N-type source region (emitter), P-type substrate region (base), and the N-type drain region (collector) (see Figure 2).

When $\overline{OE}$ is HIGH, the gate of the NMOS transistor is at 0V and the switch is OPEN or OFF. An undershoot condition actually creates two phenomena that could turn these transistors back ON, creating potential data corruption on the isolated bus.
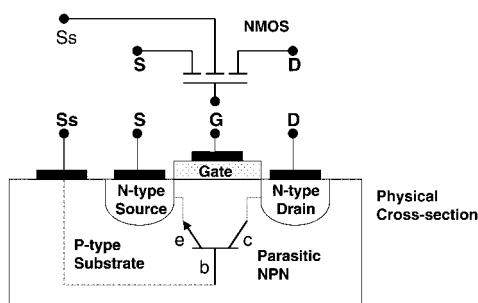

FIGURE 2. Characterization of an NMOS Switch

The first phenomenon occurs when the switching bus undershoots ground and the source node voltage of the NMOS transistor becomes lower than that of the gate. The NMOS threshold voltage, V_{TN}, for a typical CMOS process is approximately 650 mV. Thus any undershoot on the source node greater than or equal to 650 mV will create a positive V_{GS}, and enable the bus switch to activate and pass a LOW to Bus B and data corruption would be likely. Varying the clamp diode on this node to clamp undershoot voltage to something less than a V_{TN} could prevent this phenomenon from occurring.

The second phenomenon occurs when the source node of the bus switch is pulled below ground by an undershoot event and enough current exists on the substrate-to-source path that a positive VBE on the parasitic NPN bipolar transistor will occur. The NPN will conduct current from the drain to the source also placing a LOW on Bus B and data corruption is again likely. With a beta of approximately 10, it does not take much base current on the NPN to create a great deal of current flow from collector to emitter.

The important thing to note is that regardless of the type of clamping used to prevent the NMOS from turning ON, the parasitic phenomenon will still cause severe leakage to Bus B and could still cause data corruption.

Possible Undershoot Hardening Solutions

This applications note discusses four possible solutions to undershoot protection or "hardening".

Schottky Clamp Diode Solution

The Schottky Clamp hardening solution illustrated in Figure 3 utilizes the lower clamping voltage of a Schottky diode to clamp the input undershoot to approximately 350mV thus preventing the NMOS from achieving a 650mV V_{TN} and turning ON.
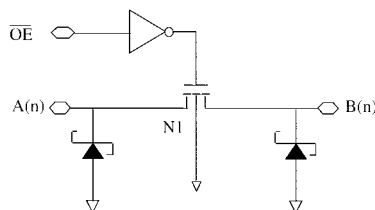

FIGURE 3. Schottky Clamp Solution

The advantages of the Schottky Diode solution are its low power and that it clamps slower edges preventing the NMOS from turning ON. One disadvantage is that these diodes are usually very large and dramatically increases die size of the bus switch. The biggest disadvantage is this is not a fail-safe solution for two reasons. The first is that diodes take time to react and the larger the energy that hits the diode, the more difficult it will be for the diode to react in time to clamp the undershoot event before the NMOS turns ON. The second, and most important reason why this is not a fail-safe solution is that it does nothing to prevent the parasitic NPN from turning ON. As a result the device will still cause large leakage currents (10 mA to 15 mA) on the output that will load down the isolated bus and potentially cause data errors.
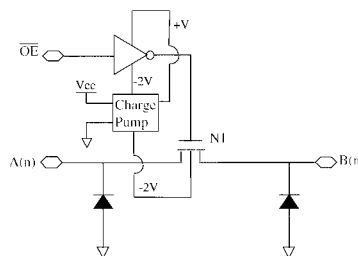
Charge Pump Solution

FIGURE 4. Charge Pump Solution

Figure 4 illustrates a charge pump solution that "pumps up" the voltage to the enable buffer (usually +7V) and "pumps down" the gate and substrate voltage to the same negative voltage (usually –2V). This charge pump condition is ON all of the time and in an undershoot event it prevents the NMOS from turning ON with undershoot voltages less than -2V.

The advantage of the charge pump solution is that it does prevent the NMOS from turning ON in most undershoot conditions. Rarely does an undershoot voltage exceed –2V. There are two disadvantages to this solution. The first

Possible Undershoot Hardening Solutions (Continued)

being that this is not a truly fail-safe solution. Although rare, undershoot voltages greater than −2V can cause the NMOS to turn ON, causing data corruption. The most important disadvantage is that the charge pump attempts to solve the problem at the expense of power. Quiescent I_{CC}, and therefore power, for these charge pump devices increase 100-fold over standard non-charge pump solutions, from 3uA to 3mA. On lower power applications this can become a burdensome issue.
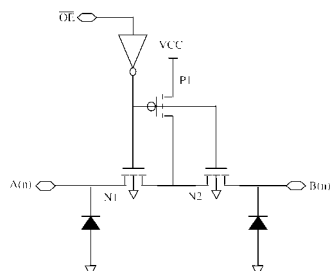
Series NMOS Solution

FIGURE 5. Series NMOS Solution

Figure 5 illustrates a Series NMOS hardening solution. In this solution, when $\overline{OE}$ is HIGH, both the NMOS transistors N1 and N2 are OFF and the PMOS transistor P1 is ON. The intermediate point between the N1 and N2 is actively pulled to V_{CC} by P1. When undershoot is present on the input, the NMOS on the side of the undershoot voltage may turn ON. However, P1 will hold the intermediate point high enough to prevent the second NMOS from turning ON by keeping $V_{GS} < V_{TN}$.

The advantage to this solution is that it is fail-safe. Although the first NMOS may turn ON in an undershoot event, it is extremely unlikely that the intermediate point will get pulled down from V_{CC} to below ground in such an event.

One disadvantage to this solution is that an undershoot condition will drain I_{CC} through P1 and N1 causing a momentary increase in power consumption. The major disadvantage is a doubling in R_{ON} from using two MOSFETs in series, and a marginal increase in enable and disable times due to the increased capacitive load on the $\overline{OE}$ inverter.

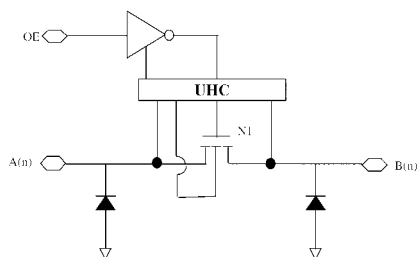### FSTU Undershoot Hardening Circuit (UHC)

FIGURE 6. Fairchild's Pfcdf]YHUfmUHC Solution

Figure 6 illustrates Fairchild's new (proprietary) Undershoot Hardening Circuit (UHC). In an undershoot event, the primary causes of both the NMOS turning ON, and the parasitic NPN turning ON is primarily the difference in potentials between the gate and the source of the NMOS and the base (NMOS substrate) and emitter (NMOS source) of the NPN, respectively. The most effective and fail-safe solution is to prevent such a difference in potentials without the use of power hungry charge pumps. The UHC solution involves sense circuitry that compares the voltages of both ports of the NMOS switch with regard to ground when $\overline{OE}$ is HIGH.

Figure 7 illustrates the effectiveness of this circuit in the new FSTU6800 versus the Schottky Diode clamp solution of a competing 3384 and a standard 6800. For this test a valid logic "1" on Bus B was represented by charging a load capacitor on the B-side of the bus switch to 3.3V. Figure 8 illustrates the test set-up used. The bus switch was then disabled and the input was hit with an undershoot condition. The voltage level of the capacitor was observed to see if data corruption did occur.
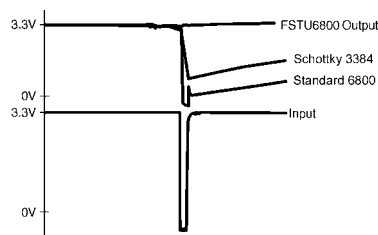

FIGURE 7. Undershoot Hardening Effectiveness of the FSTU Family

The data shows that a standard, non-hardened bus switch, represented here by a standard 6800, will turn ON quickly and discharge the capacitor. A Schottky Diode solution, represented here by a competitors 3384, turns ON through the more resistive parasitic NPN. Although the discharge is slower than the non-hardened switch, the capacitor discharges just the same indicating potential for data corruption on B-side. The UHC hardened FSTU6800 never turns ON, maintaining data integrity on the B-side throughout the entire undershoot event.
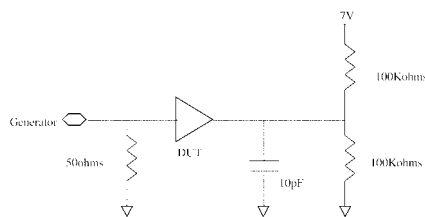

FIGURE 8. Set-up for Undershoot Test

Conclusion

While good transmission line design techniques may alleviate most undershoot events, systems that intentionally use reflective-wave and/or hot-swap architectures (such as servers using CompactPCI) are likely to experience undershoot conditions. In the case of an undershoot condition, standard NMOS bus switches are apt to malfunction, potentially causing data errors on busses intended to be isolated.

If your system demands the higher performance and you wish the highest level of noise immunity possible, there are several possible solutions to undershoot hardening. Although most of the solutions address some of the signal integrity concerns, only one solution, Fairchild's (proprietary) FSTU family of undershoot hardened bus switches, implement a truly fail-safe solution without any of the negative side-effects such as increased power consumption, increased R_{ON}, or enable/disable times.

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