



November 1993
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74ABT16952

16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ABT16952 is a 16-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

Features

- Separate clock, clock enable and 3-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT16952CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16952CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

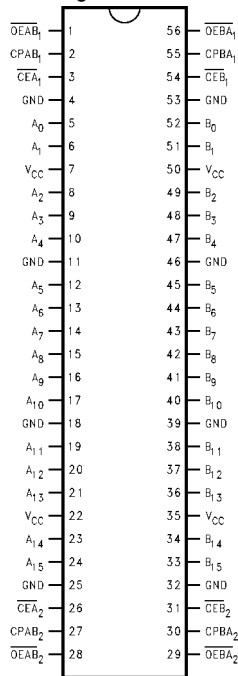
Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

Pin Descriptions

Pin Names	Description
A ₀ –A ₁₅	Data Register A Inputs/ B-Register 3-STATE Outputs
B ₀ –B ₁₅	Data Register B Inputs/ A-Register 3-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
CEA _n , CEB _n	Clock Enable
OEAB _n , OEBA _n	Output Enable Inputs

Connection Diagram

Pin Assignment for SSOP



Output Control

OE	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Register Function Table

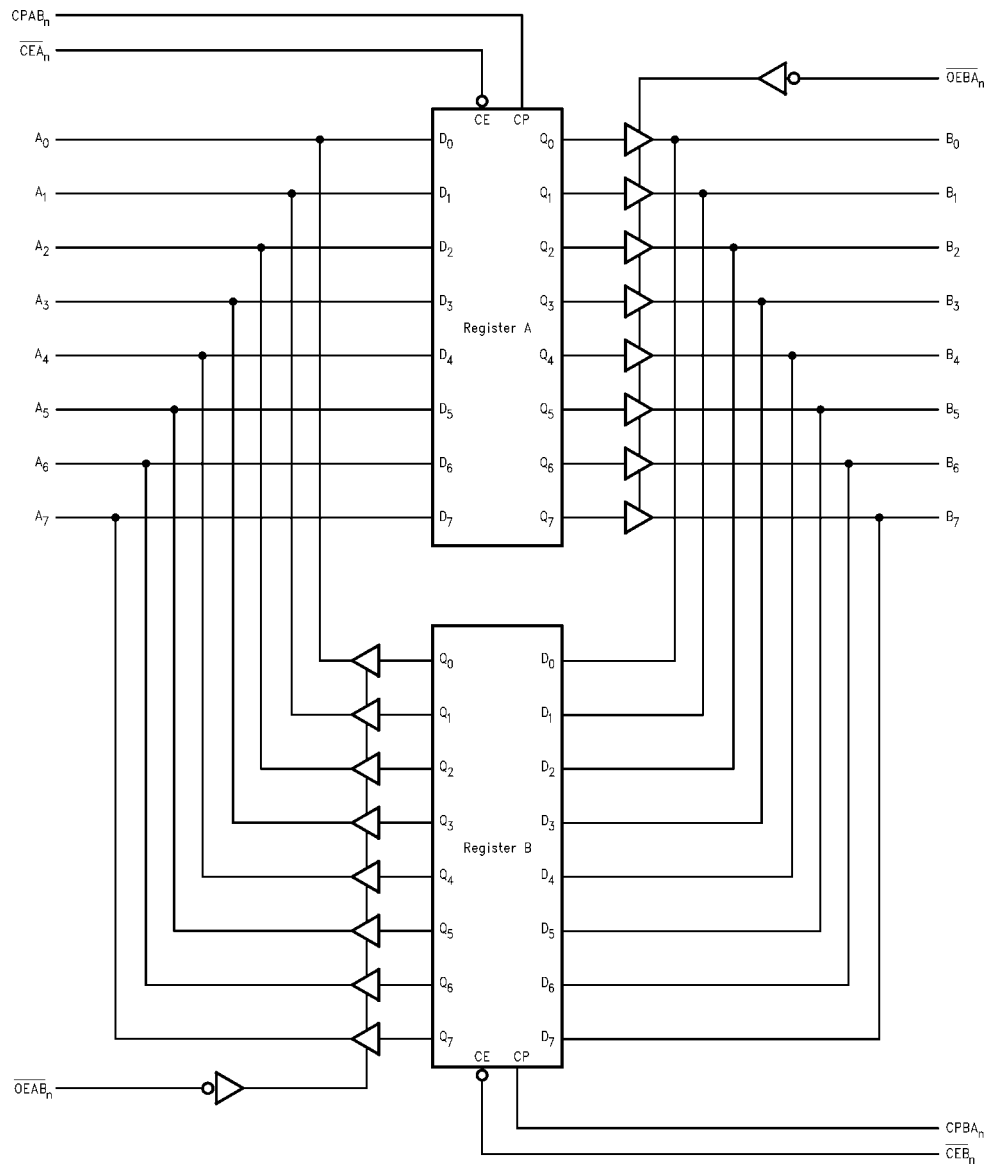
(Applies to A or B Register)

Inputs			Internal	Function
D	CP	CE	Q	
X	X	H	NC	Hold Data
L	↘	L	L	Load Data
H	↘	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↘ = LOW-to-HIGH Transition
NC = No Change

74ABT16952 16-Bit Registered Transceiver with 3-STATE Outputs

Block Diagram



n for either byte 1 or byte 2

Absolute Maximum Ratings (Note 1)		DC Latchup Source Current		–500 mA			
Storage Temperature	–65°C to +150°C	Over Voltage Latchup (I/O)		10V			
Ambient Temperature under Bias	–55°C to +125°C	Recommended Operating Conditions					
Junction Temperature under Bias	–55°C to +150°C						
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V	Free Air Ambient Temperature	–40°C to +85°C				
Input Voltage (Note 2)	–0.5V to +7.0V	Supply Voltage	+4.5V to +5.5V				
Input Current (Note 2)	–30 mA to +5.0 mA	Minimum Input Edge Rate (ΔV/Δt)					
Voltage Applied to Any Output in the Disable or Power-Off State	–0.5V to +5.5V	Data Input	50 mV/ns				
in the HIGH State	–0.5V to V _{CC}	Enable Input	20 mV/ns				
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)	Clock Input	100 mV/ns				
		Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.					
		Note 2: Either voltage limit or current limit is sufficient to protect inputs.					
DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	2.5					I _{OH} = –3 mA (A _n , B _n) I _{OH} = –32 mA (A _n , B _n)
V _{OL}	Output LOW Voltage			0.55			I _{OL} = 64 mA (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current			1	μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 4) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			–1	μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 4) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			10	μA	0V–5.5V	V _{OUT} = 2.7V (A _n , B _n); OE _A or OE _B = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current			–10	μA	0V–5.5V	V _{OUT} = 0.5V (A _n , B _n); OE _A or OE _B = 2.0V
I _{OS}	Output Short-Circuit Current	–100		–275	mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μA	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE; All Others GND
I _{CCT}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} – 2.1V; All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 4)	No Load		0.18	mA/MHz	Max	Outputs Open OE _A or OE _B = GND, Non-I/O = GND or V _{CC} One Bit toggling, 50% duty cycle (Note 3)
Note 3: For 8-bit toggling, I _{CCD} <1.4 mA/MHz.							
Note 4: Guaranteed, but not tested.							

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Max	Min	Max	
f _{max}	Max Clock Frequency	200		200		MHz
t _{PLH} t _{PHL}	Propagation Delay CPAB _n or CPBA _n to A _n or B _n	1.5	5.3	1.5	5.3	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OEAB}}_n$ or $\overline{\text{OEBA}}_n$ to A _n or B _n	1.5	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OEAB}}_n$ or $\overline{\text{OEBA}}_n$ to A _n or B _n	1.5	6.0	1.5	6.0	ns

AC Operating Requirements

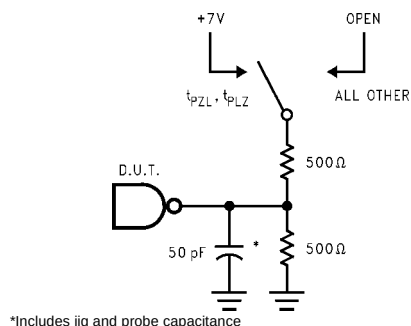
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Max	Min	Max	
t _S (H) t _S (L)	Setup Time, HIGH or LOW A _n or B _n to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	2.5		2.5		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW A _n or B _n to CPAB _n or CPBA _n	1.5		1.5		ns
t _S (H) t _S (L)	Setup Time, HIGH or LOW $\overline{\text{CEA}}_n$ or $\overline{\text{CEB}}_n$ to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	2.5		2.5		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW $\overline{\text{CEA}}_n$ or $\overline{\text{CEB}}_n$ to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	1.5		1.5		ns
t _W (H) t _W (L)	Pulse Width, HIGH or LOW to $\overline{\text{CPAB}}_n$ or $\overline{\text{CPBA}}_n$	3.0		3.0		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5	pF	V _{CC} = 0V (Non I/O Pins)
C _{I/O} (Note 5)	Output Capacitance	11	pF	V _{CC} = 5.0V (A _n , B _n)

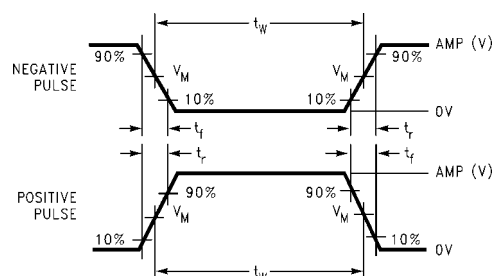
Note 5: C_{I/O} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



$V_M = 1.5V$

FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Input Signal Requirements

AC Waveforms

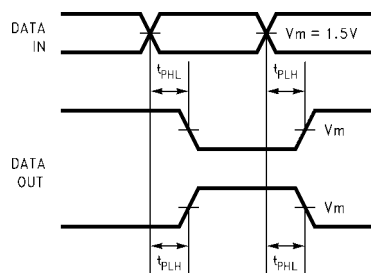


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

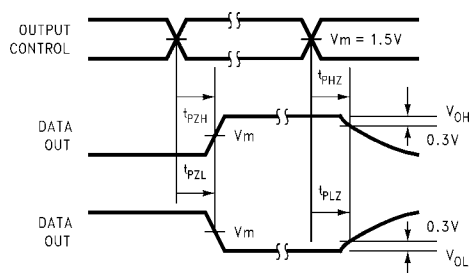


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

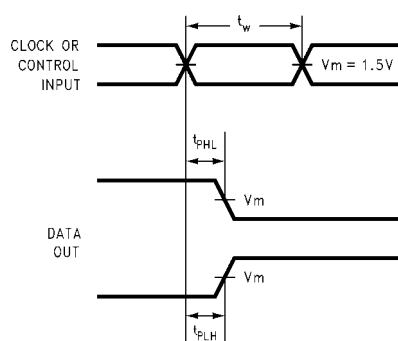


FIGURE 5. Propagation Delay, Pulse Width Waveforms

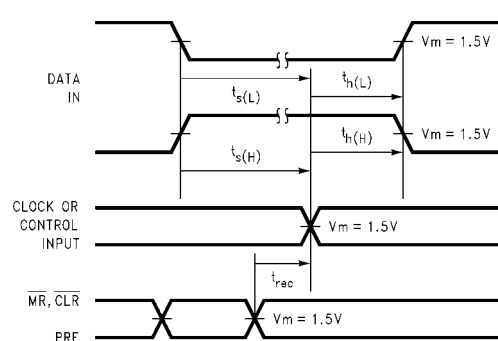
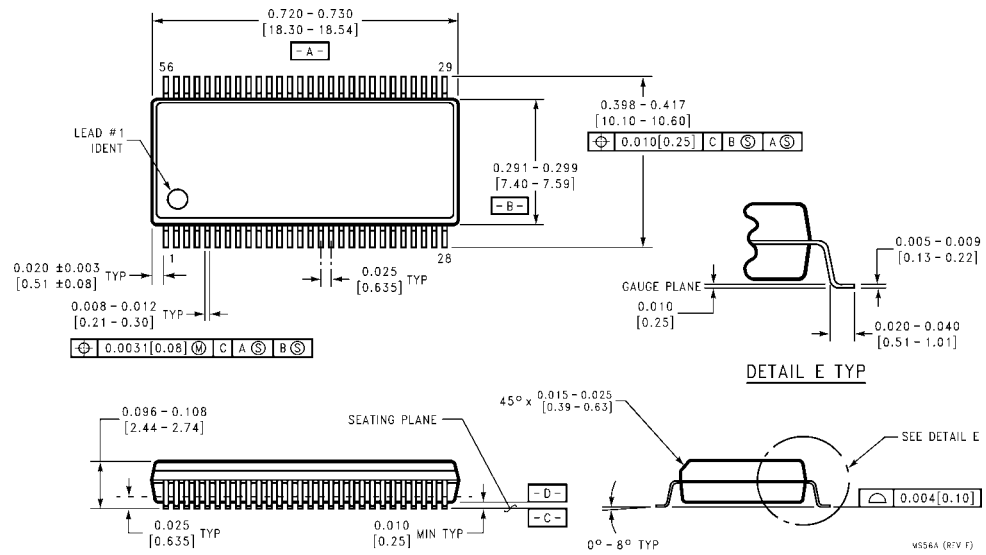


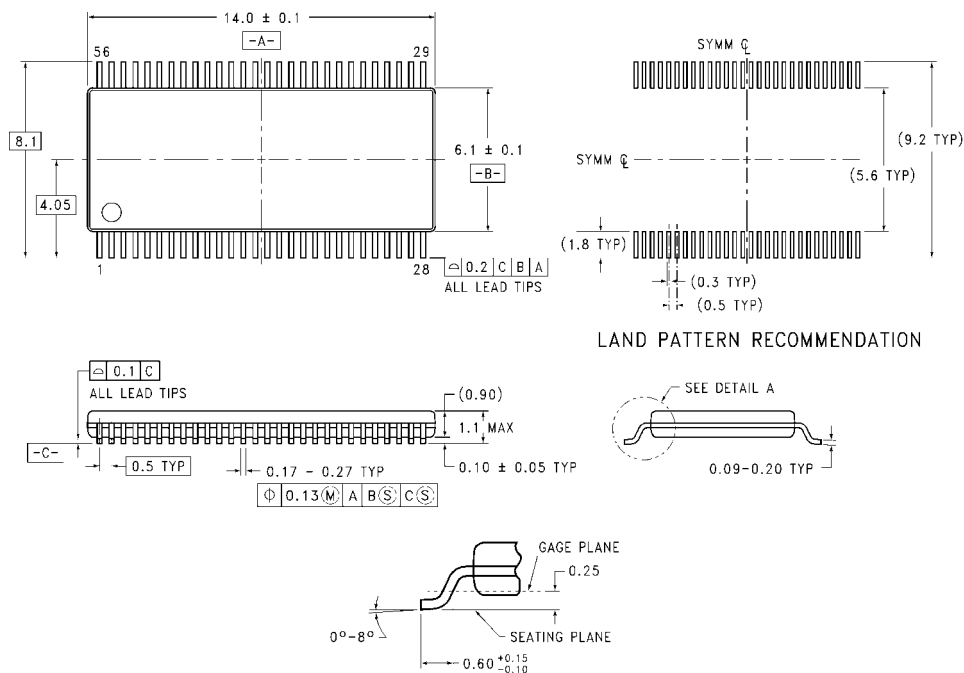
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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