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S1D13706 Embedded Memory LCD Controller

Hardware Functional Specification

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13706 Embedded Memory LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

For additional documentation related to the S1D13706 see Section 17, "References" on page 151.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13706 is a color/monochrome LCD graphics controller with an embedded 80K byte SRAM display buffer. While supporting all other panel types, the S1D13706 is the only LCD controller to directly interface to both the Epson D-TFD and the Sharp HR-TFT family of products thus removing the requirement of an external Timing Control IC. This high level of integration provides a low cost, low power, single chip solution to meet the demands of embedded markets such as Mobile Communications devices and Palm-size PCs, where board size and battery life are major concerns.

The S1D13706 utilizes a guaranteed low-latency CPU architecture providing support for microprocessors without READY/WAIT# handshaking signals. The 32-bit internal data path provides high performance bandwidth into display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView ™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13706 also provides support for "Picture-in-Picture Plus" (a variable size Overlay window).

The S1D13706 provides impressive support for Palm OS® handhelds, however its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

2 Features

2.1 Integrated Frame Buffer

- Embedded 80K byte SRAM display buffer.

2.2 CPU Interface

- Direct support of the following interfaces:
  Generic MPU bus interface using WAIT# signal.
  Hitachi SH-3.
  Hitachi SH-4.
  Motorola M68K.
  Motorola MC68EZ328/MC68VZ328 DragonBall.
  Motorola “REDCAP2” - no WAIT# signal.
- 8-bit processor support with “glue logic”.
- “Fixed” low-latency CPU access times.
- Registers are memory-mapped - M/R# input selects between memory and register address space.
- The complete 80K byte display buffer is directly and contiguously available through the 17-bit address bus.
- Single level CPU write buffer.

2.3 Display Support

- Single-panel, single-drive passive displays.
  - 4/8-bit monochrome LCD interface.
  - 4/8/16-bit color LCD interface.
- Active Matrix TFT interface.
  - 9/12/18-bit interface.
- ‘Direct’ support for 18-bit Epson D-TFD interface.
- ‘Direct’ support for 18-bit Sharp HR-TFT interface.

2.4 Display Modes

- 1/2/4/8/16 bit-per-pixel (bpp) color depths.
- Up to 64 gray shades using Frame Rate Modulation (FRM) and dithering on monochrome passive LCD panels.
- Up to 64K colors on passive STN panels.
- Up to 64K colors on active matrix LCD panels.
- Example resolutions:
  320x240 at a color depth of 8 bpp
  160x160 at a color depth of 16 bpp
  160x240 at a color depth of 16 bpp

2.5 Display Features

- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image.
- "Picture-in-Picture Plus": displays a variable size window overlaid over background image.
- Double Buffering/Multi-pages: provides smooth animation and instantaneous screen updates.

2.6 Clock Source

- Two clock inputs: CLKI and CLKI2. It is possible to use one clock input only.
- Bus clock is derived from CLKI and can be internally divided by 2, 3, or 4.
- Memory clock is derived from bus clock. It can be internally divided by 2, 3, or 4.
- Pixel clock can be derived from CLKI, CLKI2, bus clock, or memory clock. It can be internally divided by 2, 3, 4, or 8.

2.7 Miscellaneous

- Hardware/Software Video Invert.
- Software Power Save mode.
- General Purpose Input/Output pins are available.
- 100-pin TQFP15 package.
- 104-pin CFLGA package.
- Die form available.

3 Typical System Implementation Diagrams

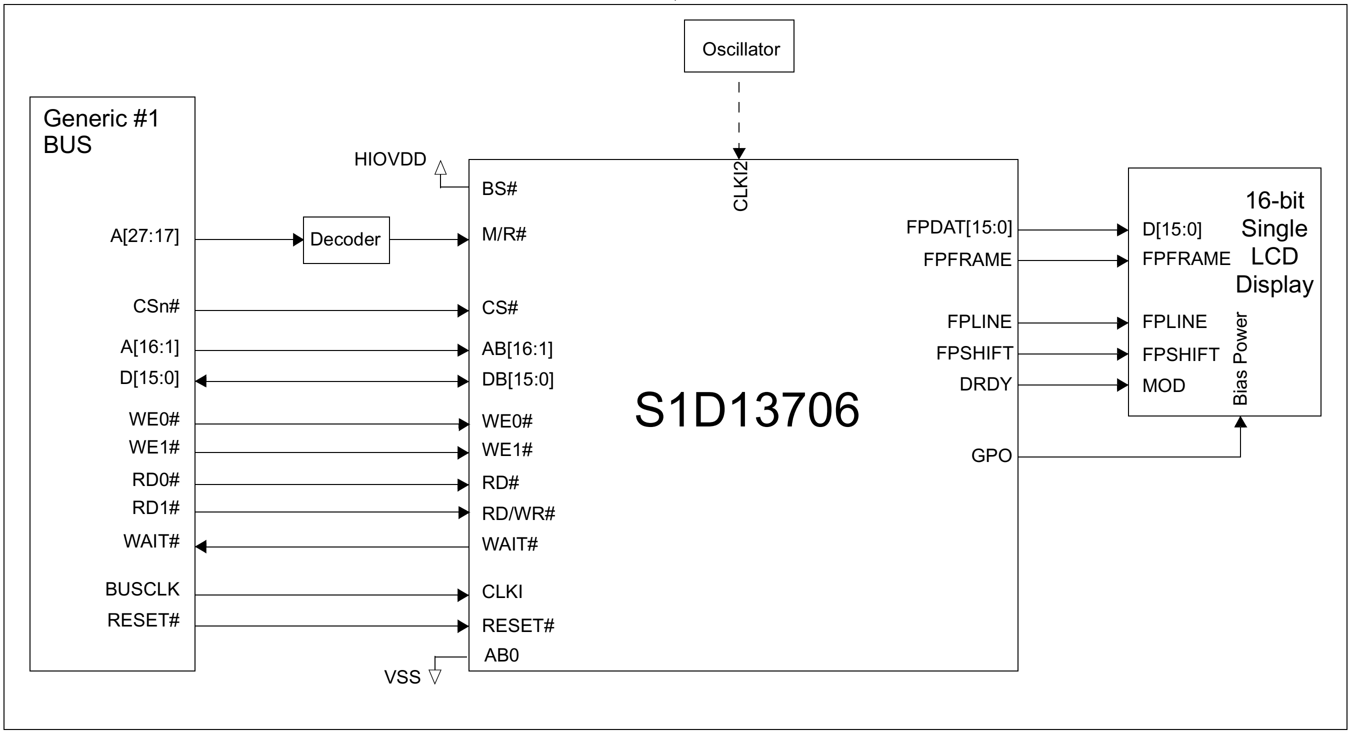


Figure 3-1: Typical System Diagram (Generic #1 Bus)

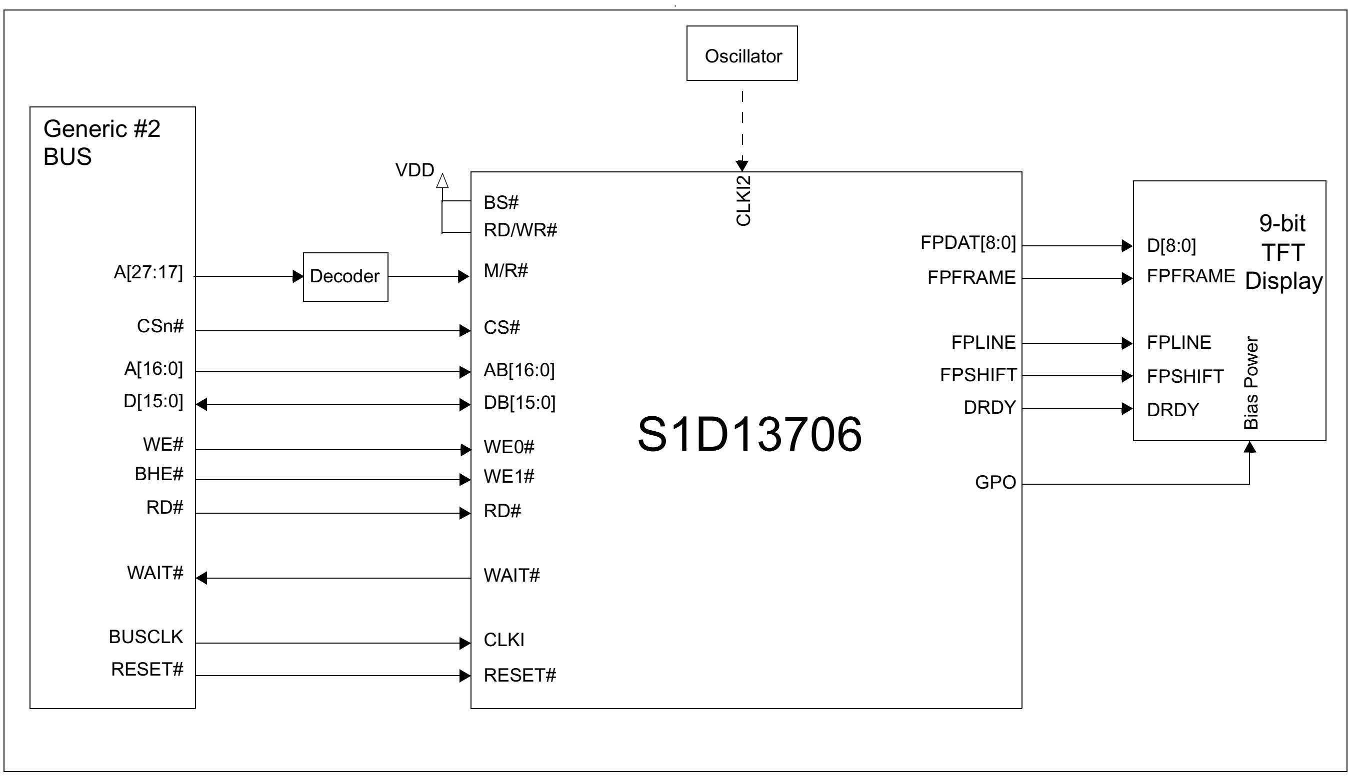


Figure 3-2: Typical System Diagram (Generic #2 Bus)

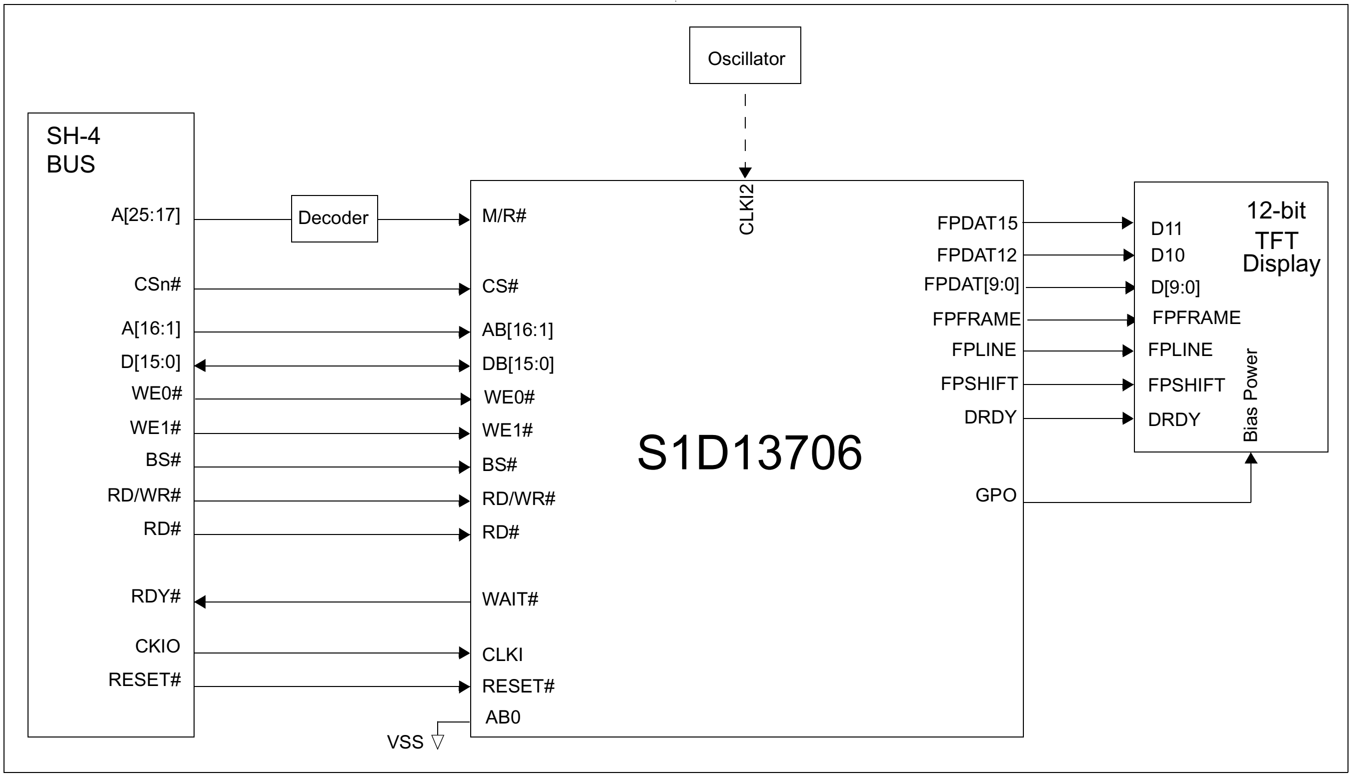


Figure 3-3: Typical System Diagram (Hitachi SH-4 Bus)

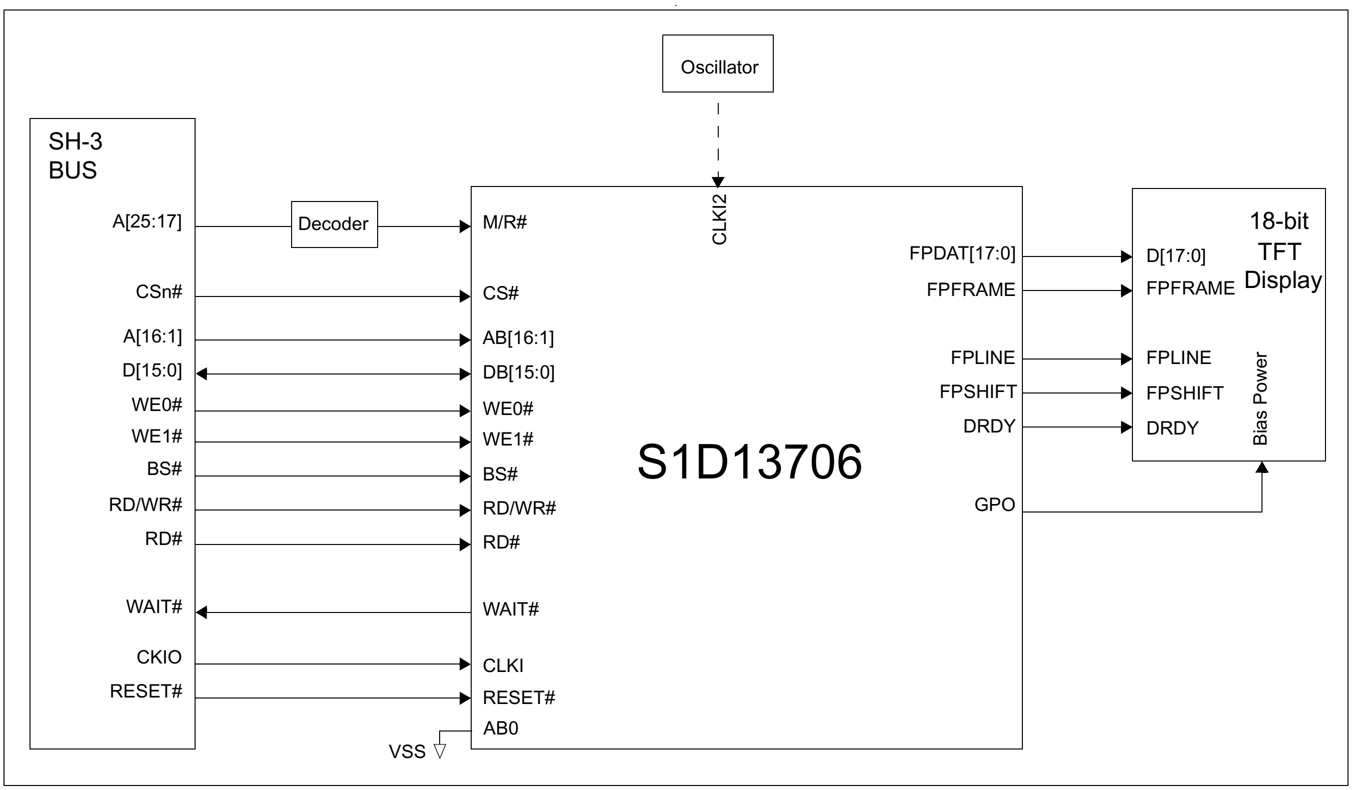


Figure 3-4: Typical System Diagram (Hitachi SH-3 Bus)

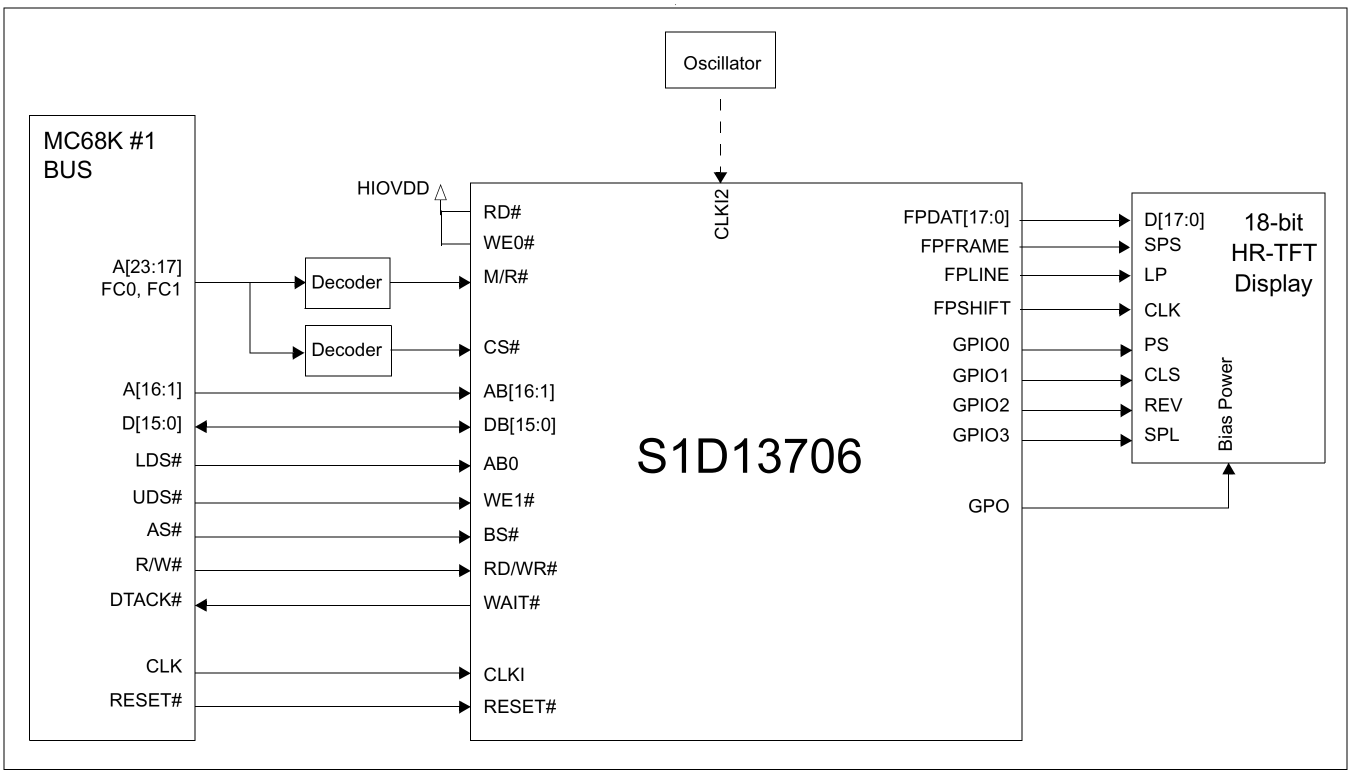


Figure 3-5: Typical System Diagram (MC68K # 1, Motorola 16-Bit 68000)

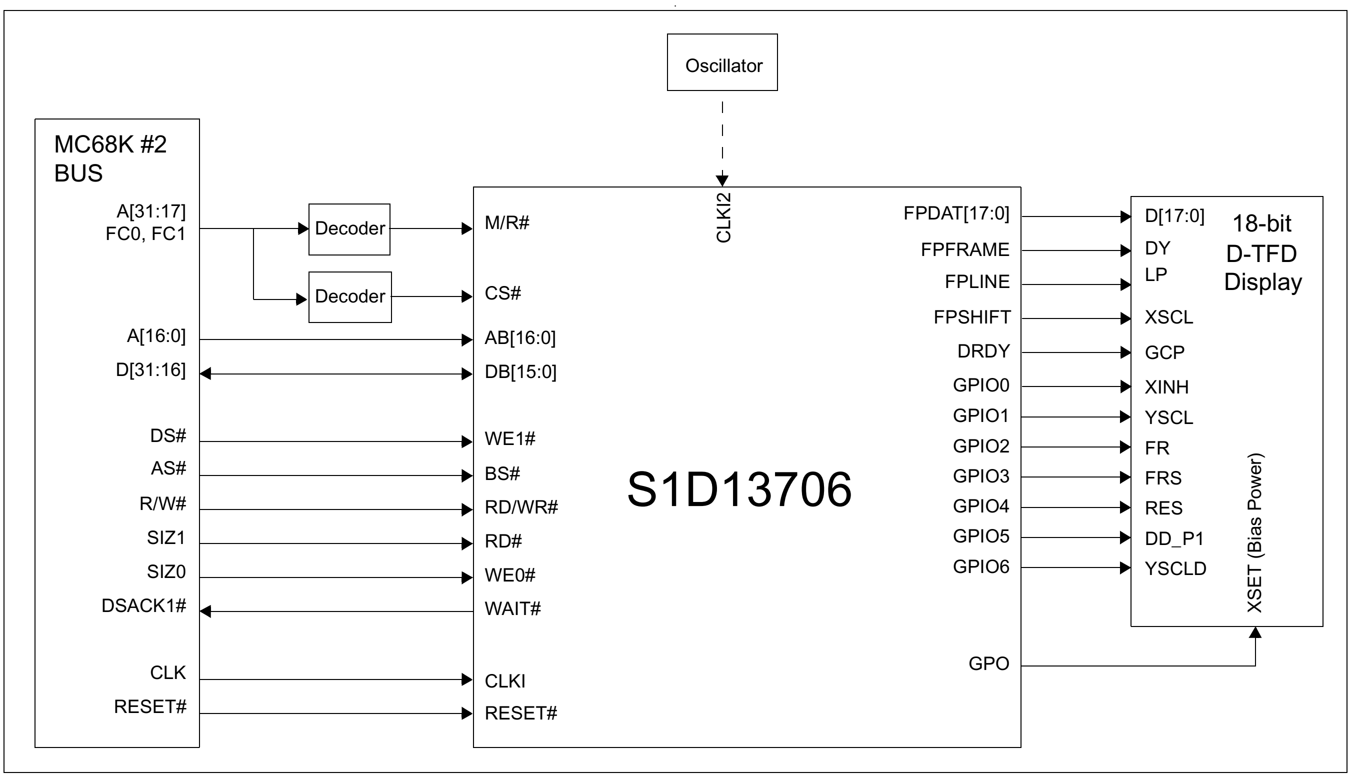


Figure 3-6: Typical System Diagram (MC68K #2, Motorola 32-Bit 68030)

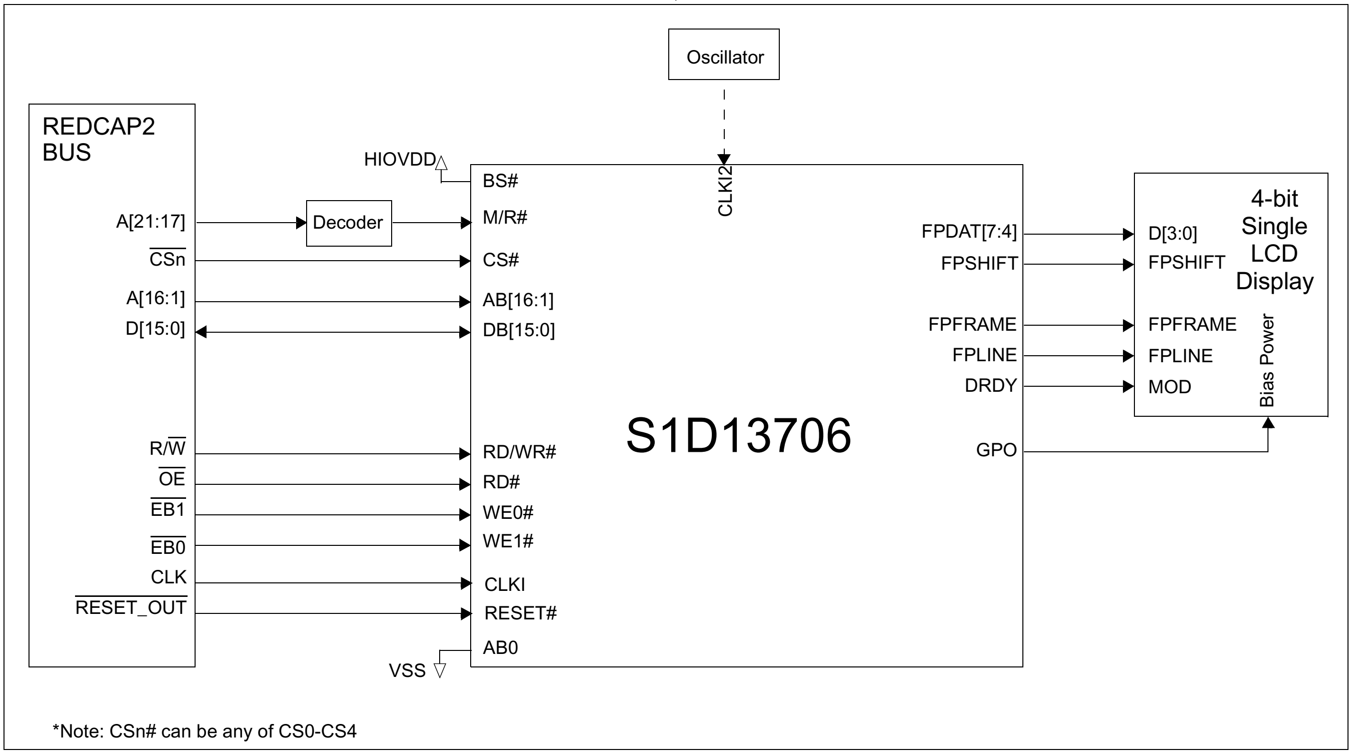


Figure 3-7: Typical System Diagram (Motorola REDCAP2 Bus)

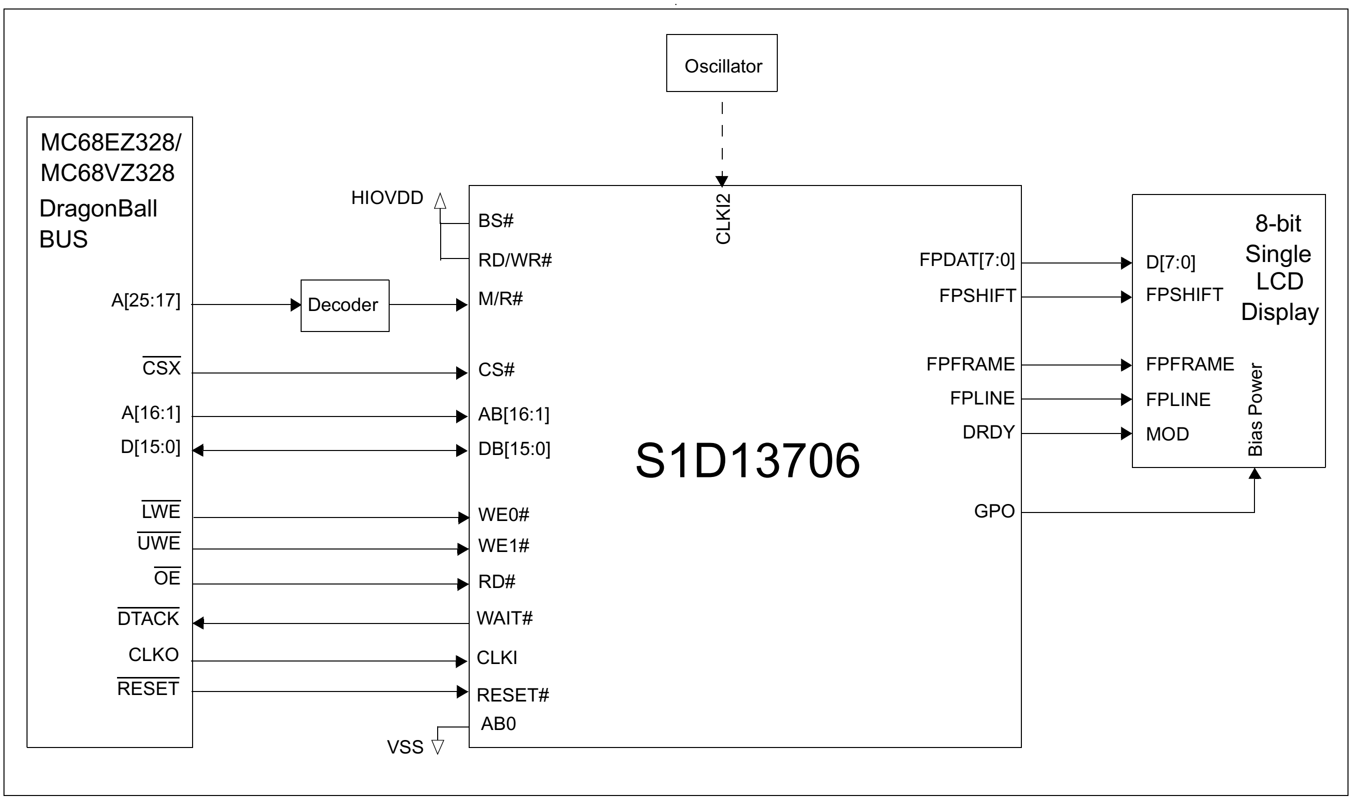


Figure 3-8: Typical System Diagram (Motorola MC68EZ328/MC68VZ328 "DragonBall" Bus)

4 Pins

4.1 Pinout Diagram - TQFP15 - 100pin

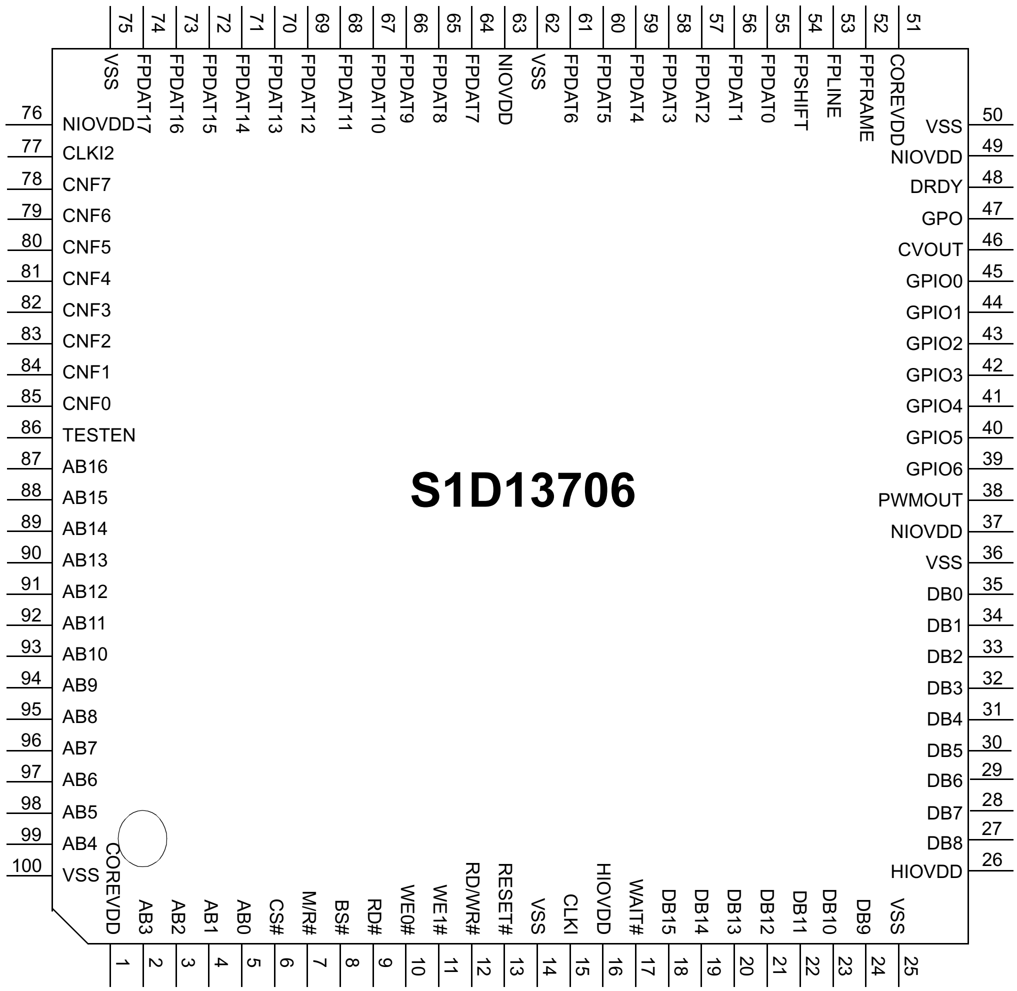


Figure 4-1: Pinout Diagram - TQFP15 - 100pin (S1D13706F00A)

Note
Package type: 100 pin surface mount TQFP15

4.2 Pinout Diagram - Die Form

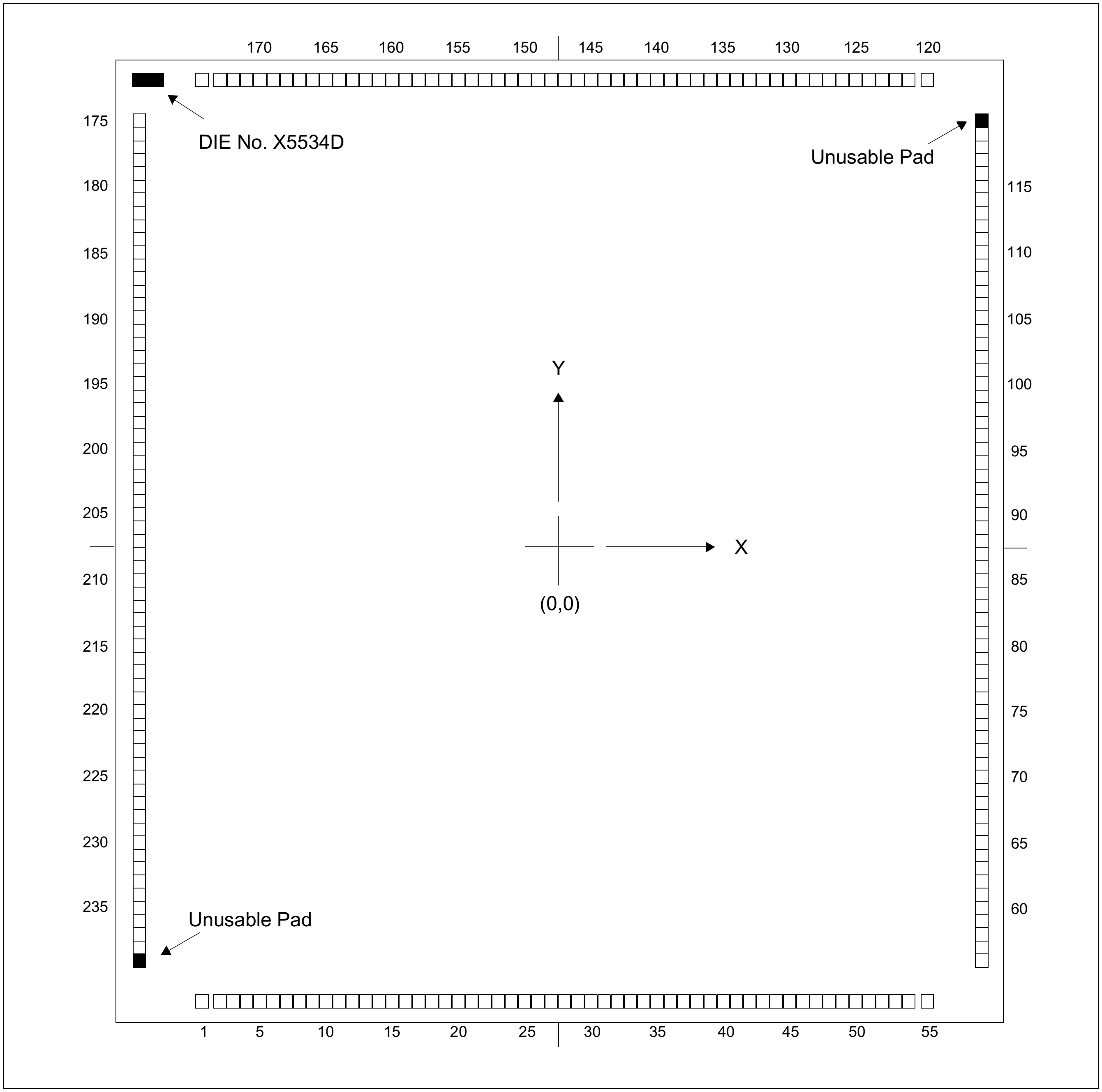


Figure 4-2: Pinout Diagram - Die Form (S1D13706D00A)

Chip Size: 5.88 x 6.55 mm
PAD size: 68 x 68 µm

Table 4-1: Pinout Assignments - Die Form (S1D13706D00A)

Pin No.	Pad No.	Pin Name	X (µm)	Y (µm)	Pin No.	Pad No.	Pin Name	X (µm)	Y (µm)
1	1	LVDD	-2331	-3149	51	119	LVDD	2813	2667
2	3	AB3	-2100	-3149	52	122	FPFRAME	2100	3149
3	5	AB2	-1932	-3149	53	124	FPLINE	1932	3149
4	8	AB1	-1680	-3149	54	127	FPSHIFT	1680	3149
5	10	AB0	-1512	-3149	55	129	FPDAT0	1512	3149
6	12	CS#	-1344	-3149	56	131	FPDAT1	1344	3149
7	15	M/R#	-1092	-3149	57	134	FPDAT2	1092	3149
8	17	BS#	-924	-3149	58	136	FPDAT3	924	3149
9	20	RD#	-672	-3149	59	139	FPDAT4	672	3149
10	22	WE0#	-504	-3149	60	141	FPDAT5	504	3149
11	24	WE1#	-336	-3149	61	143	FPDAT6	336	3149
12	27	RD/WR#	-84	-3149	62	146	VSS	84	3149
13	29	RESET#	84	-3149	63	148	HVDD	-84	3149
14	31	VSS	252	-3149	64	150	FPDAT7	-252	3149
15	34	CLKI	504	-3149	65	153	FPDAT8	-504	3149
16	36	HVDD	672	-3149	66	155	FPDAT9	-672	3149
17	39	WAIT#	924	-3149	67	158	FPDAT10	-924	3149
18	41	DB15	1092	-3149	68	160	FPDAT11	-1092	3149
19	43	DB14	1260	-3149	69	162	FPDAT12	-1260	3149
20	46	DB13	1512	-3149	70	165	FPDAT13	-1512	3149
21	48	DB12	1680	-3149	71	167	FPDAT14	-1680	3149
22	50	DB11	1848	-3149	72	169	FPDAT15	-1848	3149
23	53	DB10	2100	-3149	73	172	FPDAT16	-2100	3149
24	55	DB9	2331	-3149	74	174	FPDAT17	-2331	3149
25	58	VSS	2813	-2478	75	177	VSS	-2813	2478
26	60	HVDD	2813	-2310	76	179	HVDD	-2813	2310
27	62	DB8	2813	-2142	77	181	CLKI2	-2813	2142
28	65	DB7	2813	-1890	78	184	CNF7	-2813	1890
29	67	DB6	2813	-1722	79	186	CNF6	-2813	1722
30	70	DB5	2813	-1470	80	189	CNF5	-2813	1470
31	72	DB4	2813	-1302	81	191	CNF4	-2813	1302
32	74	DB3	2813	-1134	82	193	CNF3	-2813	1134
33	77	DB2	2813	-882	83	196	CNF2	-2813	882
34	79	DB1	2813	-714	84	198	CNF1	-2813	714
35	81	DB0	2813	-546	85	200	CNF0	-2813	546
36	84	VSS	2813	-294	86	203	TESTEN	-2813	294
37	86	HVDD	2813	-126	87	205	AB16	-2813	126
38	89	PWMOUT	2813	126	88	208	AB15	-2813	-126
39	91	GPIO6	2813	294	89	210	AB14	-2813	-294
40	93	GPIO5	2813	462	90	212	AB13	-2813	-462
41	96	GPIO4	2813	714	91	215	AB12	-2813	-714
42	98	GPIO3	2813	882	92	217	AB11	-2813	-882
43	100	GPIO2	2813	1050	93	219	AB10	-2813	-1050
44	103	GPIO1	2813	1302	94	222	AB9	-2813	-1302
45	105	GPIO0	2813	1470	95	224	AB8	-2813	-1470
46	108	CVOUT	2813	1722	96	227	AB7	-2813	-1722
47	110	GPO	2813	1890	97	229	AB6	-2813	-1890
48	112	DRDY	2813	2058	98	231	AB5	-2813	-2058
49	115	HVDD	2813	2310	99	234	AB4	-2813	-2310
50	117	VSS	2813	2478	100	236	VSS	-2813	-2478

4.3 Pin Descriptions

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
LIS	=	LVTTL[a] Schmitt input
LI	=	LVTTL input
LB2A	=	LVTTL IO buffer (6mA/-6mA@3.3V)
LB3P	=	Low noise LVTTL IO buffer (12mA/-12mA@3.3V)
LO3	=	Low noise LVTTL Output buffer (12mA/-12mA@3.3V)
LB3M	=	Low noise LVTTL IO buffer with input mask (12mA/-12mA@3.3V)
T1	=	Test mode control input with pull-down resistor (typical value of 50Ω at 3.3V)
Hi-Z	=	High Impedance

[a] LVTTL is Low Voltage TTL (see Section 5, “D.C. Characteristics” on page 31).

4.3.1 Host Interface

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
AB0	I	5	LIS	HIOVDD	0	This input pin has multiple functions. • For Generic #1, this pin is not used and should be connected to VSS. • For Generic #2, this pin inputs system address bit 0 (A0). • For SH-3/SH-4, this pin is not used and should be connected to VSS. • For MC68K #1, this pin inputs the lower data strobe (LDS#). • For MC68K #2, this pin inputs system address bit 0 (A0). • For REDCAP2, this pin is not used and should be connected to VSS. • For DragonBall, this pin is not used and should be connected to VSS. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
AB[16:1]	I	87-99, 2-4	LI	HIOVDD	0	System address bus bits 16-1.

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
DB[15:0]	IO	18-24, 27-35	LB2A	HIOVDD	Hi-Z	Input data from the system data bus. • For Generic #1, these pins are connected to D[15:0]. • For Generic #2, these pins are connected to D[15:0]. • For SH-3/SH-4, these pins are connected to D[15:0]. • For MC68K #1, these pins are connected to D[15:0]. • For MC68K #2, these pins are connected to D[31:16] for a 32-bit device (e.g. MC68030) or D[15:0] for a 16-bit device (e.g. MC68340). • For REDCAP2, these pins are connected to D[15:0]. • For DragonBall, these pins are connected to D[15:0]. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
WE0#	I	10	LIS	HIOVDD	1	This input pin has multiple functions. • For Generic #1, this pin inputs the write enable signal for the lower data byte (WE0#). • For Generic #2, this pin inputs the write enable signal (WE#) • For SH-3/SH-4, this pin inputs the write enable signal for data byte 0 (WE0#). • For MC68K #1, this pin must be tied to HIO V_{DD} • For MC68K #2, this pin inputs the bus size bit 0 (SIZ0). • For REDCAP2, this pin inputs the byte enable signal for the D[7:0] data byte ($\overline{EB1}$). • For DragonBall, this pin inputs the byte enable signal for the D[7:0] data byte ($\overline{LWE}$). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
WE1#	I	11	LIS	HIOVDD	1	This input pin has multiple functions. • For Generic #1, this pin inputs the write enable signal for the upper data byte (WE1#). • For Generic #2, this pin inputs the byte enable signal for the high data byte (BHE#). • For SH-3/SH-4, this pin inputs the write enable signal for data byte 1 (WE1#). • For MC68K #1, this pin inputs the upper data strobe (UDS#). • For MC68K #2, this pin inputs the data strobe (DS#). • For REDCAP2, this pin inputs the byte enable signal for the D[15:8] data byte ($\overline{EB0}$). • For DragonBall, this pin inputs the byte enable signal for the D[15:8] data byte ($\overline{UWE}$). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
CS#	I	6	LI	HIOVDD	1	Chip select input. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
M/R#	I	7	LIS	HIOVDD	0	This input pin is used to select between the display buffer and register address spaces of the S1D13706. M/R# is set high to access the display buffer and low to access the registers. See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.

Table 4-2: Host Interface Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Type</th><th>Pin #</th><th>Cell</th><th>IO Voltage</th><th>RESET# State</th><th>Description</th></tr>
<tr><td>BS#</td><td>I</td><td>8</td><td>LIS</td><td>HIOVDD</td><td>1</td><td>This input pin has multiple functions.
For Generic #1, this pin must be tied to HIO V_{DD}.
For Generic #2, this pin must be tied to HIO V_{DD}.
For SH-3/SH-4, this pin inputs the bus start signal (BS#).
For MC68K #1, this pin inputs the address strobe (AS#).
For MC68K #2, this pin inputs the address strobe (AS#).
For REDCAP2, this pin must be tied to HIO V_{DD}.
For DragonBall, this pin must be tied to HIO V_{DD}.
See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.</td></tr>
<tr><td>RD/WR#</td><td>I</td><td>12</td><td>LIS</td><td>HIOVDD</td><td>1</td><td>This input pin has multiple functions.
For Generic #1, this pin inputs the read command for the upper data byte (RD1#).
For Generic #2, this pin must be tied to HIO V_{DD}.
For SH-3/SH-4, this pin inputs the RD/WR# signal. The S1D13706 needs this signal for early decode of the bus cycle.
For MC68K #1, this pin inputs the R/W# signal.
For MC68K #2, this pin inputs the R/W# signal.
For REDCAP2, this pin inputs the R/$\overline{\text{W}}$ signal.
For DragonBall, this pin must be tied to HIO V_{DD}.
See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.</td></tr>
<tr><td>RD#</td><td>I</td><td>9</td><td>LIS</td><td>HIOVDD</td><td>1</td><td>This input pin has multiple functions.
For Generic #1, this pin inputs the read command for the lower data byte (RD0#).
For Generic #2, this pin inputs the read command (RD#).
For SH-3/SH-4, this pin inputs the read signal (RD#).
For MC68K #1, this pin must be tied to HIO V_{DD}.
For MC68K #2, this pin inputs the bus size bit 1 (SIZ1).
For REDCAP2, this pin inputs the output enable ($\overline{\text{OE}}$).
For DragonBall, this pin inputs the output enable ($\overline{\text{OE}}$).
See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.</td></tr>
</table>

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
WAIT#	O	17	LB2A	HIOVDD	Hi-Z	During a data transfer, this output pin is driven active to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to the high impedance state after the data transfer is complete. Its active polarity is configurable. See Table 4-7: “Summary of Power-On/Reset Options,” on page 28. • For Generic #1, this pin outputs the wait signal (WAIT#). • For Generic #2, this pin outputs the wait signal (WAIT#). • For SH-3 mode, this pin outputs the wait request signal (WAIT#). • For SH-4 mode, this pin outputs the device ready signal (RDY#). • For MC68K #1, this pin outputs the data transfer acknowledge signal (DTACK#). • For MC68K #2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#). • For REDCAP2, this pin is unused (Hi-Z). • For DragonBall, this pin outputs the data transfer acknowledge signal ($\overline{\text{DTACK}}$). See Table 4-8: “Host Bus Interface Pin Mapping,” on page 29 for summary.
RESET#	I	13	LIS	HIOVDD	0	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

4.3.2 LCD Interface

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
FPDAT[17:0]	O	74-64, 61-55	LB3P	NIOVDD	0	Panel Data bits 17-0.
FPFRAME	O	52	LB3P	NIOVDD	0	This output pin has multiple functions. • Frame Pulse • SPS for Sharp HR-TFT • DY for Epson D-TFD See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
FPLINE	O	53	LB3P	NIOVDD	0	This output pin has multiple functions. • Line Pulse • LP for Sharp HR-TFT • LP for Epson D-TFD See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
FPSHIFT	O	54	LB3P	NIOVDD	0	This output pin has multiple functions. • Shift Clock • CLK for Sharp HR-TFT • XSCL for Epson D-TFD See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
DRDY	O	48	LO3	NIOVDD	0	This output pin has multiple functions. • Display enable (DRDY) for TFT panels • 2nd shift clock (FPSHIFT2) for passive LCD with Format 1 interface • GCP for Epson D-TFD • LCD backplane bias signal (MOD) for all other LCD panels See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO0	IO	45	LB3M	NIOVDD	0	This pin has multiple functions. • PS for Sharp HR-TFT • XINH for Epson D-TFD • General purpose IO pin 0 (GPIO0) • Hardware Video Invert See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO1	IO	44	LB3M	NIOVDD	0	This pin has multiple functions. • CLS for Sharp HR-TFT • YSCL for Epson D-TFD • General purpose IO pin 1 (GPIO1) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
GPIO2	IO	43	LB3M	NIOVDD	0	This pin has multiple functions. • REV for Sharp HR-TFT • FR for Epson D-TFD • General purpose IO pin 2 (GPIO2) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO3	IO	42	LB3M	NIOVDD	0	This pin has multiple functions. • SPL for Sharp HR-TFT • FRS for Epson D-TFD • General purpose IO pin 3 (GPIO3) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO4	IO	41	LB3M	NIOVDD	0	This pin has multiple functions. • RES for Epson D-TFD • General purpose IO pin 4 (GPIO4) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO5	IO	40	LB3M	NIOVDD	0	This pin has multiple functions. • DD_P1 for Epson D-TFD • General purpose IO pin 5 (GPIO5) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
GPIO6	IO	39	LB3M	NIOVDD	0	This pin has multiple functions. • YSCLD for Epson D-TFD • General purpose IO pin 6 (GPIO6) See Table 4-9: “LCD Interface Pin Mapping,” on page 30 for summary.
PWMOUT	O	38	LB3P	NIOVDD	0	This output pin has multiple functions. • PWM Clock output • General purpose output
CVOUT	O	46	LB3P	NIOVDD	0	This output pin has multiple functions. • CV Pulse Output • General purpose output

4.3.3 Clock Input

Table 4-4: Clock Input Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
CLKI	I	15	LI	NIOVDD	—	Typically used as input clock source for bus clock and memory clock
CLKI2	I	77	LI	NIOVDD	—	Typically used as input clock source for pixel clock

4.3.4 Miscellaneous

Table 4-5: Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
CNF[7:0]	I	78-85	LI	NIOVDD	—	These inputs are used to configure the S1D13706 - see Table 4-7: “Summary of Power-On/Reset Options,” on page 28. **Note: These pins are used for configuration of the S1D13706 and must be connected directly to IO V_{DD} or V_{SS}.**
GPO	O	47	LO3	NIOVDD	0	General Purpose Output (possibly used for controlling the LCD power). It may also be used for the MOD control signal of the Sharp HR-TFT panel.
TESTEN	I	86	T1	NIOVDD	0	Test Enable input used for production test only (has type 1 pull-down resistor with a typical value of 50Ω at 3.3V).

4.3.5 Power And Ground

Table 4-6: Power And Ground Pin Descriptions

Pin Name	Type	Pin #	Cell	IO Voltage	RESET# State	Description
HIOVDD	P	16, 26	P	—	—	IO V_{DD} pins associated with the host interface pins as described in Section 4.3.1, “Host Interface” on page 21.
NIOVDD	P	37, 49, 63, 76	P	—	—	IO V_{DD} pins associated with the non-host interface pins as described in Section 4.3.2, “LCD Interface” on page 25, Section 4.3.3, “Clock Input” on page 27, and Section 4.3.4, “Miscellaneous” on page 27.
COREVDD	P	1, 51	P	—	—	2 Core $V_{DD.}$ pins.
VSS	P	14, 25, 36, 50, 62, 75, 100	P	—	—	7 V_{SS} pins.

4.4 Summary of Configuration Options

These pins are used for configuration of the S1D13706 and must be connected directly to $NIOV_{DD}$ or V_{SS}. The state of CNF[6:0] is latched on the rising edge of RESET#. Changing state at any other time has no effect.

Table 4-7: Summary of Power-On/Reset Options

<table>
<tr><th rowspan="2">S1D13706 Configuration Input</th><th colspan="2">Power-On/Reset State</th></tr>
<tr><th>1 (connected to NIOV_{DD})</th><th>0 (Connected to V_{SS})</th></tr>
<tr><td>CNF4,CNF[2:0]</td><td colspan="2">Select host bus interface as follows:

CNF4 CNF2 CNF1 CNF0 Host Bus
1 0 0 0 SH-4/SH-3 interface, Big Endian
0 0 0 0 SH-4/SH-3 interface, Little Endian
1 0 0 1 MC68K #1, Big Endian
0 0 0 1 Reserved
1 0 1 0 MC68K #2, Big Endian
0 0 1 0 Reserved
1 0 1 1 Generic #1, Big Endian
0 0 1 1 Generic #1, Little Endian
1 1 0 0 Reserved
0 1 0 0 Generic #2, Little Endian
1 1 0 1 REDCAP2, Big Endian
0 1 0 1 Reserved
1 1 1 0 DragonBall (MC68EZ328/MC68VZ328), Big Endian
0 1 1 0 Reserved
X 1 1 1 Reserved

Note: The host bus interface is 16-bit only.</td></tr>
<tr><td>CNF3</td><td>Configure GPIO pins as inputs at power-on</td><td>Configure GPIO pins as outputs at power-on (for use by HR-TFT/D-TFD when selected)</td></tr>
<tr><td>CNF5</td><td>WAIT# is active high</td><td>WAIT# is active low</td></tr>
<tr><td>CNF[7:6]</td><td colspan="2">CLKI to BCLK divide select:

CNF7 CNF6 CLKI to BCLK Divide Ratio
0 0 1 : 1
0 1 2 : 1
1 0 3 : 1
1 1 4 : 1</td></tr>
</table>

4.5 Host Bus Interface Pin Mapping

Table 4-8: Host Bus Interface Pin Mapping

S1D13706 Pin Name	Generic #1	Generic #2	Hitachi SH-3 /SH-4	Motorola MC68K #1	Motorola MC68K #2	Motorola REDCAP2	Motorola MC68EZ328/ MC68VZ328 DragonBall
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0[1]	A0	A0[1]	LDS#	A0	A0[1]	A0[1]
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0]	D[15:0][2]	D[15:0]	D[15:0]
CS#	External Decode		CSn#	External Decode		$\overline{\text{CSn}}$	$\overline{\text{CSX}}$
M/R#	External Decode						
CLKI	BUSCLK	BUSCLK	CKIO	CLK	CLK	CLK	CLKO
BS#	Connected to V_{DD}		BS#	AS#	AS#	Connected to V_{DD}	
RD/WR#	RD1#	Connected to V_{DD}	RD/WR#	R/W#	R/W#	R/$\overline{\text{W}}$	Connected to V_{DD}
RD#	RD0#	RD#	RD#	Connected to V_{DD}	SIZ1	$\overline{\text{OE}}$	$\overline{\text{OE}}$
WE0#	WE0#	WE#	WE0#	Connected to V_{DD}	SIZ0	$\overline{\text{EB1}}$	$\overline{\text{LWE}}$
WE1#	WE1#	BHE#	WE1#	UDS#	DS#	$\overline{\text{EB0}}$	$\overline{\text{UWE}}$
WAIT#	WAIT#	WAIT#	WAIT#/ RDY#	DTACK#	DSACK1#	N/A	$\overline{\text{DTACK}}$
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	$\overline{\text{RESET\_OUT}}$	$\overline{\text{RESET}}$

Note
[1] A0 for these busses is not used internally by the S1D13706 and should be connected to V_{SS}.
[2] If the target MC68K bus is 32-bit, then these signals should be connected to D[31:16].

4.6 LCD Interface Pin Mapping

Table 4-9: LCD Interface Pin Mapping

Pin Name	Monochrome Passive Panel		Color Passive Panel				Color TFT Panel				
	Single		Single				Others			Sharp HR-TFT[1]	Epson D-TFD[1]
	4-bit	8-bit	4-bit	Format 1 8-bit	Format 2 8-bit	16-Bit	9-bit	12-bit	18-bit	18-bit	18-bit
FPFRAME	FPFRAME									SPS	DY
FPLINE	FPLINE									LP	LP
FPSHIFT	FPSHIFT									DCLK	XSCL
DRDY	MOD			FPSHIFT2	MOD		DRDY			no connect	GCP
FPDAT0	driven 0	D0	driven 0	D0 (B5)[2]	D0 (G3)[2]	D0 (R6)[2]	R2	R3	R5	R5	R5
FPDAT1	driven 0	D1	driven 0	D1 (R5)[2]	D1 (R3)[2]	D1 (G5)[2]	R1	R2	R4	R4	R4
FPDAT2	driven 0	D2	driven 0	D2 (G4)[2]	D2 (B2)[2]	D2 (B4)[2]	R0	R1	R3	R3	R3
FPDAT3	driven 0	D3	driven 0	D3 (B3)[2]	D3 (G2)[2]	D3 (R4)[2]	G2	G3	G5	G5	G5
FPDAT4	D0	D4	D0 (R2)[2]	D4 (R3)[2]	D4 (R2)[2]	D8 (B5)[2]	G1	G2	G4	G4	G4
FPDAT5	D1	D5	D1 (B1)[2]	D5 (G2)[2]	D5 (B1)[2]	D9 (R5)[2]	G0	G1	G3	G3	G3
FPDAT6	D2	D6	D2 (G1)[2]	D6 (B1)[2]	D6 (G1)[2]	D10 (G4)[2]	B2	B3	B5	B5	B5
FPDAT7	D3	D7	D3 (R1)[2]	D7 (R1)[2]	D7 (R1)[2]	D11 (B3)[2]	B1	B2	B4	B4	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	D4 (G3)[2]	B0	B1	B3	B3	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	D5 (B2)[2]	driven 0	R0	R2	R2	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	D6 (R2)[2]	driven 0	driven 0	R1	R1	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	D7 (G1)[2]	driven 0	driven 0	R0	R0	R0
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	D12 (R3)[2]	driven 0	G0	G2	G2	G2
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	D13 (G2)[2]	driven 0	driven 0	G1	G1	G1
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	D14 (B1)[2]	driven 0	driven 0	G0	G0	G0
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	D15 (R1)[2]	driven 0	B0	B2	B2	B2
FPDAT16	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B1	B1	B1
FPDAT17	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	B0	B0	B0
GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	PS	XINH
GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	CLS	YSCL
GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	REV	FR
GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	SPL	FRS
GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4	GPIO4 (output only)	RES
GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5	GPIO5 (output only)	DD_P1
GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6	GPIO6 (output only)	YSCLD
GPO	GPO (General Purpose Output)									MOD[3]	GPO
CVOUT	CVOUT										
PWMOUT	PWMOUT										

Note

[1] GPIO pins must be configured as outputs (CNF3 = 0 at RESET#) when the HR-TFT or D-TFD interface is selected.

[2] These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see Section 6.4, “Display Interface” on page 56.

[3] When the HR-TFT interface is selected (REG[10h] bits 1-0 = 10), this GPO can be used to control the HR-TFT MOD signal. Note this is not the same signal as the S1D13706 DRDY(MOD) signal used for passive panels.

5 D.C. Characteristics

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	1.8	2.0	2.2	V
			3.0	3.3	3.6	V
HIO V_{DD}	Supply Voltage	V_{SS} = 0 V	1.8	2.0	2.2	V
			3.0	3.3	3.6	V
NIO V_{DD}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
V_{IN}	Input Voltage		V_{SS}		IO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Note
The S1D13706 requires that Core VDD ≤ HIO VDD and Core VDD ≤ NIO VDD.

Table 5-3: Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			170	µA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min I_{OH} = -6mA (Type 2) -12mA (Type 3)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 6mA (Type 2) 12mA (Type 3)			0.4	V
V_{IH}	High Level Input Voltage	LVTTL Level, V_{DD} = max	2.0			V
V_{IL}	Low Level Input Voltage	LVTTL Level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	LVTTL Schmitt	1.1		2.4	V
V_{T-}	Low Level Input Voltage	LVTTL Schmitt	0.6		1.8	V
V_{H1}	Hysteresis Voltage	LVTTL Schmitt	0.1			V
R_{PD}	Pull Down Resistance	V_I = V_{DD}	20	50	120	kΩ
C_I	Input Pin Capacitance				10	pF
C_O	Output Pin Capacitance				10	pF
C_{IO}	Bi-Directional Pin Capacitance				10	pF

6 A.C. Characteristics

Conditions: HIO V_{DD} = 2.0V ± 10% and HIO V_{DD} = 3.3V ± 10%
NIO V_{DD} = 3.3V ± 10%
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 50pF (Bus/MPU Interface)
C_L = 0pF (LCD Panel Interface)

6.1 Clock Timing

6.1.1 Input Clocks

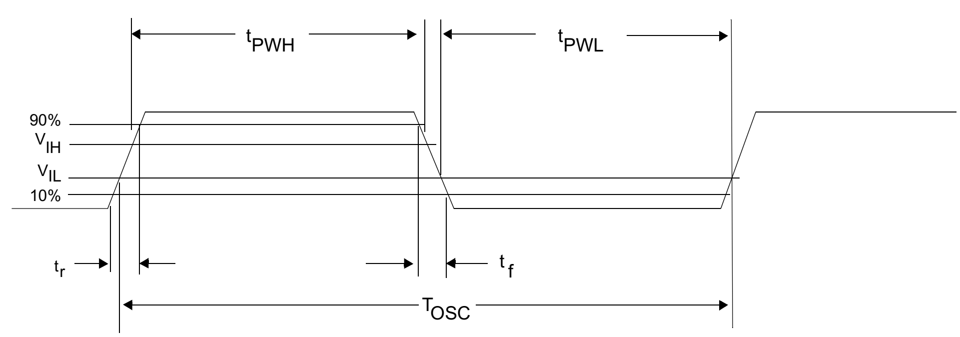


Figure 6-1: Clock Input Requirements

Table 6-1: Clock Input Requirements for CLKI when CLKI to BCLK divide > 1

Symbol	Parameter	2.0V		3.3V		Units
		Min	Max	Min	Max	
f_{OSC}	Input Clock Frequency (CLKI)		40		100	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$		$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	4.5		4.5		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	4.5		4.5		ns
t_f	Input Clock Fall Time (10% - 90%)		5		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5		5	ns

Note
Maximum internal requirements for clocks derived from CLKI must be considered when determining the frequency of CLKI. See Section 6.1.2, “Internal Clocks” on page 34 for internal clock requirements.

Table 6-2: Clock Input Requirements for CLKI when CLKI to BCLK divide = 1

Symbol	Parameter	2.0V		3.3V		Units
		Min	Max	Min	Max	
f_{OSC}	Input Clock Frequency (CLKI)		20		66	MHz
T_{OSC}	Input Clock period (CLKI)	$1/f_{OSC}$		$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	3		3		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	3		3		ns
t_f	Input Clock Fall Time (10% - 90%)		5		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5		5	ns

Note

Maximum internal requirements for clocks derived from CLKI must be considered when determining the frequency of CLKI. See Section 6.1.2, “Internal Clocks” on page 34 for internal clock requirements.

Table 6-3: Clock Input Requirements for CLKI2

Symbol	Parameter	2.0V		3.3V		Units
		Min	Max	Min	Max	
f_{OSC}	Input Clock Frequency (CLKI2)		20		66	MHz
T_{OSC}	Input Clock period (CLKI2)	$1/f_{OSC}$		$1/f_{OSC}$		ns
t_{PWH}	Input Clock Pulse Width High (CLKI2)	3		3		ns
t_{PWL}	Input Clock Pulse Width Low (CLKI2)	3		3		ns
t_f	Input Clock Fall Time (10% - 90%)		5		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5		5	ns

Note

Maximum internal requirements for clocks derived from CLKI2 must be considered when determining the frequency of CLKI2. See Section 6.1.2, “Internal Clocks” on page 34 for internal clock requirements.

6.1.2 Internal Clocks

Table 6-4: Internal Clock Requirements

Symbol	Parameter	2.0V		3.3V		Units
		Min	Max	Min	Max	
f_{BCLK}	Bus Clock frequency		20		66	MHz
f_{MCLK}	Memory Clock frequency		20		50	MHz
f_{PCLK}	Pixel Clock frequency		20		50	MHz
f_{PWMCLK}	PWM Clock frequency		20		66	MHz

Note
For further information on internal clocks, refer to Section 7, “Clocks” on page 90.

6.2 CPU Interface Timing

The following section includes CPU interface AC Timing for both 2.0V and 3.3V. The 2.0V timings are based on HIO V_{DD} = Core V_{DD} = 2.0V. The 3.3V timings are based on HIO V_{DD} = Core V_{DD} = 3.3V.

6.2.1 Generic #1 Interface Timing

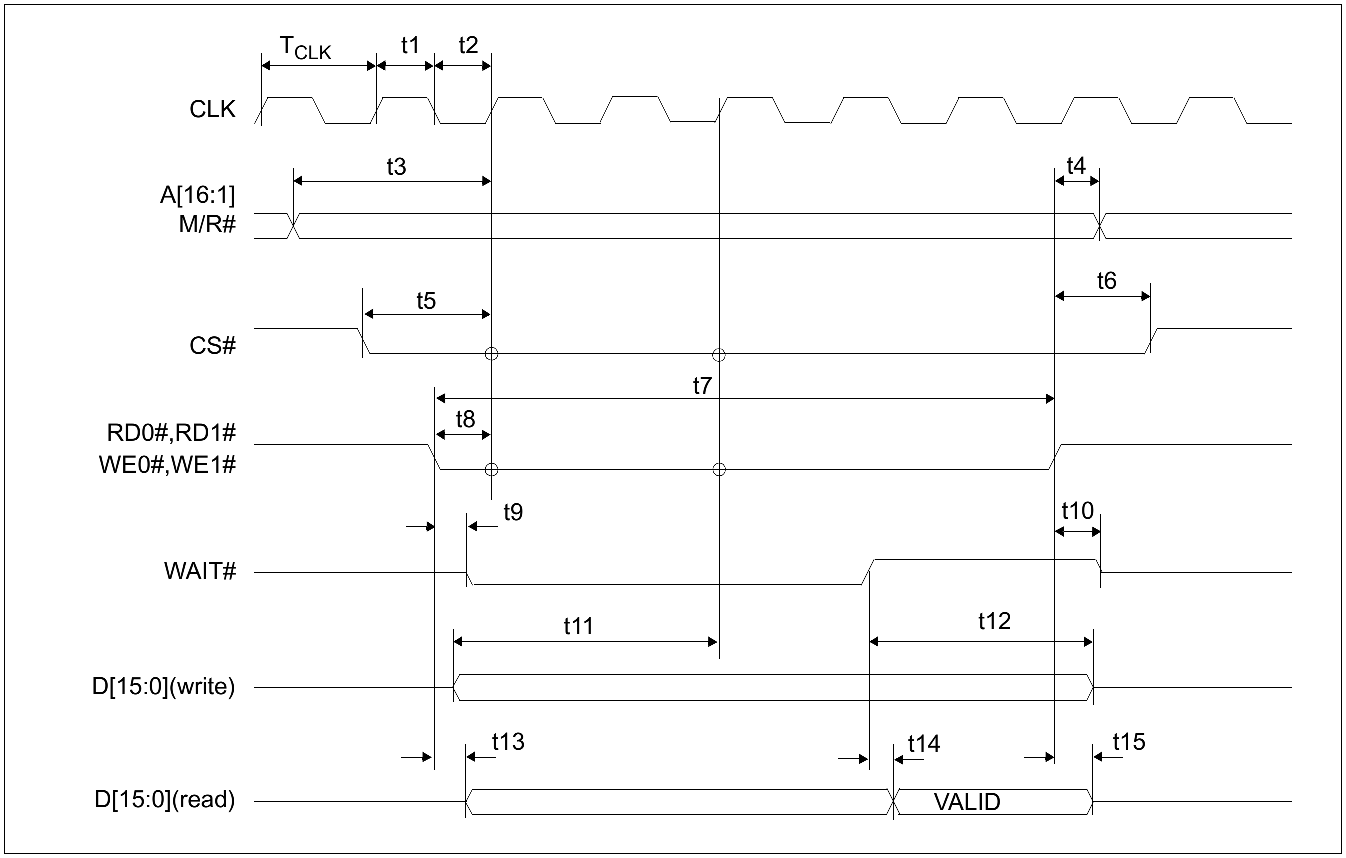


Figure 6-2: Generic #1 Interface Timing

Table 6-5: Generic #1 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{CLK}	Bus Clock frequency		20		50	MHz
T_{CLK}	Bus Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t1	Clock pulse width high	22.5		9		ns
t2	Clock pulse width low	22.5		9		ns
t3	A[16:1], M/R# setup to first CLK rising edge where CS# = 0 and either RD0#, RD1# = 0 or WE0#, WE1# = 0	1		1		ns
t4	A[16:1], M/R# hold from either RD0#, RD1# or WE0#, WE1# rising edge	0		0		ns
t5	CS# setup to CLK rising edge	0		1		ns
t6	CS# hold from either RD0#, RD1# or WE0#, WE1# rising edge	0		0		ns
t7a	RD0#, RD1#, WE0#, WE1# asserted for MCLK = BCLK		8.5		8.5	T_{CLK}
t7b	RD0#, RD1#, WE0#, WE1# asserted for MCLK = BCLK ÷ 2		11.5		11.5	T_{CLK}
t7c	RD0#, RD1#, WE0#, WE1# asserted for MCLK = BCLK ÷ 3		13.5		13.5	T_{CLK}
t7d	RD0#, RD1#, WE0#, WE1# asserted for MCLK = BCLK ÷ 4		17.5		17.5	T_{CLK}
t8	RD0#, RD1#, WE0#, WE1# setup to CLK rising edge	2		1		ns
t9	Falling edge of either RD0#, RD1# or WE0#, WE1# to WAIT# driven low	5	31	3	15	ns
t10	Rising edge of either RD0#, RD1# or WE0#, WE1# to WAIT# high impedance	5	34	3	13	ns
t11	D[15:0] setup to third CLK rising edge where CS# = 0 and WE0#, WE1# = 0 (write cycle) (see note 1)	1		0		ns
t12	D[15:0] hold from WAIT# rising edge (write cycle)	1		0		ns
t13	RD0#, RD1# falling edge to D[15:0] driven (read cycle)	4	27	3	14	ns
t14	WAIT# rising edge to D[15:0] valid (read cycle)		0		2	ns
t15	RD0#, RD1# rising edge to D[15:0] high impedance (read cycle)	3	29	3	11	ns

1. t11 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.2 Generic #2 Interface Timing (e.g. ISA)

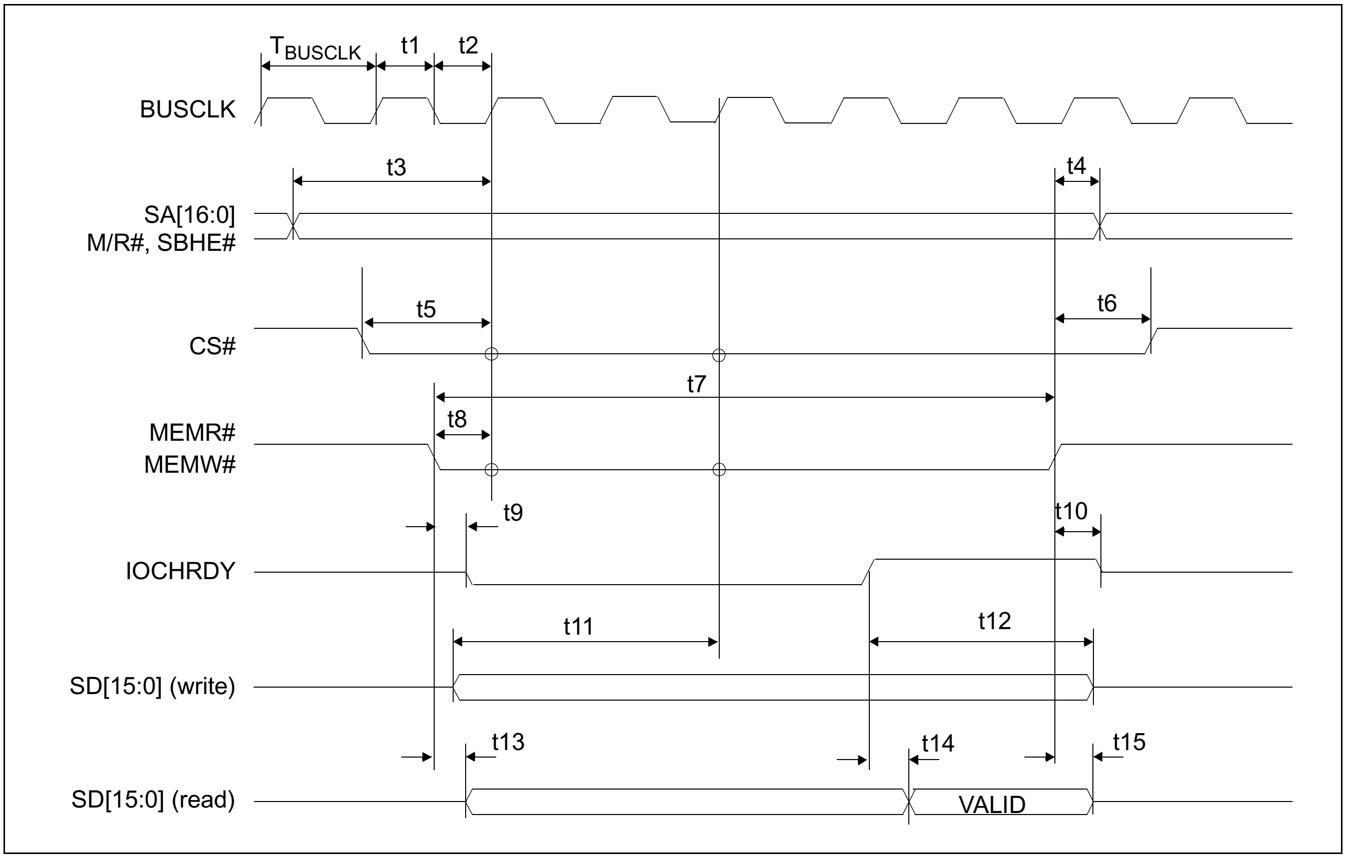


Figure 6-3: Generic #2 Interface Timing

Table 6-6: Generic #2 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{BUSCLK}	Bus Clock frequency		20		50	MHz
T_{BUSCLK}	Bus Clock period	$1/f_{BUSCLK}$		$1/f_{BUSCLK}$		ns
t1	Clock pulse width high	22.5		9		ns
t2	Clock pulse width low	22.5		9		ns
t3	SA[16:0], M/R#, SBHE# setup to first BUSCLK rising edge where CS# = 0 and either MEMR# = 0 or MEMW# = 0	1		1		ns
t4	SA[16:0], M/R#, SBHE# hold from either MEMR# or MEMW# rising edge	0		0		ns
t5	CS# setup to BUSCLK rising edge	0		1		ns
t6	CS# hold from either MEMR# or MEMW# rising edge	0		0		ns
t7a	MEMR#/MEMW# asserted for MCLK = BCLK		8.5		8	T_{BUSCLK}
t7b	MEMR#/MEMW# asserted for MCLK = BCLK ÷ 2		11.5		11	T_{BUSCLK}
t7c	MEMR#/MEMW# asserted for MCLK = BCLK ÷ 3		13.5		13	T_{BUSCLK}
t7d	MEMR#/MEMW# asserted for MCLK = BCLK ÷ 4		17.5		17	T_{BUSCLK}
t8	MEMR# or MEMW# setup to BUSCLK rising edge	2		1		ns
t9	Falling edge of either MEMR# or MEMW# to IOCHRDY driven low	5		3	15	ns
t10	Rising edge of either MEMR# or MEMW# to IOCHRDY high impedance	5		3	13	ns
t11	SD[15:0] setup to third BUSCLK rising edge where CS# = 0 and MEMW# = 0 (write cycle) (see note 1)	1		0		ns
t12	SD[15:0] hold from IOCHRDY rising edge (write cycle)	1		0		ns
t13	MEMR# falling edge to SD[15:0] driven (read cycle)	4	26	3	13	ns
t14	IOCHRDY rising edge to SD[15:0] valid (read cycle)		0		2	ns
t15	Rising edge of MEMR# to SD[15:0] high impedance (read cycle)	5	33	3	12	ns

1. t11 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.3 Hitachi SH-4 Interface Timing

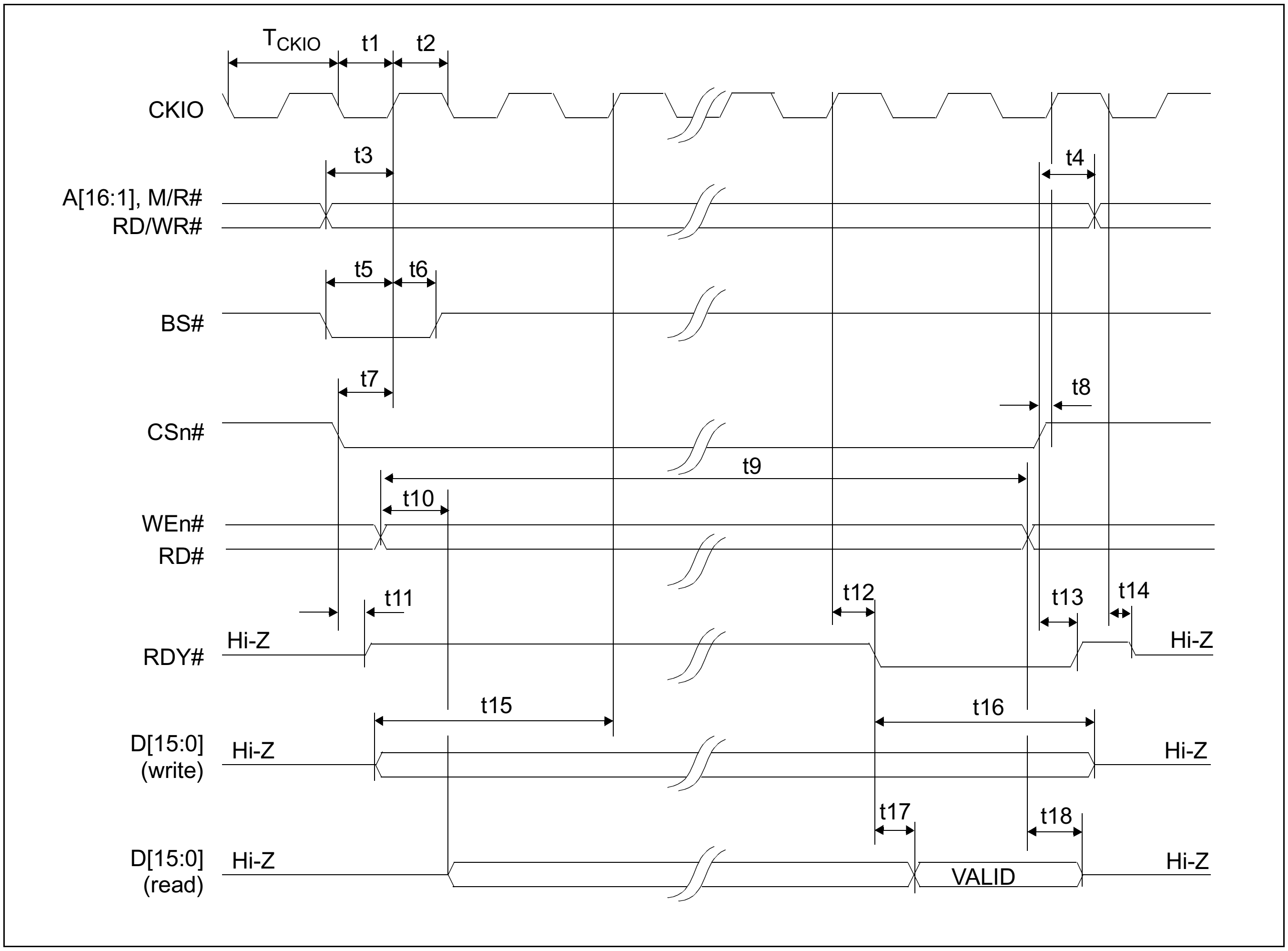


Figure 6-4: Hitachi SH-4 Interface Timing

Table 6-7: Hitachi SH-4 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{CKIO}	Clock frequency		20		66	MHz
T_{CKIO}	Clock period	$1/f_{CKIO}$		$1/f_{CKIO}$		ns
t1	Clock pulse width low	22.5		6.8		ns
t2	Clock pulse width high	22.5		6.8		ns
t3	A[16:1], M/R#, RD/WR# setup to CKIO	0		1		ns
t4	A[16:1], M/R#, RD/WR# hold from CSn#	0		0		ns
t5	BS# setup	3		1		ns
t6	BS# hold	7		2		ns
t7	CSn# setup	0		1		ns
t8	CSn# high setup to CKIO	0		2		ns
t9a	RD# or WEn# asserted for MCLK = BCLK (max. MCLK = 50MHz)		8.5		8.5	T_{CKIO}
t9b	RD# or WEn# asserted for MCLK = BCLK ÷ 2		11.5		11.5	T_{CKIO}
t9c	RD# or WEn# asserted for MCLK = BCLK ÷ 3		13.5		13.5	T_{CKIO}
t9d	RD# or WEn# asserted for MCLK = BCLK ÷ 4		18.5		18.5	T_{CKIO}
t10	Falling edge RD# to D[15:0] driven (read cycle)	5	24	3	12	ns
t11	Falling edge CSn# to RDY# driven high	3	19	3	12	ns
t12	CKIO to RDY# low	5	42	4	18	ns
t13	CSn# high to RDY# high	5	35	4	14	ns
t14	Falling edge CKIO to RDY# high impedance	5	38	4	14	ns
t15	D[15:0] setup to 2^{nd} CKIO after BS# (write cycle) (see note 1)	1		0		ns
t16	D[15:0] hold (write cycle)	0		0		ns
t17	RDY# falling edge to D[15:0] valid (read cycle)		0		2	ns
t18	Rising edge RD# to D[15:0] high impedance (read cycle)	5	31	3	12	ns

1. t15 is the delay from when data is placed on the bus until the data is latched into the write buffer.

Note
Minimum one software WAIT state is required.

6.2.4 Hitachi SH-3 Interface Timing

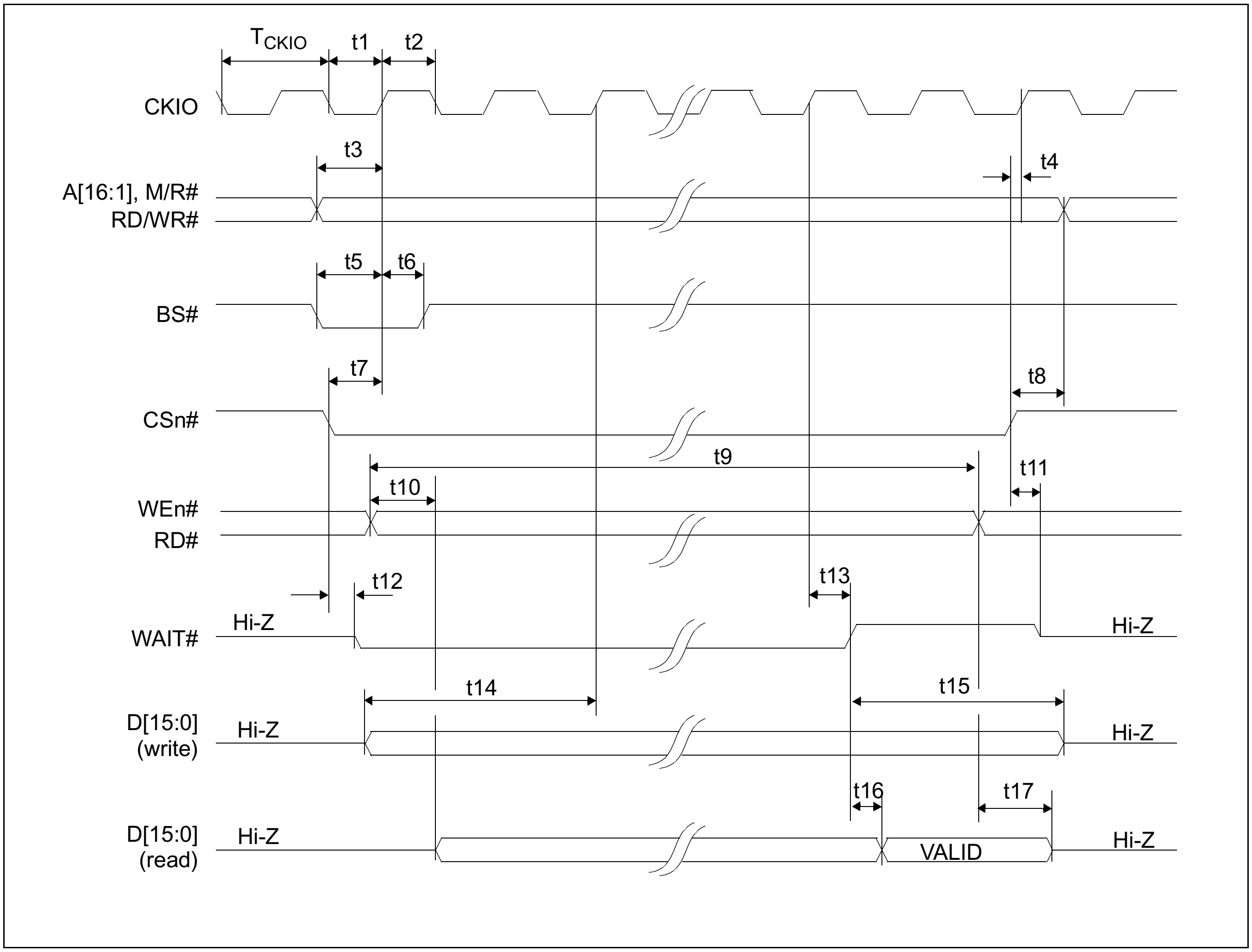


Figure 6-5: Hitachi SH-3 Interface Timing

Table 6-8: Hitachi SH-3 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{CKIO}	Bus Clock frequency		20		66	MHz
T_{CKIO}	Bus Clock period	$1/f_{CKIO}$		$1/f_{CKIO}$		ns
t1	Bus Clock pulse width low	22.5		6.8		ns
t2	Bus Clock pulse width high	22.5		6.8		ns
t3	A[16:1], M/R#, RD/WR# setup to CKIO	0		1		ns
t4	CSn# high setup to CKIO	0		1		ns
t5	BS# setup	3		1		ns
t6	BS# hold	7		2		ns
t7	CSn# setup	0		1		ns
t8	A[16:1], M/R#, RD/WR# hold from CS#	0		0		ns
t9a	RD# or WEn# asserted for MCLK = BCLK (max. MCLK = 50MHz)		8.5		8.5	T_{CKIO}
t9b	RD# or WEn# asserted for MCLK = BCLK ÷ 2		11.5		11.5	T_{CKIO}
t9c	RD# or WEn# asserted for MCLK = BCLK ÷ 3		13.5		13.5	T_{CKIO}
t9d	RD# or WEn# asserted for MCLK = BCLK ÷ 4		18.5		18.5	T_{CKIO}
t10	Falling edge RD# to D[15:0] driven (read cycle)	5	24	3	12	ns
t11	Rising edge CSn# to WAIT# high impedance	4	24	2	10	ns
t12	Falling edge CSn# to WAIT# driven low	3	24	2	12	ns
t13	CKIO to WAIT# delay	6	45	4	18	ns
t14	D[15:0] setup to 2^{nd} CKIO after BS# (write cycle) (see note 1)	1		0		ns
t15	D[15:0] hold (write cycle)	0		0		ns
t16	WAIT# rising edge to D[15:0] valid (read cycle)		0		2	ns
t17	Rising edge RD# to D[15:0] high impedance (read cycle)	5	31	3	12	ns

1. t14 is the delay from when data is placed on the bus until the data is latched into the write buffer.

Note

Minimum one software WAIT state is required.

6.2.5 Motorola MC68K #1 Interface Timing (e.g. MC68000)

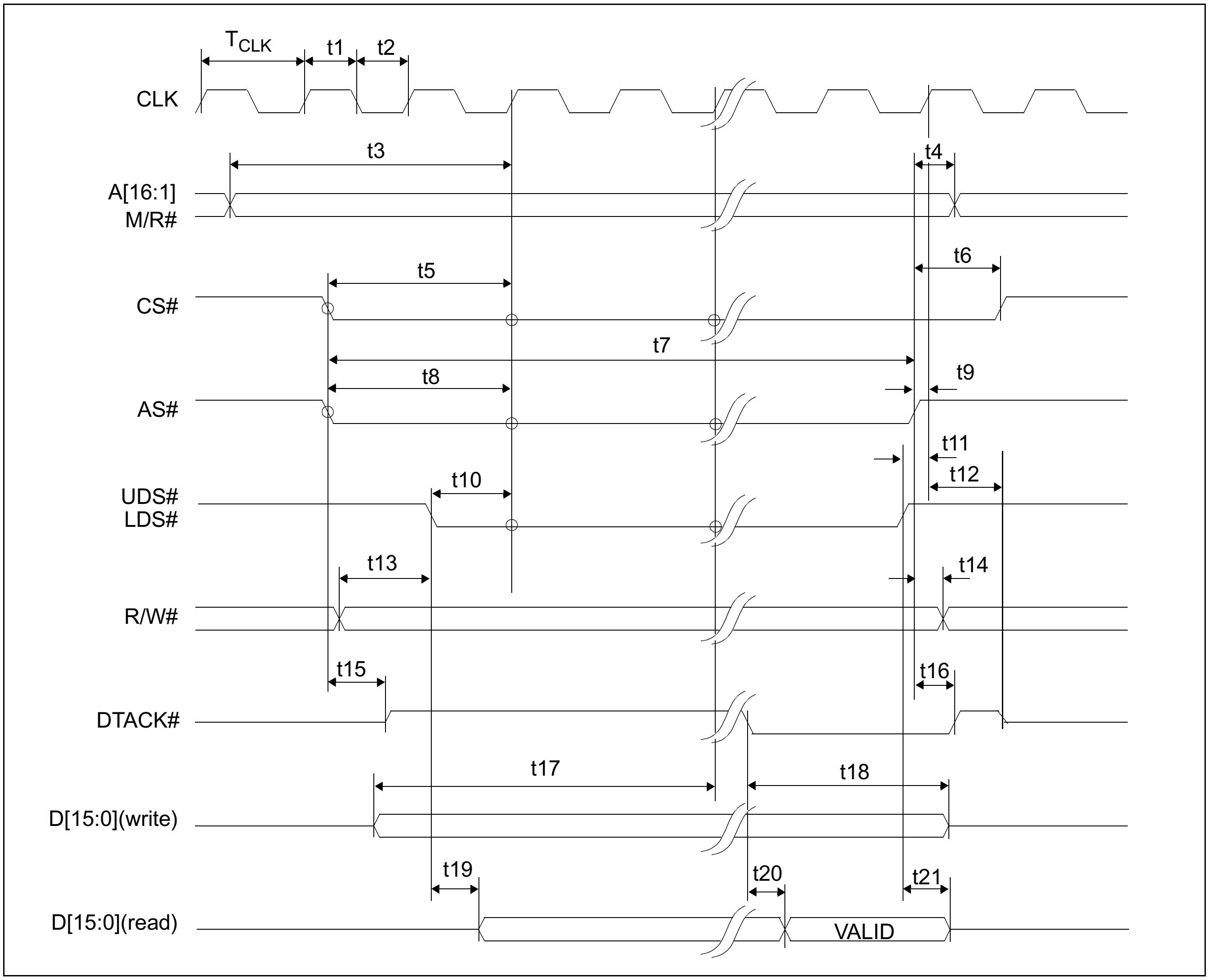


Figure 6-6: Motorola MC68K #1 Interface Timing

Table 6-9: Motorola MC68K #1 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{CLK}	Bus Clock Frequency		20		50	MHz
T_{CLK}	Bus Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t1	Clock pulse width high	22.5		9		ns
t2	Clock pulse width low	22.5		9		ns
t3	A[16:1], M/R# setup to first CLK rising edge where CS# = 0, AS# = 0, UDS# = 0, and LDS# = 0	1		1		ns
t4	A[16:1], M/R# hold from AS# rising edge	0		0		ns
t5	CS# setup to CLK rising edge while CS#, AS#, UDS#/LDS# = 0	0		1		ns
t6	CS# hold from AS# rising edge	0		0		ns
t7a	AS# asserted for MCLK = BCLK		8		8	T_{CLK}
t7b	AS# asserted for MCLK = BCLK ÷ 2		11		11	T_{CLK}
t7c	AS# asserted for MCLK = BCLK ÷ 3		13		13	T_{CLK}
t7d	AS# asserted for MCLK = BCLK ÷ 4		18		18	T_{CLK}
t8	AS# setup to CLK rising edge while CS#, AS#, UDS#/LDS# = 0	1		1		ns
t9	AS# setup to CLK rising edge	1		2		ns
t10	UDS#/LDS# setup to CLK rising edge while CS#, AS#, UDS#/LDS# = 0	3		1		ns
t11	UDS#/LDS# high setup to CLK rising edge	3		2		ns
t12	First CLK rising edge where AS# = 1 to DTACK# high impedance	5	40	3	14	ns
t13	R/W# setup to CLK rising edge before all CS#, AS#, UDS# and/or LDS# = 0	0		1		ns
t14	R/W# hold from AS# rising edge	0		0		ns
t15	AS# = 0 and CS# = 0 to DTACK# driven high	4	23	3	13	ns
t16	AS# rising edge to DTACK# rising edge	6	39	4	16	ns
t17	D[15:0] valid to third CLK rising edge where CS# = 0, AS# = 0 and either UDS# = 0 or LDS# = 0 (write cycle) (see note 1)	1		0		ns
t18	D[15:0] hold from DTACK# falling edge (write cycle)	0		0		ns
t19	UDS# = 0 and/or LDS# = 0 to D[15:0] driven (read cycle)	4	27	3	13	ns
t20	DTACK# falling edge to D[15:0] valid (read cycle)		0		2	ns
t21	UDS#, LDS# rising edge to D[15:0] high impedance (read cycle)	5	33	3	13	ns

1. t17 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.6 Motorola MC68K #2 Interface Timing (e.g. MC68030)

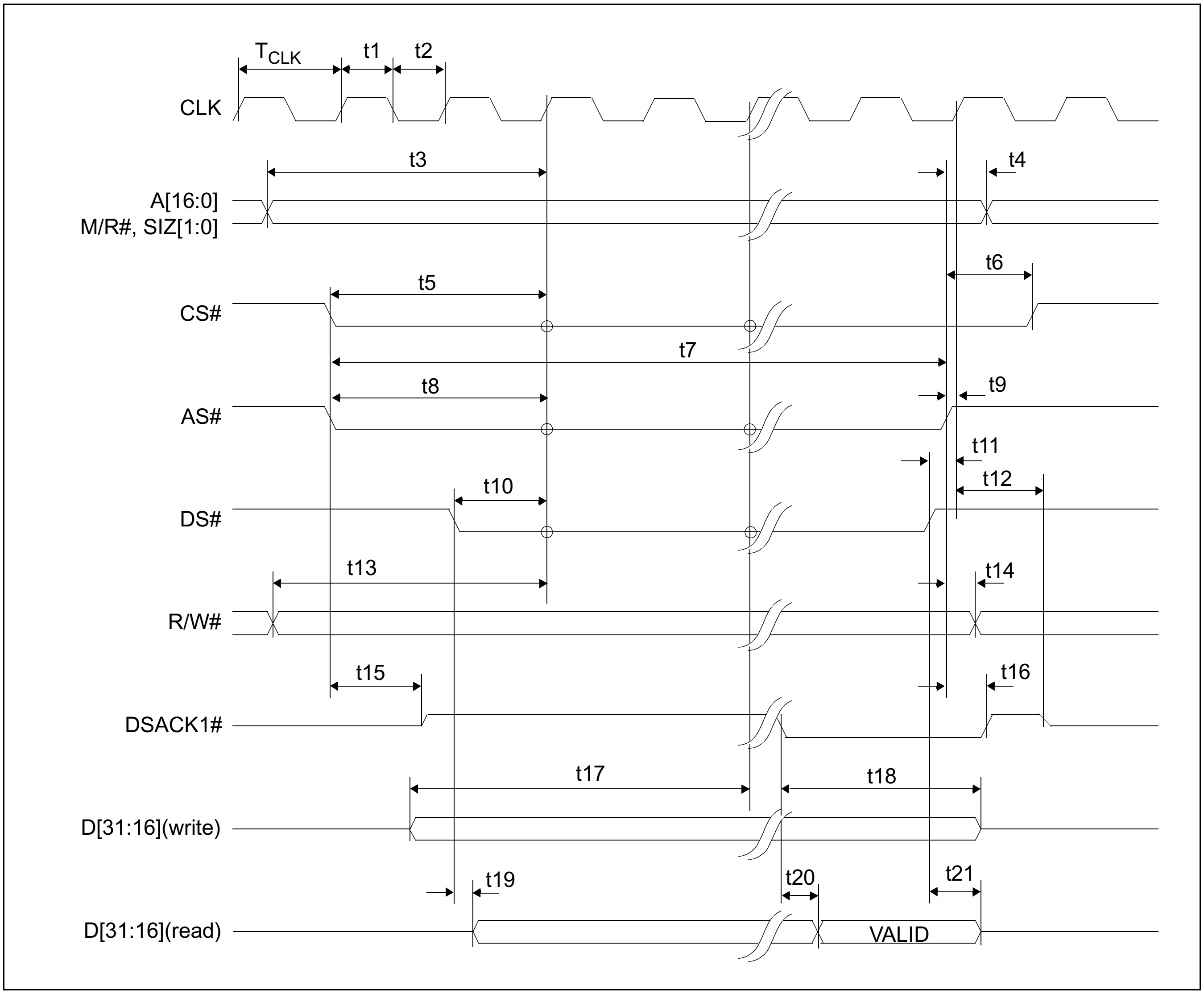


Figure 6-7: Motorola MC68K #2 Interface Timing

Note

For information on the implementation of the Motorola 68K #2 Host Bus Interface, see *Interfacing To The Motorola MC68030 Microprocessor*, document number X31B-G-013-xx.

Table 6-10: Motorola MC68K #2 Interface Timing

Symbol	Parameter	2.0V		3.3V		Unit
		Min	Max	Min	Max	
f_{CLK}	Bus Clock frequency		20		50	MHz
T_{CLK}	Bus Clock period	$1/f_{CLK}$		$1/f_{CLK}$		ns
t1	Clock pulse width high	22.5		9		ns
t2	Clock pulse width low	22.5		9		ns
t3	A[16:0], SIZ[1:0], M/R# setup to first CLK rising edge where CS# = 0, AS# = 0, DS# = 0	1		1		ns
t4	A[16:0], SIZ[1:0], M/R# hold from AS# rising edge	0		0		ns
t5	CS# setup to CLK rising edge	0		1		ns
t6	CS# hold from AS# rising edge	0		0		ns
t7a	AS# asserted for MCLK = BCLK		8		8	T_{CLK}
t7b	AS# asserted for MCLK = BCLK ÷ 2		11		11	T_{CLK}
t7c	AS# asserted for MCLK = BCLK ÷ 3		13		13	T_{CLK}
t7d	AS# asserted for MCLK = BCLK ÷ 4		18		18	T_{CLK}
t8	AS# falling edge to CLK rising edge	1		1		ns
t9	AS# rising edge to CLK rising edge	1		3		ns
t10	DS# falling edge to CLK rising edge	1		1		ns
t11	DS# setup to CLK rising edge	1		3		ns
t12	First CLK where AS# = 1 to DSACK1# high impedance	5	40	3	14	ns
t13	R/W# setup to CLK rising edge before all CS# = 0, AS# = 0, and DS# = 0	1		1		ns
t14	R/W# hold from AS# rising edge	0		0		ns
t15	AS# = 0 and CS# = 0 to DSACK1# rising edge	4	23	3	14	ns
t16	AS# rising edge to DSACK1# rising edge	6	39	4	17	ns
t17	D[31:16] valid to third CLK rising edge where CS# = 0, AS# = 0, and DS# = 0 (write cycle) (see note 1)	1		0		ns
t18	D[31:16] hold from falling edge of DSACK1# (write cycle)	0		0		ns
t19	DS# falling edge to D[31:16] driven (read cycle)	4	32	3	14	ns
t20	DSACK1# falling edge to D[31:16] valid (read cycle)		0		2	ns
t21	DS# rising edge to D[31:16] invalid/high impedance (read cycle)	5	36	3	13	ns

1. t17 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.7 Motorola REDCAP2 Interface Timing

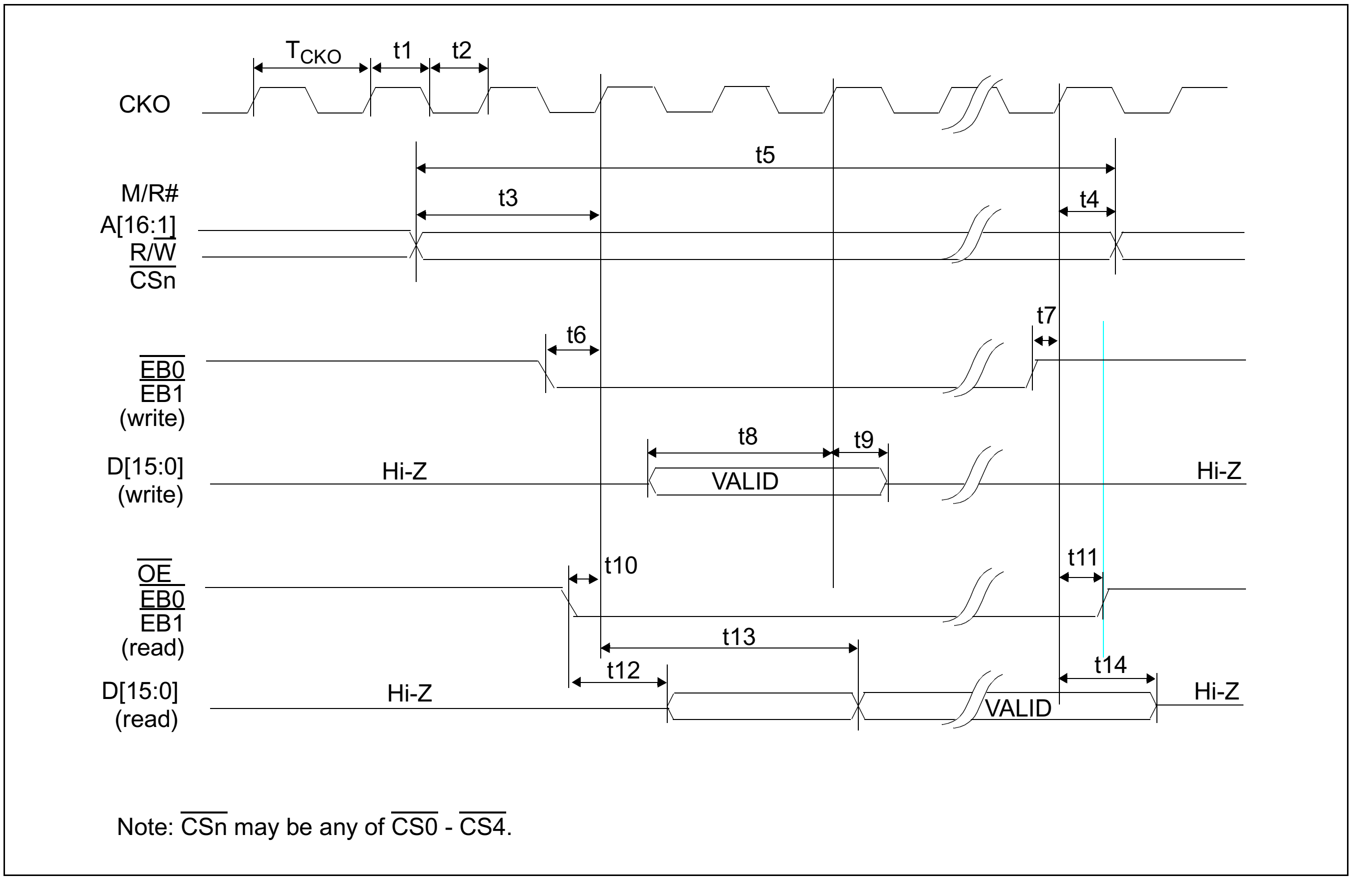


Figure 6-8: Motorola REDCAP2 Interface Timing

Note

For further information on implementing the REDCAP2 microprocessor, see *Interfacing to the Motorola REDCAP2 DSP with Integrated MCU*, document number X31B-G-013-xx.

Table 6-11: Motorola REDCAP2 Interface Timing

Symbol	Parameter	2.0V		3.3V		Units
		Min	Max	Min	Max	
f_{CKO}	Bus Clock frequency		17		17	MHz
T_{CKO}	Bus Clock period	$1/f_{CKO}$		$1/f_{CKO}$		ns
t1	Bus Clock pulse width low	26		26		ns
t2	Bus Clock pulse width high	26		26		ns
t3	A[16:1], M/R#, R/$\overline{W}$, $\overline{CSn}$ setup to CKO rising edge	1		1		ns
t4	A[16:1], M/R#, R/$\overline{W}$, $\overline{CSn}$ hold from CKO rising edge	0		0		ns
t5a	$\overline{CSn}$ asserted for MCLK = BCLK	8		8		T_{CKO}
t5b	$\overline{CSn}$ asserted for MCLK = BCLK ÷ 2	10		10		T_{CKO}
t5c	$\overline{CSn}$ asserted for MCLK = BCLK ÷ 3	13		13		T_{CKO}
t5d	$\overline{CSn}$ asserted for MCLK = BCLK ÷ 4	15		15		T_{CKO}
t6	$\overline{EB0}$, $\overline{EB1}$ asserted to CKO rising edge (write cycle)	1		1		ns
t7	$\overline{EB0}$, $\overline{EB1}$ de-asserted to CKO rising edge (write cycle)	1		4		ns
t8	D[15:0] input setup to 3rd CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low (write cycle) (see note 1)	1		0		ns
t9	D[15:0] input hold from 3rd CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low (write cycle)	23		8		ns
t10	$\overline{OE}$, $\overline{EB0}$, $\overline{EB1}$ setup to CKO rising edge (read cycle)	1		0		ns
t11	$\overline{OE}$, $\overline{EB0}$, $\overline{EB1}$ hold to CKO rising edge (read cycle)	1		0		ns
t12	D[15:0] output delay from $\overline{OE}$, $\overline{EB0}$, $\overline{EB1}$ falling edge (read cycle)	4	29	3	10	ns
t13a	1st CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low to D[15:0] valid for MCLK = BCLK (read cycle)		4.5CKO + 7		4.5CKO + 20	ns
t13b	1st CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 2 (read cycle)		7CKO + 10		6.5CKO + 20	ns
t13c	1st CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 3 (read cycle)		8.5CKO + 8		9.5CKO + 20	ns
t13d	1st CKO rising edge after $\overline{EB0}$ or $\overline{EB1}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 4 (read cycle)		9CKO + 11		11.5CKO + 20	ns
t14	CKO rising edge to D[15:0] output in Hi-Z (read cycle)	4	31	1	11	ns

1. t8 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.8 Motorola DragonBall Interface Timing with $\overline{\text{DTACK}}$ (e.g. MC68EZ328/MC68VZ328)

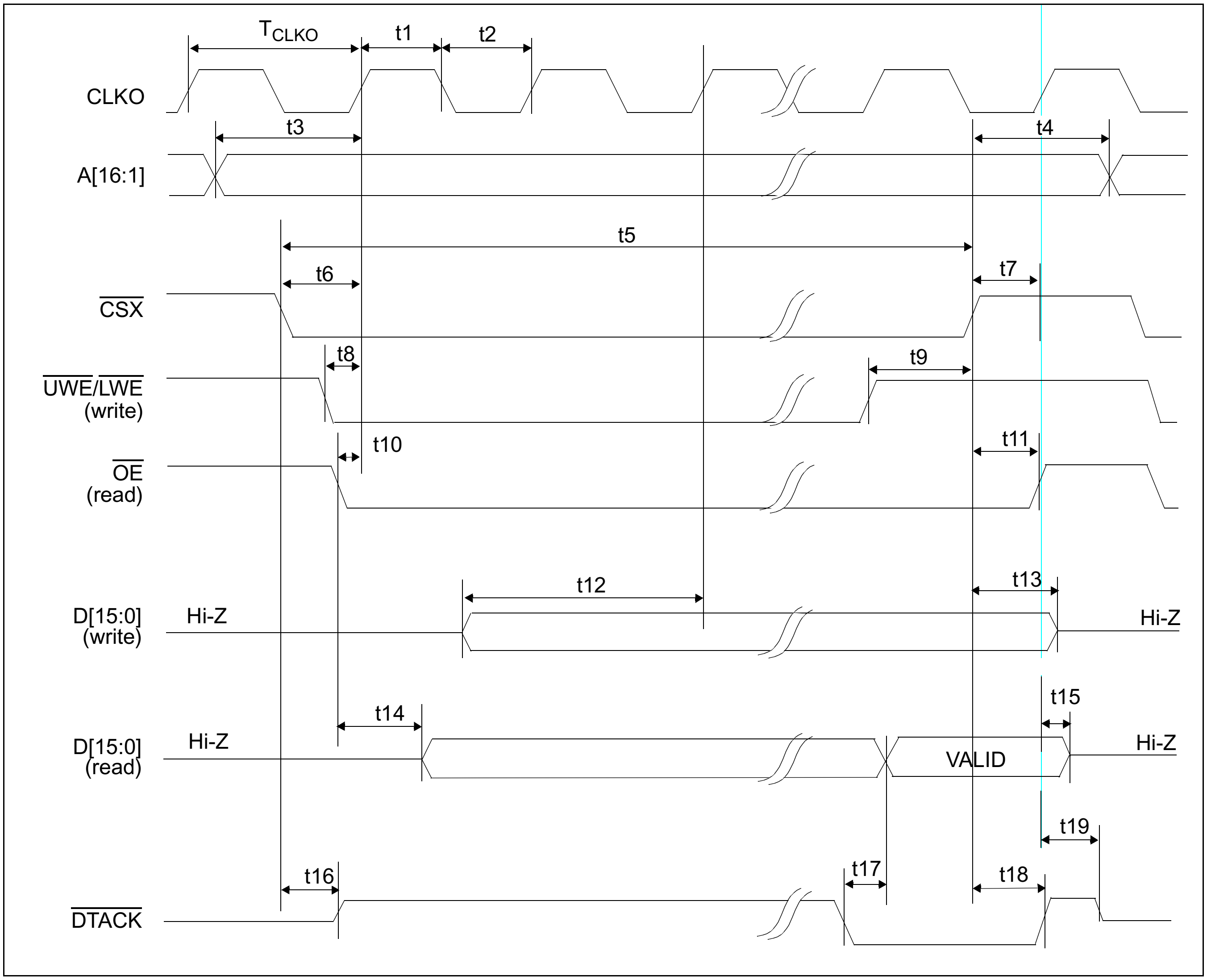


Figure 6-9: Motorola DragonBall Interface with $\overline{\text{DTACK}}$ Timing

Table 6-12: Motorola DragonBall Interface with $\overline{DTACK}$ Timing

Symbol	Parameter	MC68EZ328				MC68VZ328				Unit
		2.0V		3.3V		2.0V		3.3V		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CLKO}	Bus Clock frequency		16		16		20		33	MHz
T_{CLKO}	Bus Clock period	$1/f_{CLKO}$		$1/f_{CLKO}$		$1/f_{CLKO}$		$1/f_{CLKO}$		ns
t1	Clock pulse width high	28.1		28.1		22.5		13.5		ns
t2	Clock pulse width low	28.1		28.1		22.5		13.5		ns
t3	A[16:1] setup 1st CLKO when $\overline{CSX}$ = 0 and either $\overline{UWE}$/$\overline{LWE}$ or $\overline{OE}$ = 0	0		0		0		0		ns
t4	A[16:1] hold from $\overline{CSX}$ rising edge	0		0		0		0		ns
t5a	$\overline{CSX}$ asserted for MCLK = BCLK		8		8		8		8	T_{CLKO}
t5b	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 2		11		11		11		11	T_{CLKO}
t5c	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 3		13		13		13		13	T_{CLKO}
t5d	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 4		17		17		17		17	T_{CLKO}
t6	$\overline{CSX}$ setup to CLKO rising edge	0		0		0		0		ns
t7	$\overline{CSX}$ rising edge to CLKO rising edge	0		0		0		0		ns
t8	$\overline{UWE}$/$\overline{LWE}$ falling edge to CLKO rising edge	1		0		1		0		ns
t9	$\overline{UWE}$/$\overline{LWE}$ rising edge to $\overline{CSX}$ rising edge	0		0		0		0		ns
t10	$\overline{OE}$ falling edge to CLKO rising edge	1		1		1		1		ns
t11	$\overline{OE}$ hold from $\overline{CSX}$ rising edge	0		0		0		0		ns
t12	D[15:0] setup to 3rd CLKO when $\overline{CSX}$, $\overline{UWE}$/$\overline{LWE}$ asserted (write cycle) (see note 1)	1		0		1		0		ns
t13	D[15:0] in hold from $\overline{CSX}$ rising edge (write cycle)	0		0		0		0		ns
t14	Falling edge of $\overline{OE}$ to D[15:0] driven (read cycle)	4	30	3	15	4	30	3	15	ns
t15	CLKO rising edge to D[15:0] output Hi-Z (read cycle)	4	21	2	12	4	21	2	12	ns
t16	$\overline{CSX}$ falling edge to $\overline{DTACK}$ driven high	3	20	3	13	3	20	3	13	ns
t17	$\overline{DTACK}$ falling edge to D[15:0] valid (read cycle)		0		2		0		2	ns
t18	$\overline{CSX}$ high to $\overline{DTACK}$ high	5	34	3	16	5	34	3	16	ns
t19	CLKO rising edge to $\overline{DTACK}$ Hi-Z	5	40	1	6	5	40	1	6	ns

1. t12 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.2.9 Motorola DragonBall Interface Timing w/o $\overline{\text{DTACK}}$ (e.g. MC68EZ328/MC68VZ328)

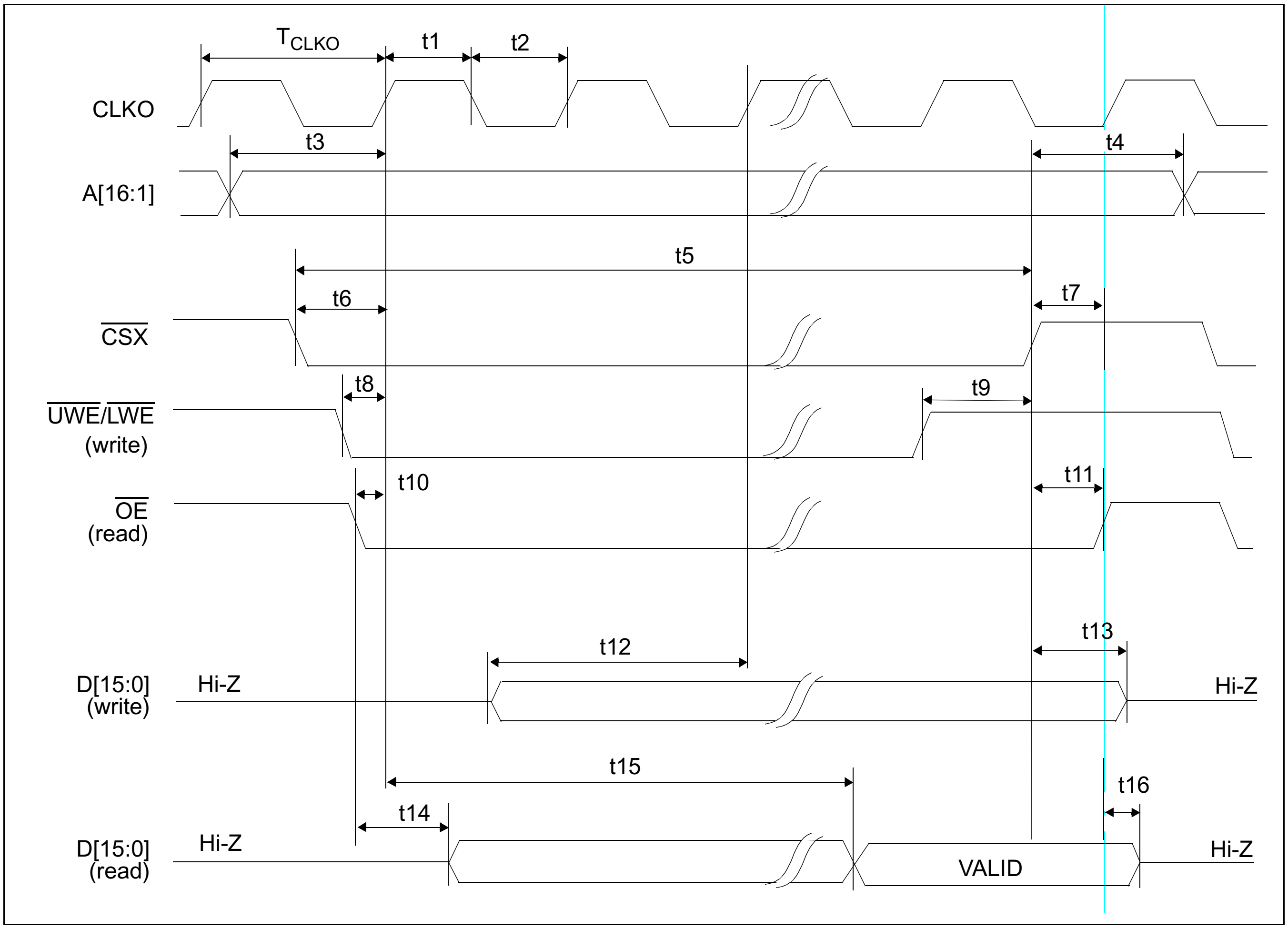


Figure 6-10: Motorola DragonBall Interface without DTACK# Timing

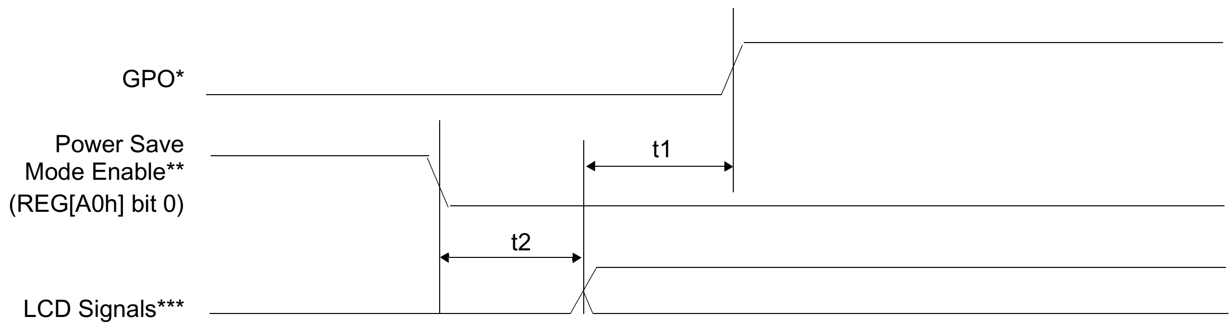
Table 6-13: Motorola DragonBall Interface without $\overline{DTACK}$ Timing

Symbol	Parameter	MC68EZ328				MC68VZ328				Unit
		2.0V		3.3V		2.0V		3.3V		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CLKO}	Bus Clock frequency		16		16		20		33	MHz
T_{CLKO}	Bus Clock period	$1/f_{CLKO}$		$1/f_{CLKO}$		$1/f_{CLKO}$		$1/f_{CLKO}$		ns
t1	Clock pulse width high	28.1		28.1		22.5		13.6		ns
t2	Clock pulse width low	28.1		28.1		22.5		13.6		ns
t3	A[16:1] setup 1st CLKO when $\overline{CSX}$ = 0 and either $\overline{UWE}$/$\overline{LWE}$ or $\overline{OE}$ = 0	0		0		0		0		ns
t4	A[16:1] hold from $\overline{CSX}$ rising edge	0		0		0		0		ns
t5a	$\overline{CSX}$ asserted for MCLK = BCLK (CPU wait state register should be programmed to 4 wait states)		8		8		8		8	T_{CLKO}
t5b	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 2 (CPU wait state register should be programmed to 6 wait states)		11		11		11		11	T_{CLKO}
t5c	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 3 (CPU wait state register should be programmed to 10 wait states)	—	Note 1	—	Note 1		13		13	T_{CLKO}
t5d	$\overline{CSX}$ asserted for MCLK = BCLK ÷ 4 (CPU wait state register should be programmed to 12 wait states)	—	Note 1	—	Note 1		17		17	T_{CLKO}
t6	$\overline{CSX}$ setup to CLKO rising edge	0		0		0		0		ns
t7	$\overline{CSX}$ rising edge setup to CLKO rising edge	0		0		0		0		ns
t8	$\overline{UWE}$/$\overline{LWE}$ setup to CLKO rising edge	1		0		1		0		ns
t9	$\overline{UWE}$/$\overline{LWE}$ rising edge to $\overline{CSX}$ rising edge	0		0		0		0		ns
t10	$\overline{OE}$ setup to CLKO rising edge	1		1		1		1		ns
t11	$\overline{OE}$ hold from $\overline{CSX}$ rising edge	0		0		0		0		ns
t12	D[15:0] setup to 3rd CLKO after $\overline{CSX}$, $\overline{UWE}$/$\overline{LWE}$ asserted (write cycle) (see note 2)	1		0		1		0		ns
t13	$\overline{CSX}$ rising edge to D[15:0] output Hi-Z (write cycle)	0		0		0		0		ns
t14	Falling edge of $\overline{OE}$ to D[15:0] driven (read cycle)	4	30	3	15	4	30	3	15	ns
t15a	1st CLKO rising edge after $\overline{OE}$ and $\overline{CSX}$ asserted low to D[15:0] valid for MCLK = BCLK (read cycle)		$5.5T_{CLKO} + 4$		$5.5T_{CLKO} + 20$		$5.5T_{CLKO} + 4$		$5.5T_{CLKO} + 20$	ns
t15b	1st CLKO rising edge after $\overline{OE}$ and $\overline{CSX}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 2 (read cycle)		$8T_{CLKO} + 19$		$8.5T_{CLKO} + 20$		$8T_{CLKO} + 19$		$8.5T_{CLKO} + 20$	ns
t15c	1st CLKO rising edge after $\overline{OE}$ and $\overline{CSX}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 3 (read cycle)		$9.5T_{CLKO} + 17$		$10.5T_{CLKO} + 20$		$9.5T_{CLKO} + 17$		$10.5T_{CLKO} + 20$	ns
t15d	1st CLKO rising edge after $\overline{OE}$ and $\overline{CSX}$ asserted low to D[15:0] valid for MCLK = BCLK ÷ 4 (read cycle)		$13T_{CLKO} + 9$		$14.5T_{CLKO} + 20$		$13T_{CLKO} + 9$		$14.5T_{CLKO} + 20$	ns
t16	CLKO rising edge to D[15:0] output Hi-Z (read cycle)	4	21	2	12	4	21	2	12	ns

1. The MC68EZ328 cannot support the MCLK = BCLK ÷ 3 and MCLK = BCLK ÷ 4 settings without $\overline{\text{DTACK}}$.
2. t12 is the delay from when data is placed on the bus until the data is latched into the write buffer.

6.3 LCD Power Sequencing

6.3.1 Passive/TFT Power-On Sequence



*It is recommended to use the general purpose output pin GPO to control the LCD bias power.
**The LCD power-on sequence is activated by programming the Power Save Mode Enable bit (REG[A0h] bit 0) to 0.
***LCD Signals include: FPDAT[17:0], FPSHIFT, FPLINE, FPFRAME, and DRDY.

Figure 6-11: Passive/TFT Power-On Sequence Timing

Table 6-14: Passive/TFT Power-On Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	LCD signals active to LCD bias active	Note 1	Note 1	
t2	Power Save Mode disabled to LCD signals active	0	20	ns

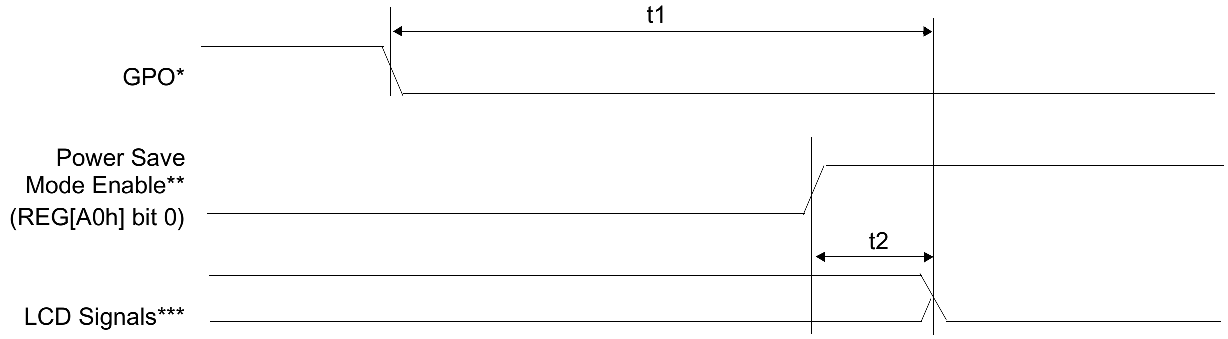
1. t1 is controlled by software and must be determined from the bias power supply delay requirements of the panel connected.

Note

For HR-TFT Power-On/Off sequence information, see *Connecting to the Sharp HR-TFT Panels*, document number X31B-G-011-xx.

For D-TFD Power-On/Off sequence information, see *Connecting to the Epson D-TFD Panels*, document number X31B-G-012-xx.

6.3.2 Passive/TFT Power-Off Sequence



*It is recommended to use the general purpose output pin GPO to control the LCD bias power.
**The LCD power-off sequence is activated by programming the Power Save Mode Enable bit (REG[A0h] bit 0) to 1.
***LCD Signals include: FPDAT[17:0], FPSHIFT, FPLINE, FPFRAME, and DRDY.

Figure 6-12: Passive/TFT Power-Off Sequence Timing

Table 6-15: Passive/TFT Power-Off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	LCD bias deactivated to LCD signals inactive	Note 1	Note 1	
t2	Power Save Mode enabled to LCD signals low	0	20	ns

1. t1 is controlled by software and must be determined from the bias power supply delay requirements of the panel connected.

6.4 Display Interface

The timing parameters required to drive a flat panel display are shown below. Timing details for each supported panel type are provided in the remainder of this section.

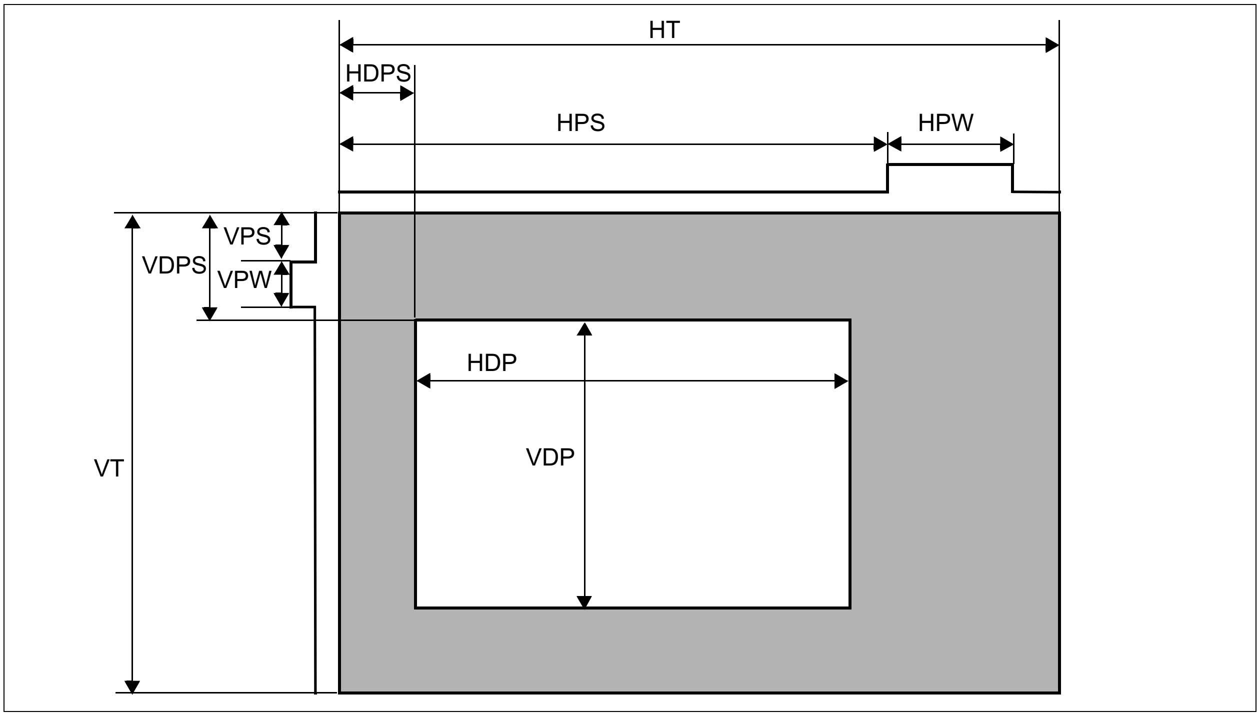


Figure 6-13: Panel Timing Parameters

Table 6-16: Panel Timing Parameter Definition and Register Summary

Symbol	Description	Derived From	Units
HT	Horizontal Total	((REG[12h] bits 6-0) + 1) x 8	Ts
HDP[1]	Horizontal Display Period[1]	((REG[14h] bits 6-0) + 1) x 8	
HDPS	Horizontal Display Period Start Position	For STN panels: ((REG[17h] bits 1-0, REG[16h] bits 7-0) + *22*)	
		For TFT panels: ((REG[17h] bits 1-0, REG[16h] bits 7-0) + *5*)	
HPS	FPLINE Pulse Start Position	(REG[23h] bits 1-0, REG[22h] bits 7-0) + 1	
HPW	FPLINE Pulse Width	(REG[20h] bits 6-0) + 1	
VT	Vertical Total	(REG[19h] bits 1-0, REG[18h] bits 7-0) + 1	Lines (HT)
VDP	Vertical Display Period	(REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1	
VDPS	Vertical Display Period Start Position	REG[1Fh] bits 1-0, REG[1Eh] bits 7-0	
VPS	FPFRAME Pulse Start Position	REG[27h] bits 1-0, REG[26h] bits 7-0	
VPW	FPFRAME Pulse Width	(REG[24h] bits 6-0) + 1	

1. For passive panels, the HDP must be a minimum of 32 pixels and must be increased by multiples of 16. For TFT panels, the HDP must be a minimum of 8 pixels and must be increased by multiples of 8.
2. The following formulas must be valid for all panel timings:
   $HDPS + HDP < HT$
   $VDPS + VDP < VT$

6.4.1 Generic STN Panel Timing

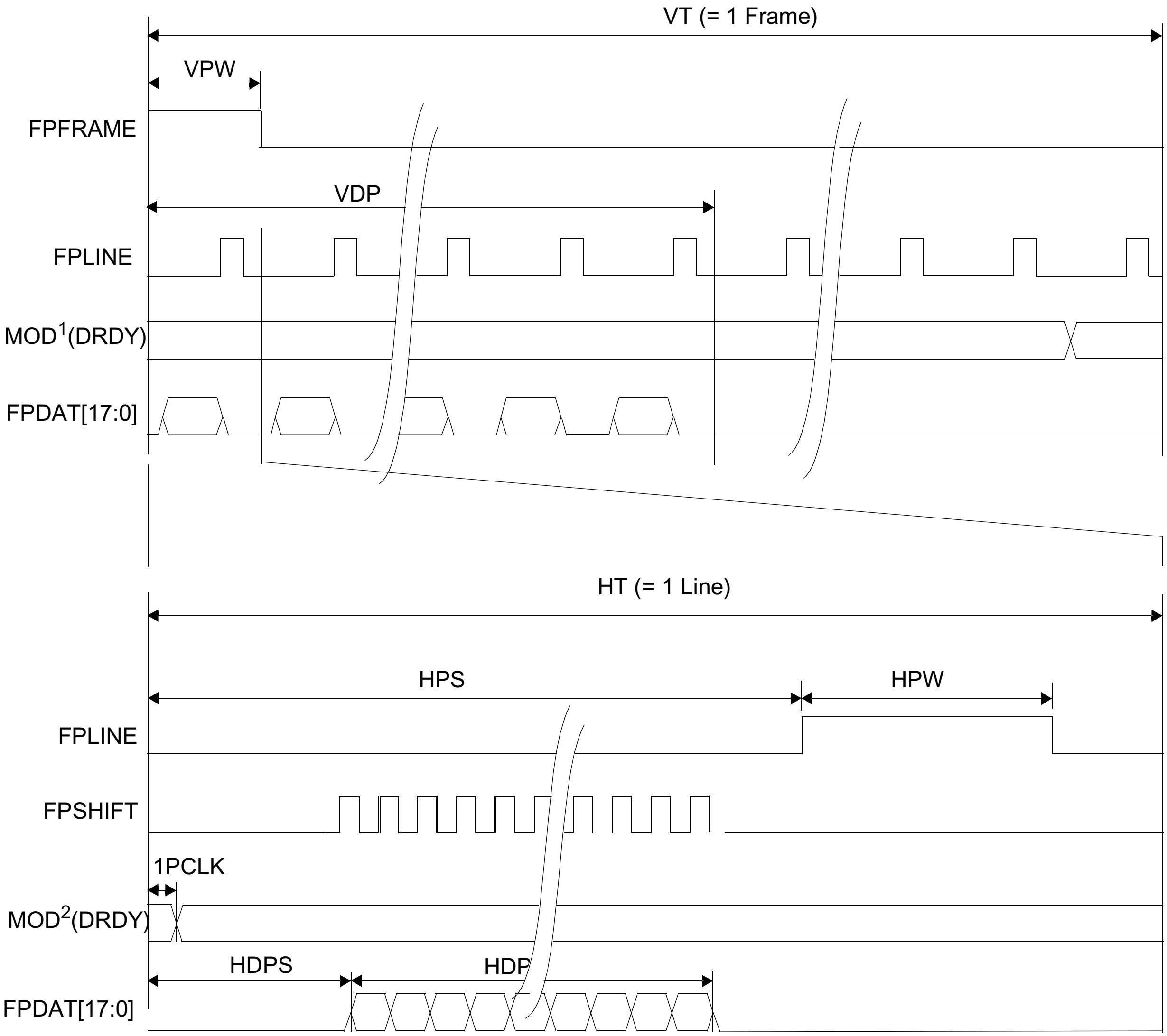


Figure 6-14: Generic STN Panel Timing

VT = Vertical Total
= [(REG[19h] bits 1-0, REG[18h] bits 7-0) + 1] lines
VPS = FPFRAME Pulse Start Position
= 0 lines, because (REG[27h] bits 1-0, REG[26h] bits 7-0) = 0
VPW = FPFRAME Pulse Width
= [(REG[24h] bits 2-0) + 1] lines
VDPS = Vertical Display Period Start Position
= 0 lines, because (REG[1Fh] bits 1-0, REG[1Eh] bits 7-0) = 0
VDP = Vertical Display Period
= [(REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1] lines
HT = Horizontal Total
= [((REG[12h] bits 6-0) + 1) x 8] pixels
HPS = FPLINE Pulse Start Position
= [(REG[23h] bits 1-0, REG[22h] bits 7-0) + 1] pixels
HPW = FPLINE Pulse Width
= [(REG[20h] bits 6-0) + 1] pixels
HDPS = Horizontal Display Period Start Position
= 22 pixels, because (REG[17h] bits 1-0, REG[16h] bits 7-0) = 0
HDP = Horizontal Display Period
= [((REG[14h] bits 6-0) + 1) x 8] pixels

*For passive panels, the HDP must be a minimum of 32 pixels and must be increased by multiples of 16.
*HPS must comply with the following formula:
HPS > HDP + 22
HPS + HPW < HT
*Panel Type Bits (REG[10h] bits 1-0) = 00b (STN)
*FPFRAME Pulse Polarity Bit (REG[24h] bit 7) = 1 (active high)
*FPLINE Polarity Bit (REG[20h] bit 7) = 1 (active high)
*MOD^1 is the MOD signal when (REG[11h] bits 5-0) = 0 (MOD toggles every FPFRAME)
*MOD^2 is the MOD signal when (REG[11h] bits 5-0) = n (MOD toggles every n FPLINE)

6.4.2 Single Monochrome 4-Bit Panel Timing

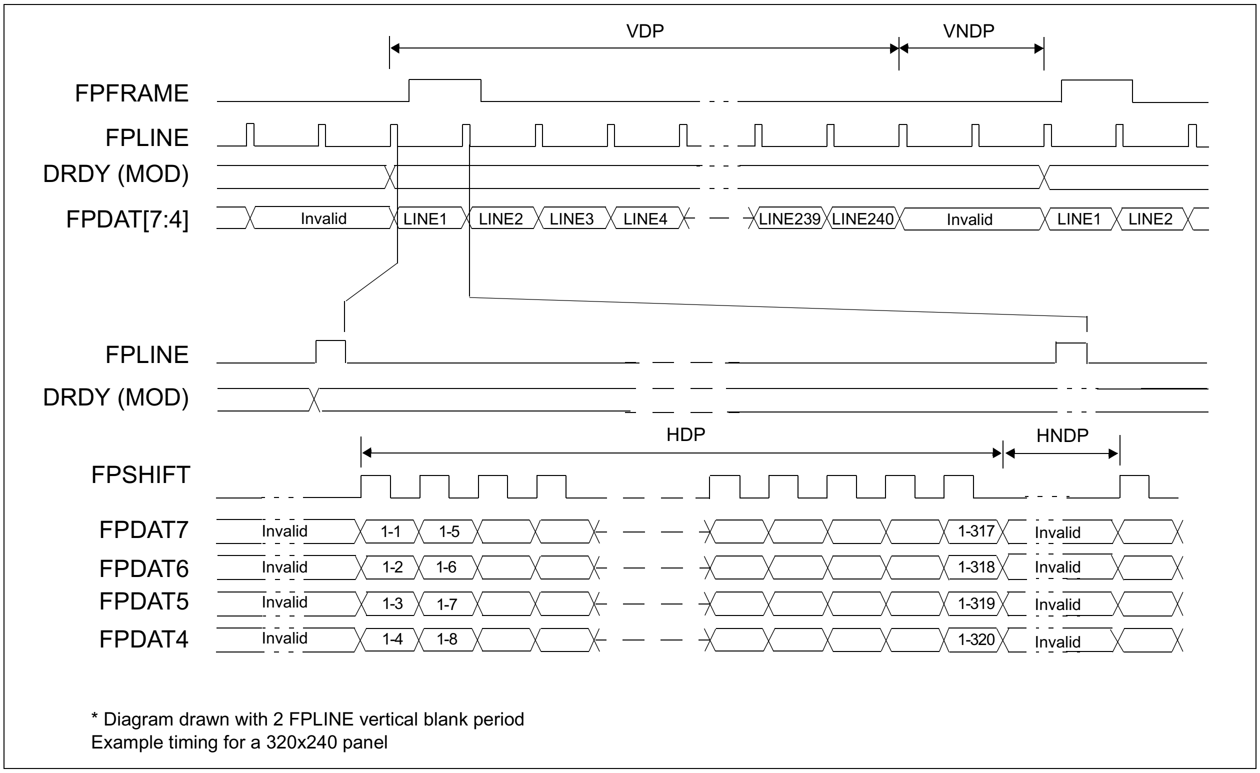


Figure 6-15: Single Monochrome 4-Bit Panel Timing

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines
VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines
HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts
HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

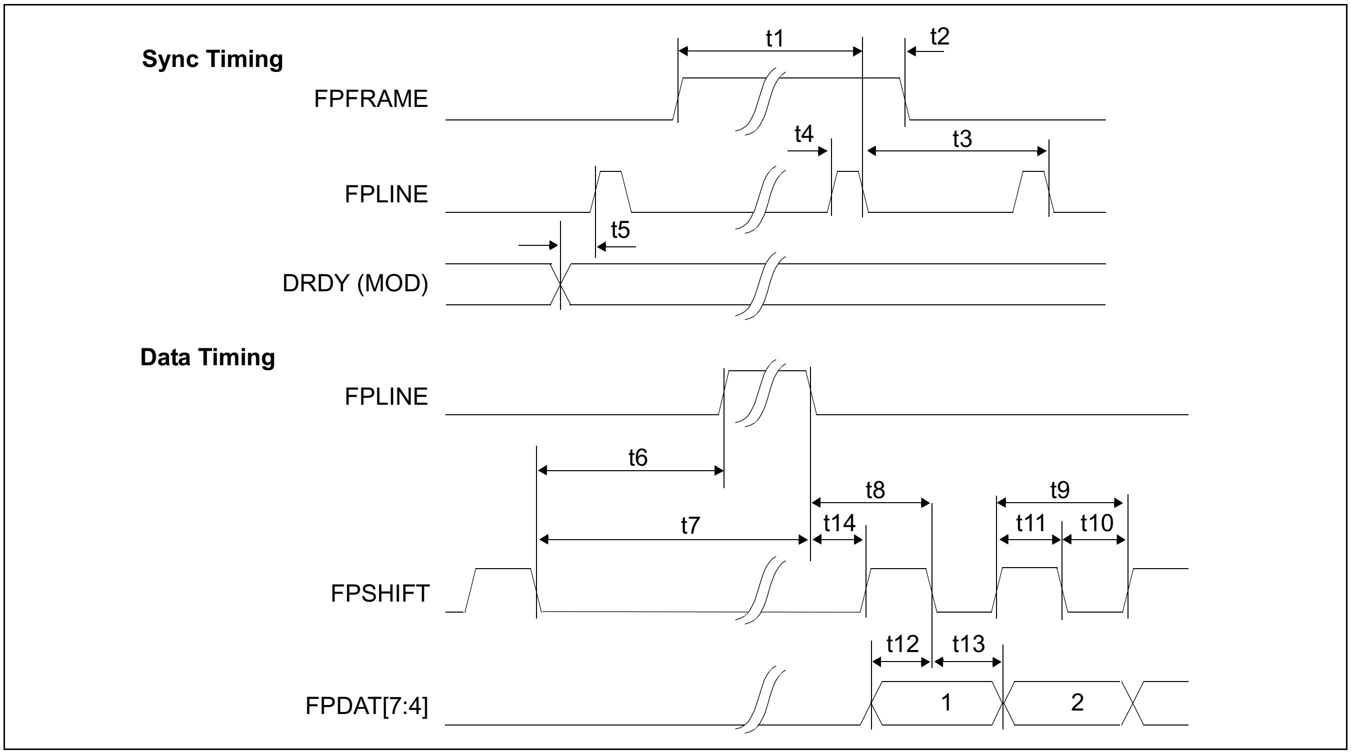


Figure 6-16: Single Monochrome 4-Bit Panel A.C. Timing

Table 6-17: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	4			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPDAT[7:4] setup to FPSHIFT falling edge	1			Ts
t13	FPDAT[7:4] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.4.3 Single Monochrome 8-Bit Panel Timing

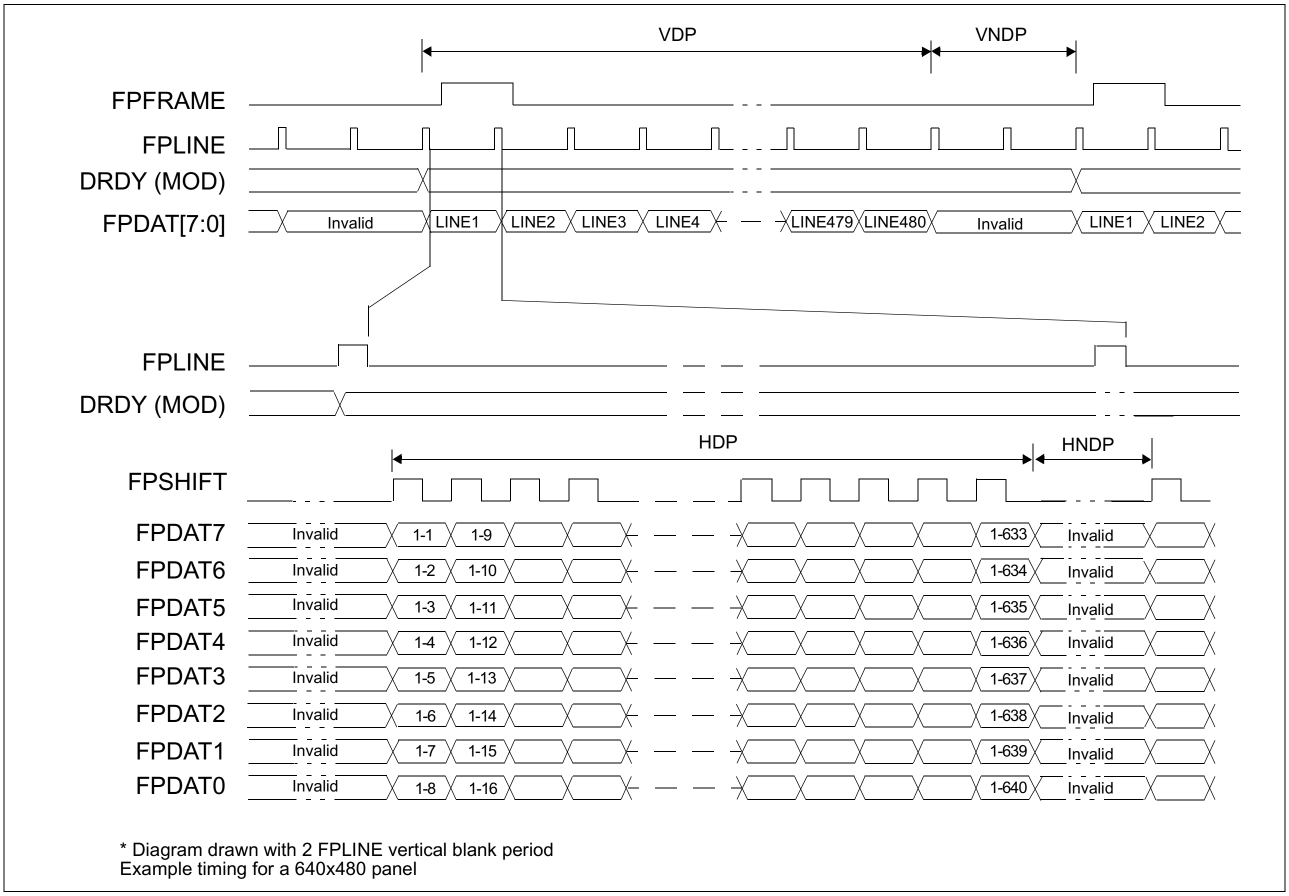


Figure 6-17: Single Monochrome 8-Bit Panel Timing

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines

HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

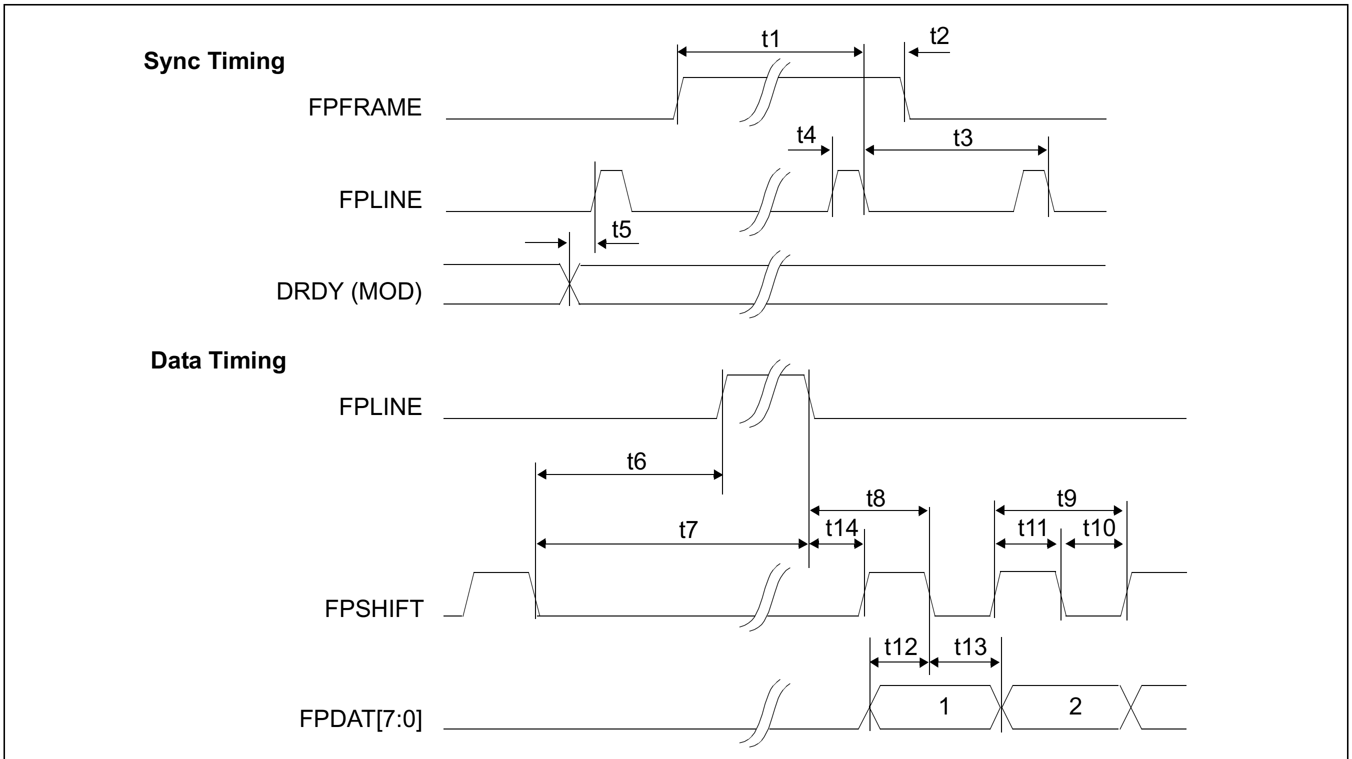


Figure 6-18: Single Monochrome 8-Bit Panel A.C. Timing

Table 6-18: Single Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 4			Ts
t9	FPSHIFT period	8			Ts
t10	FPSHIFT pulse width low	4			Ts
t11	FPSHIFT pulse width high	4			Ts
t12	FPDAT[7:0] setup to FPSHIFT falling edge	4			Ts
t13	FPDAT[7:0] hold to FPSHIFT falling edge	4			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 4, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.4.4 Single Color 4-Bit Panel Timing

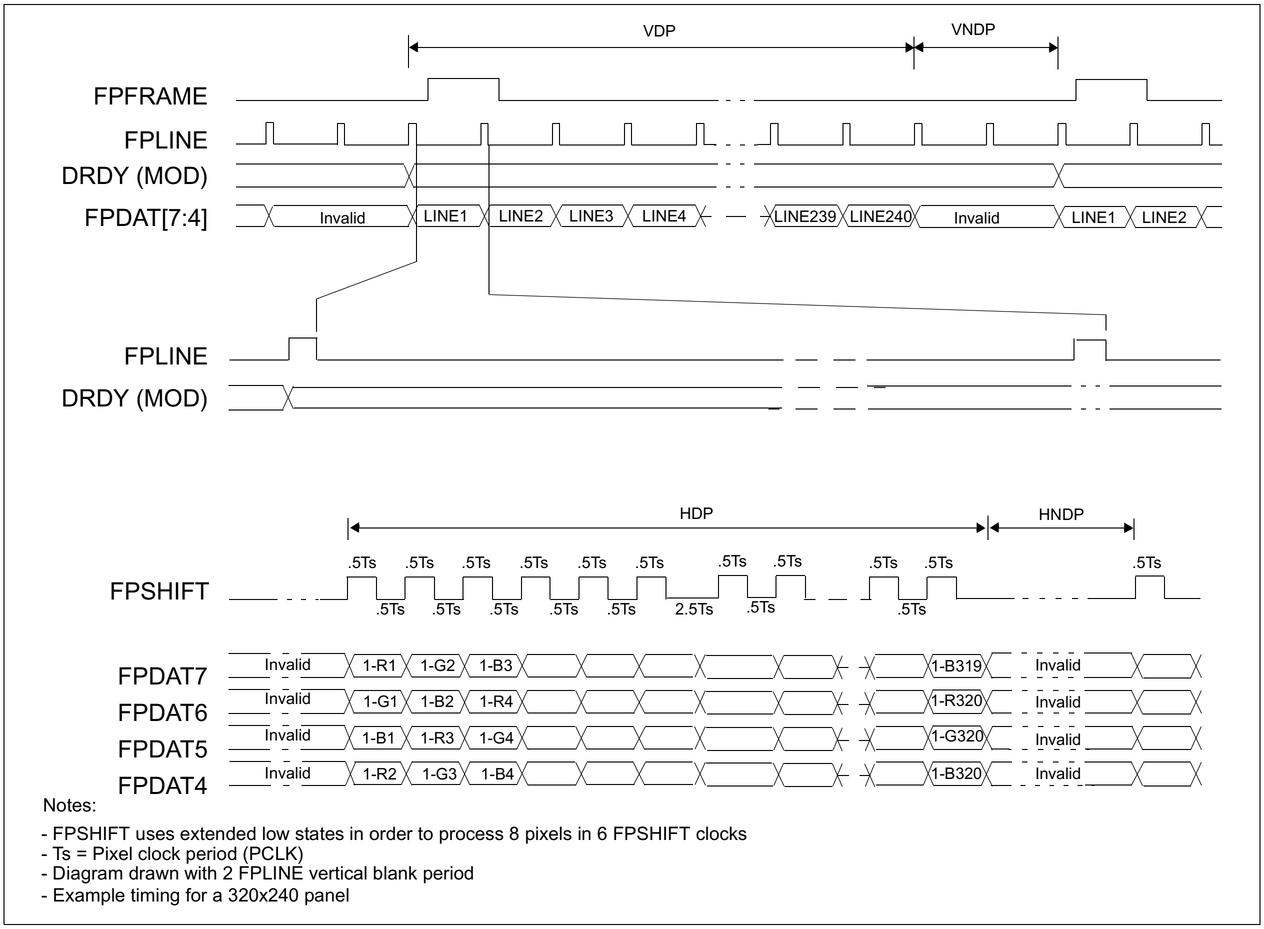


Figure 6-19: Single Color 4-Bit Panel Timing

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines
VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines
HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts
HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

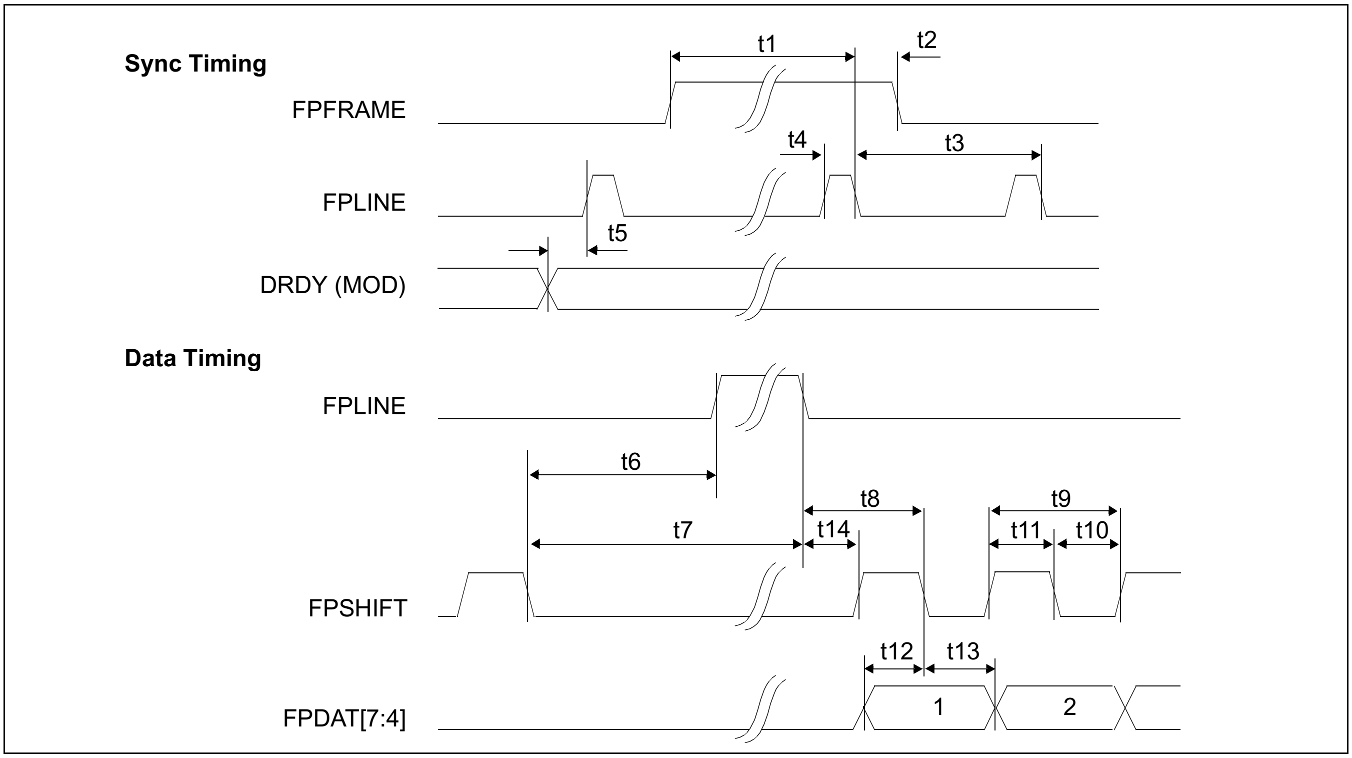


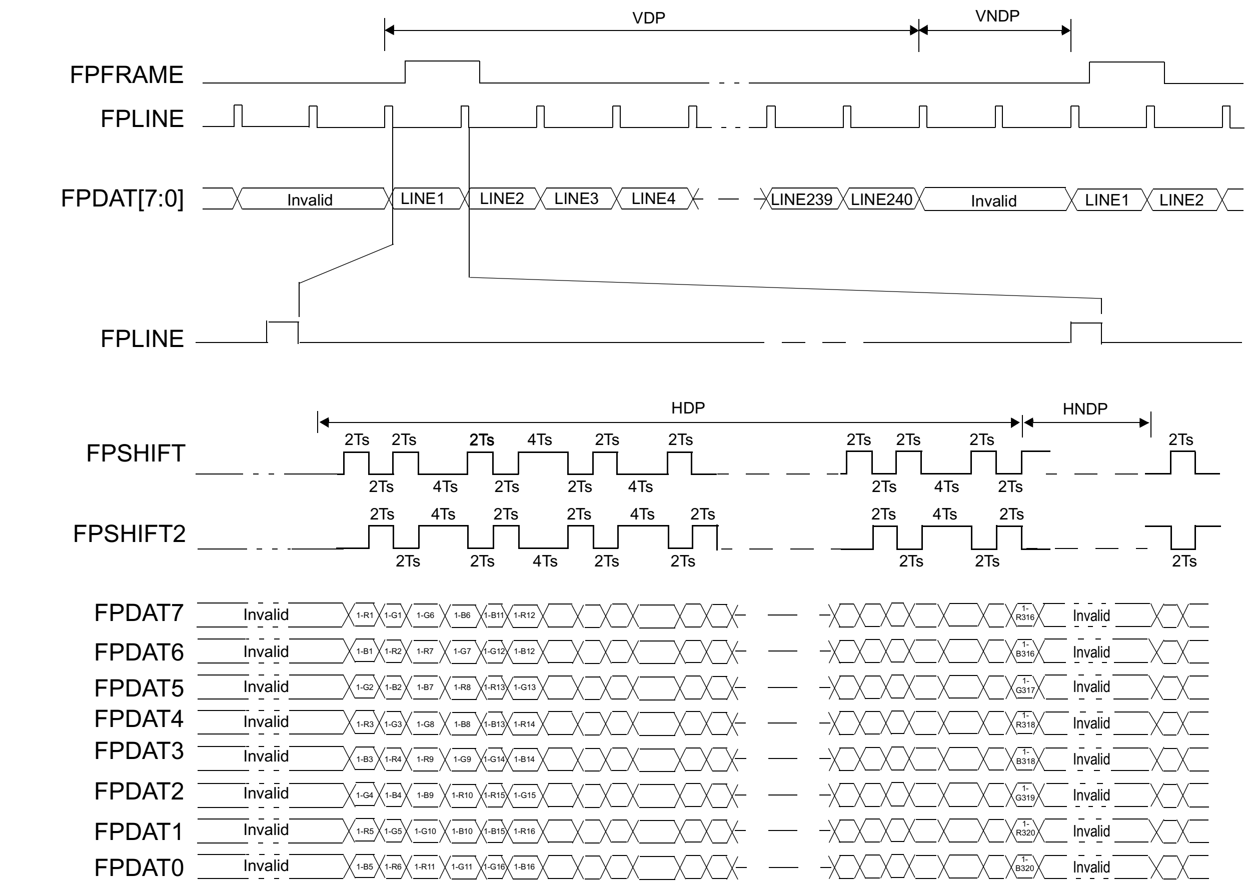
Figure 6-20: Single Color 4-Bit Panel A.C. Timing

Table 6-19: Single Color 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 0.5			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width low	0.5			Ts
t11	FPSHIFT pulse width high	0.5			Ts
t12	FPDAT[7:4] setup to FPSHIFT falling edge	0.5			Ts
t13	FPDAT[7:4] hold to FPSHIFT falling edge	0.5			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 1.5), if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$) + 1, if negative add $t3_{min}$

6.4.5 Single Color 8-Bit Panel Timing (Format 1)



Notes:
- The duty cycle of FPSHIFT changes in order to process 16 pixels in 6 FPSHIFT/FPSHIFT2 rising edges
- Ts = Pixel clock period (PCLK)
- Diagram drawn with 2 FPLINE vertical blank period
- Example timing for a 320x240 panel

Figure 6-21: Single Color 8-Bit Panel Timing (Format 1)

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines
VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines
HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts
HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

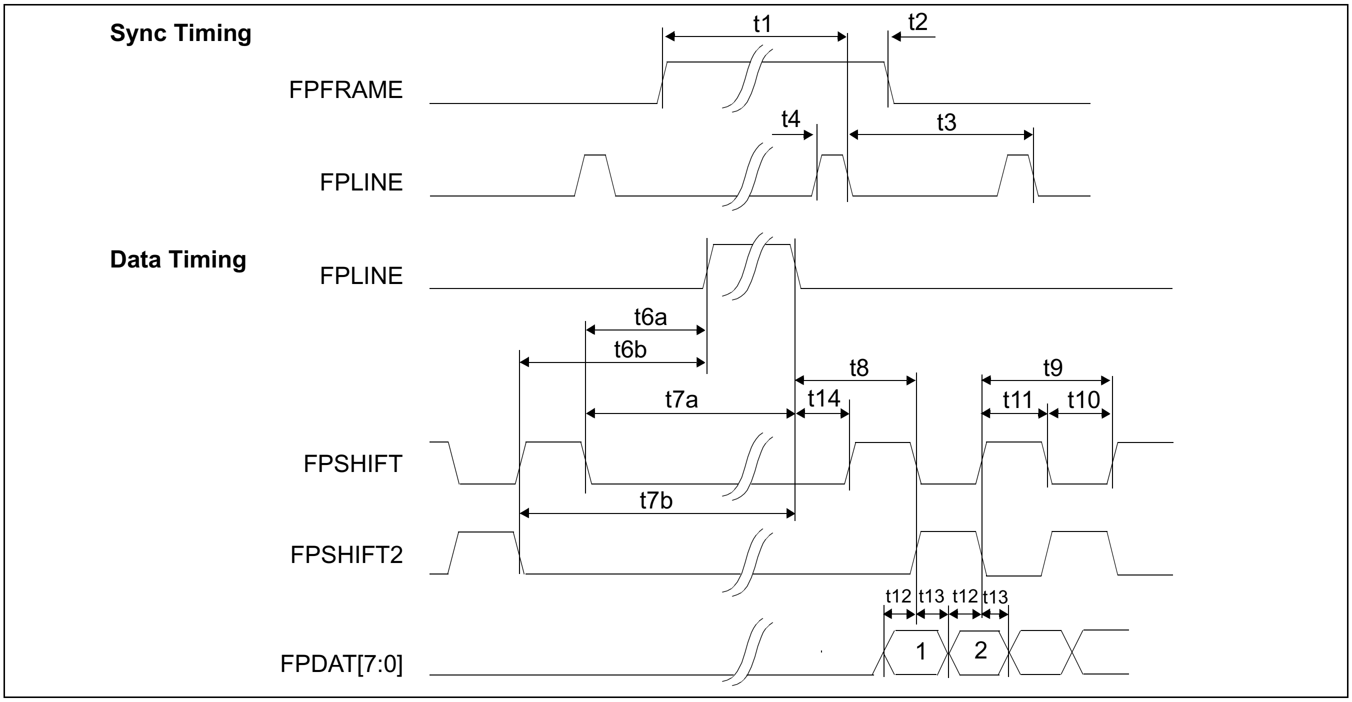


Figure 6-22: Single Color 8-Bit Panel A.C. Timing (Format 1)

Table 6-20: Single Color 8-Bit Panel A.C. Timing (Format 1)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t6a	FPSHIFT falling edge to FPLINE rising edge	note 6			Ts
t6b	FPSHIFT2 falling edge to FPLINE rising edge	note 7			Ts
t7a	FPSHIFT falling edge to FPLINE falling edge	t6a + t4			Ts
t7b	FPSHIFT2 falling edge to FPLINE falling edge	t6b + t4			Ts
t8	FPLINE falling edge to FPSHIFT rising, FPSHIFT2 falling edge	t14 + 2			Ts
t9	FPSHIFT2, FPSHIFT period	4		6	Ts
t10	FPSHIFT2, FPSHIFT pulse width low	2			Ts
t11	FPSHIFT2, FPSHIFT pulse width high	2			Ts
t12	FPDAT[7:0] setup to FPSHIFT2, FPSHIFT falling edge	1			Ts
t13	FPDAT[7:0] hold from FPSHIFT2, FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t6a_{min}$ = HPS - (HDP + HDPS), if negative add $t3_{min}$
7. $t6b_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.4.6 Single Color 8-Bit Panel Timing (Format 2)

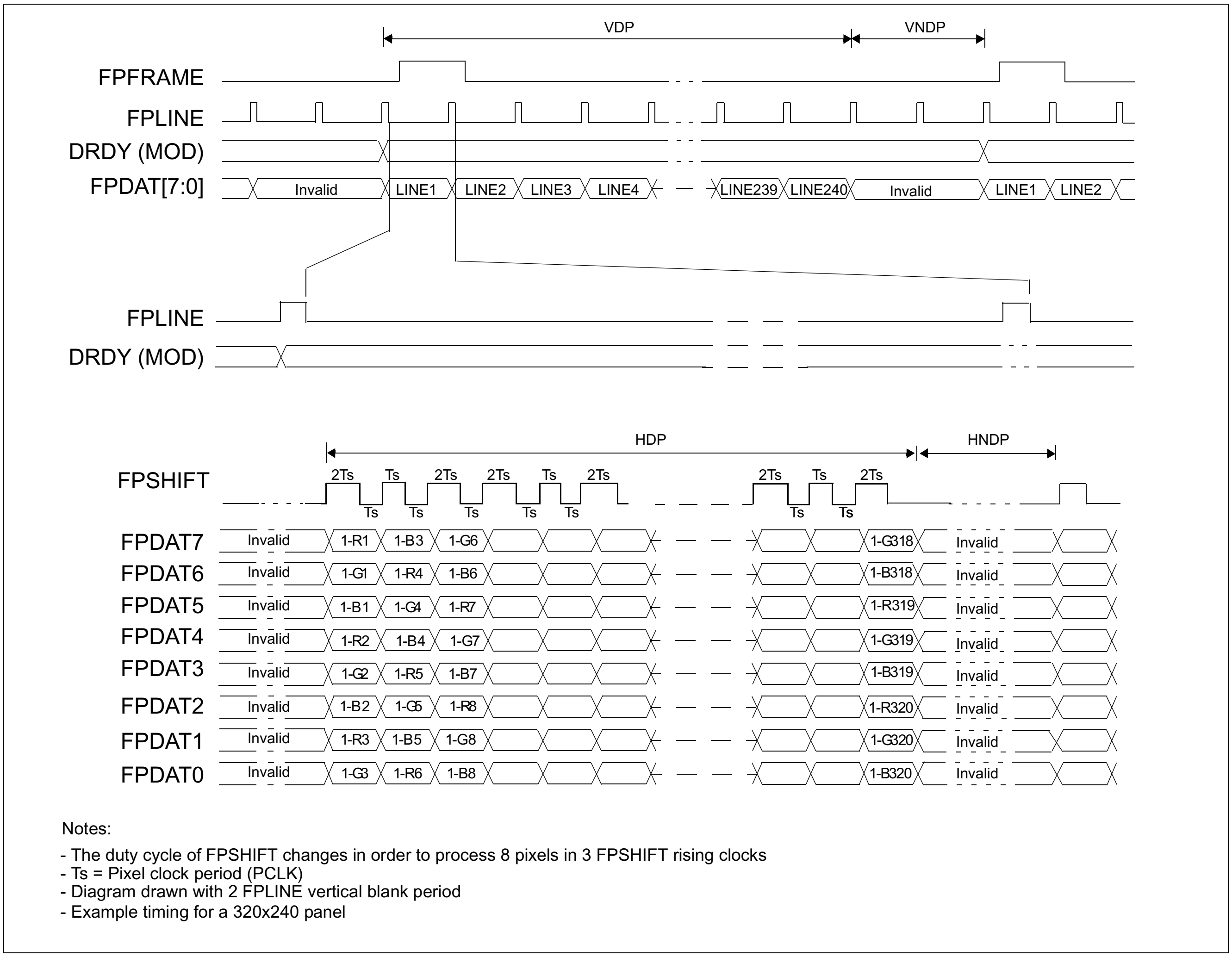


Figure 6-23: Single Color 8-Bit Panel Timing (Format 2)

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines
VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines
HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts
HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

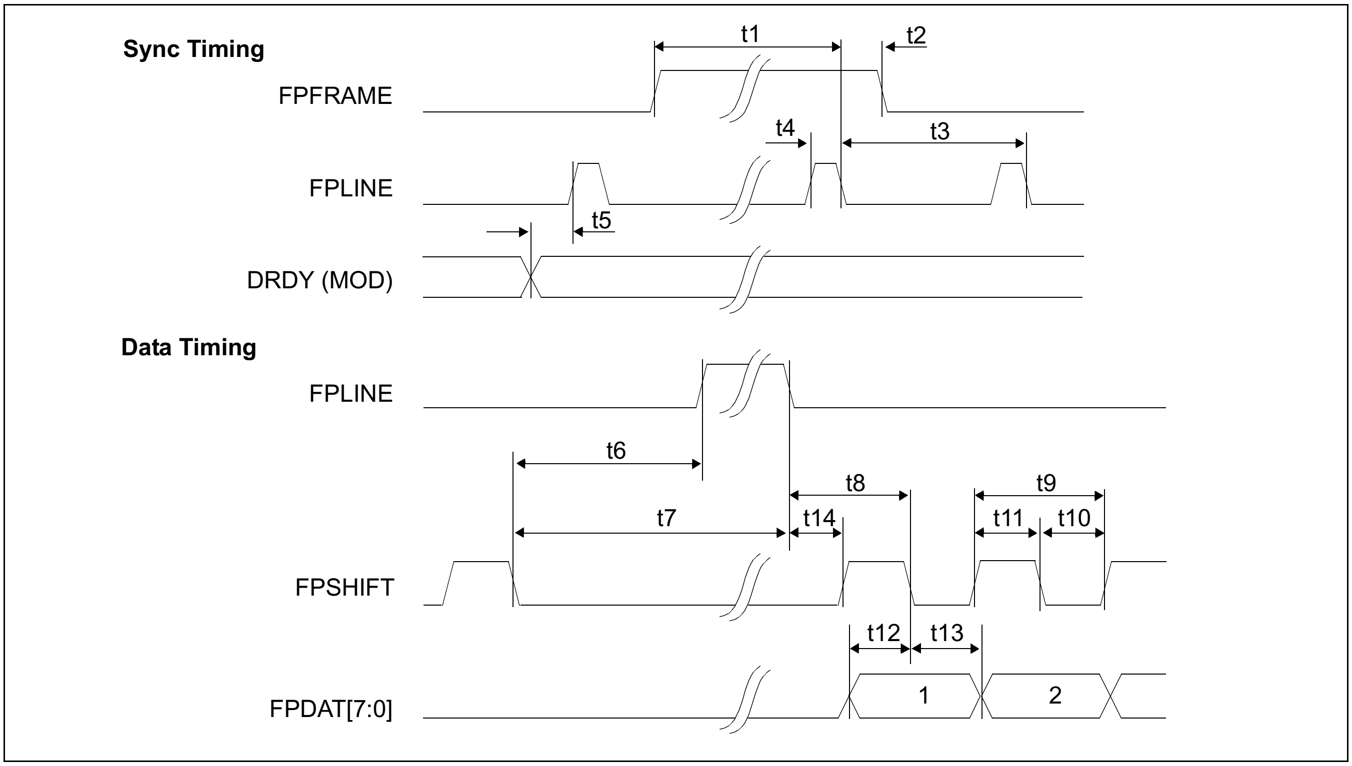


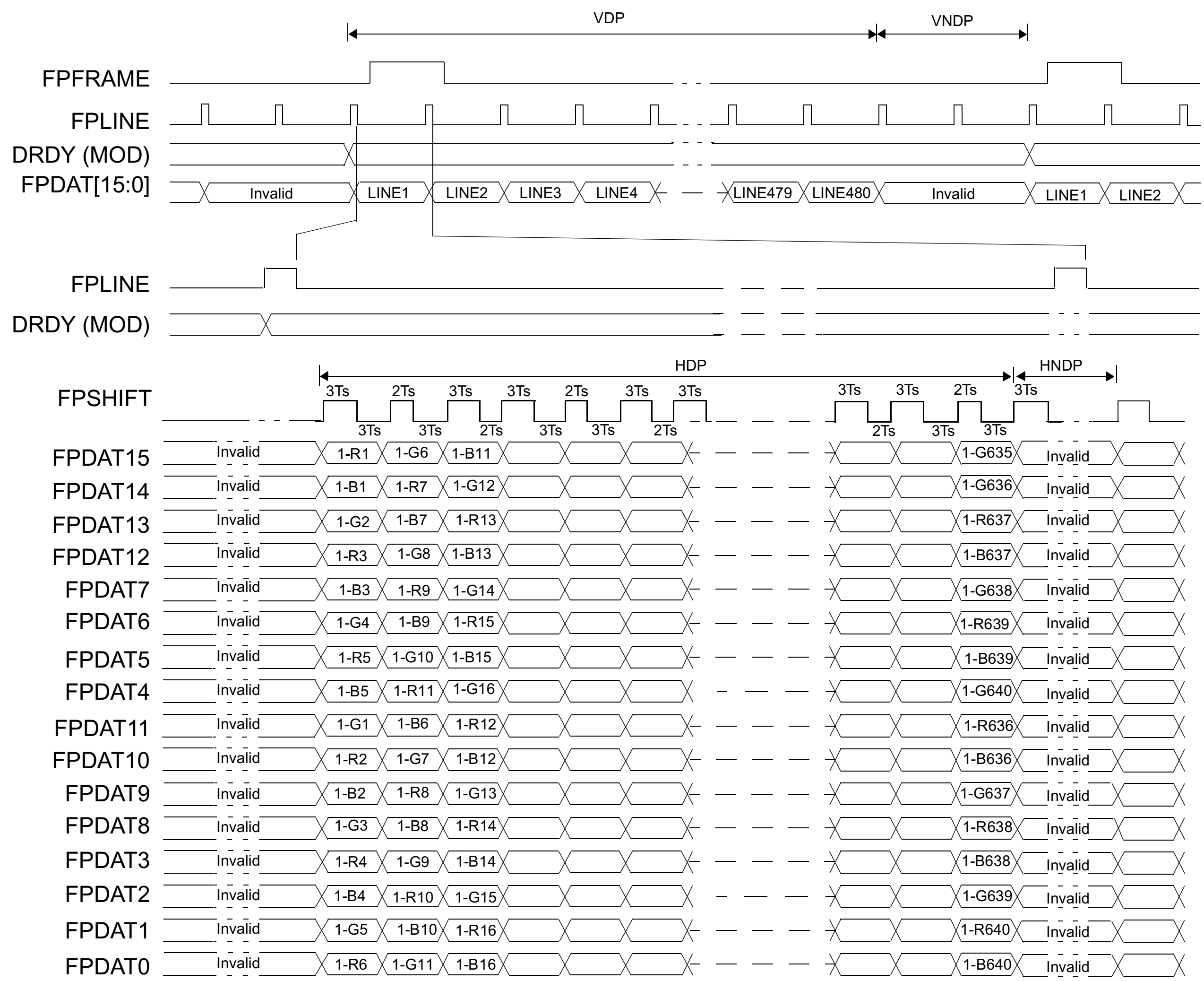
Figure 6-24: Single Color 8-Bit Panel A.C. Timing (Format 2)

Table 6-21: Single Color 8-Bit Panel A.C. Timing (Format 2)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	FPDAT[7:0] setup to FPSHIFT falling edge	1			Ts
t13	FPDAT[7:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 1, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.4.7 Single Color 16-Bit Panel Timing



Notes:

- The duty cycle of FPSHIFT changes in order to process 16 pixels in 3 FPSHIFT rising clocks
- Ts = Pixel clock period (PCLK)
- Diagram drawn with 2 FPLINE vertical blank period
- Example timing for a 640x480 panel

Figure 6-25: Single Color 16-Bit Panel Timing

VDP = Vertical Display Period
= (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1 Lines

VNDP = Vertical Non-Display Period
= VT - VDP
= (REG[19h] bits 1-0, REG[18h] bits 7-0) - (REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) Lines

HDP = Horizontal Display Period
= ((REG[14h] bits 6-0) + 1) x 8Ts

HNDP = Horizontal Non-Display Period
= HT - HDP
= (((REG[12h] bits 6-0) + 1) x 8Ts) - (((REG[14h] bits 6-0) + 1) x 8Ts)

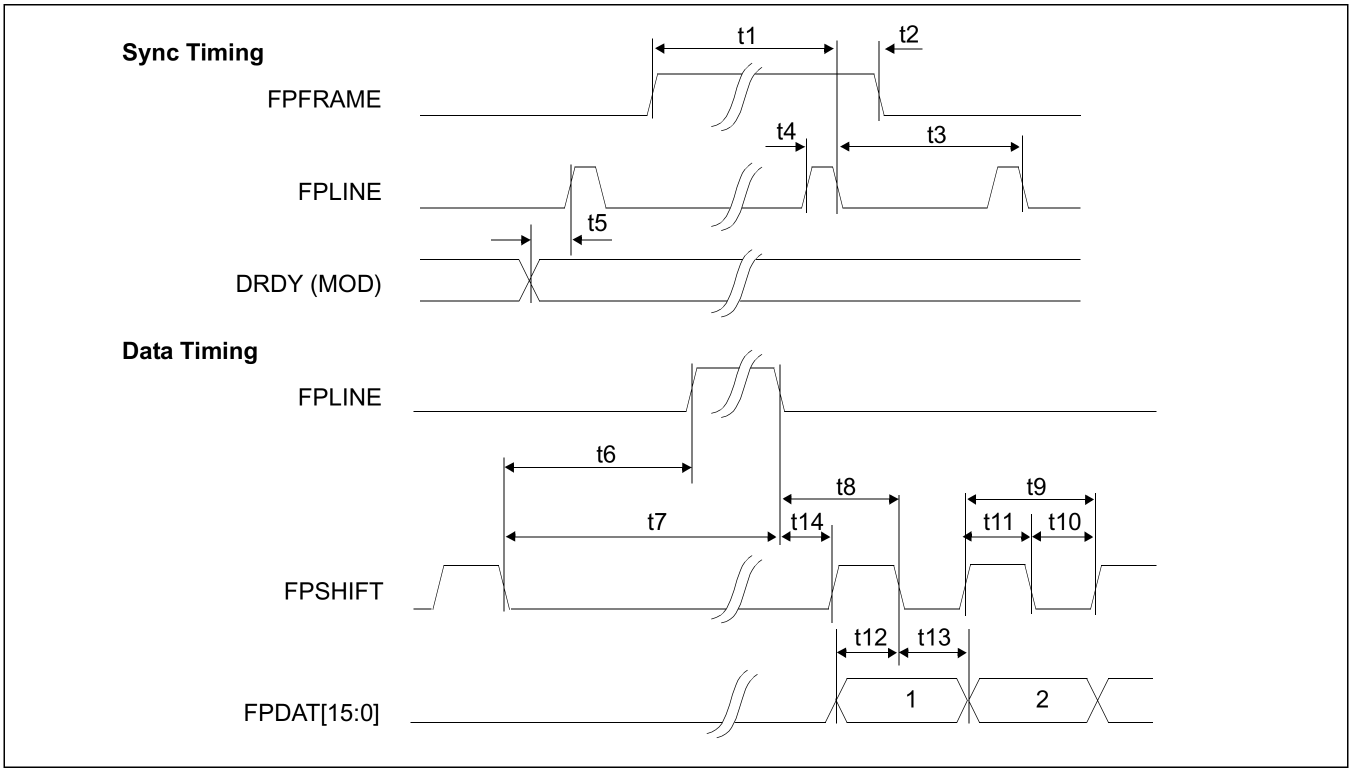


Figure 6-26: Single Color 16-Bit Panel A.C. Timing

Table 6-22: Single Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			Ts (note 1)
t2	FPFRAME hold from FPLINE falling edge	note 3			Ts
t3	FPLINE period	note 4			Ts
t4	FPLINE pulse width	note 5			Ts
t5	MOD transition to FPLINE rising edge	note 6			Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 7			Ts
t7	FPSHIFT falling edge to FPLINE falling edge	t6 + t4			Ts
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 3			Ts
t9	FPSHIFT period	5			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPDAT[15:0] setup to FPSHIFT rising edge	2			Ts
t13	FPDAT[15:0] hold to FPSHIFT rising edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	note 8			Ts

1. Ts = pixel clock period
2. $t1_{min}$ = HPS + $t4_{min}$
3. $t2_{min}$ = $t3_{min}$ - (HPS + $t4_{min}$)
4. $t3_{min}$ = HT
5. $t4_{min}$ = HPW
6. $t5_{min}$ = HPS - 1
7. $t6_{min}$ = HPS - (HDP + HDPS) + 2, if negative add $t3_{min}$
8. $t14_{min}$ = HDPS - (HPS + $t4_{min}$), if negative add $t3_{min}$

6.4.8 Generic TFT Panel Timing

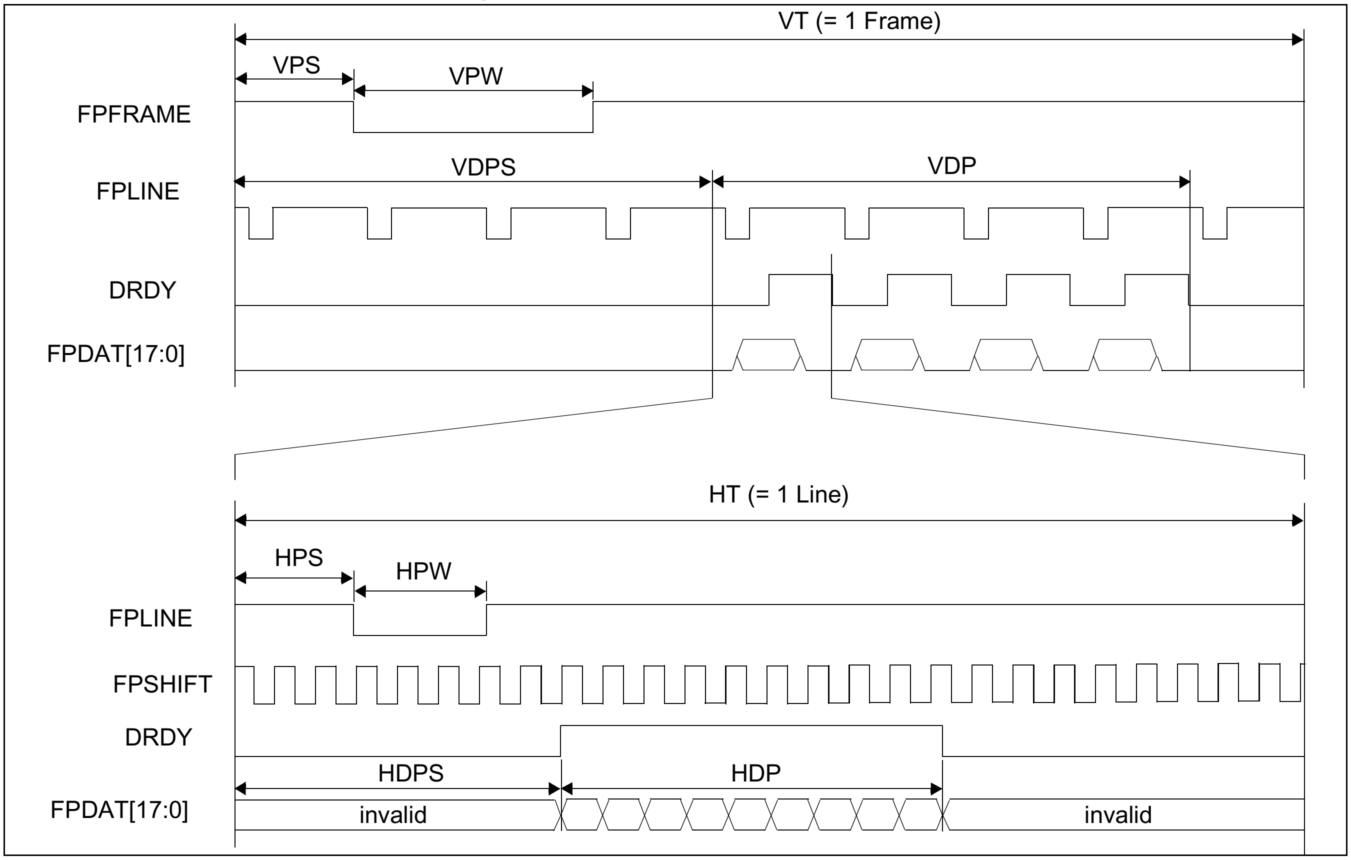


Figure 6-27: Generic TFT Panel Timing

VT	= Vertical Total	= [(REG[19h] bits 1-0, REG[18h] bits 7-0) + 1] lines
VPS	= FPFRAME Pulse Start Position	= (REG[27h] bits 1-0, REG[26h] bits 7-0) lines
VPW	= FPFRAME Pulse Width	= [(REG[24h] bits 2-0) + 1] lines
VDPS	= Vertical Display Period Start Position	= (REG[1Fh] bits 1-0, REG[1Eh] bits 7-0) lines
VDP	= Vertical Display Period	= [(REG[1Dh] bits 1-0, REG[1Ch] bits 7-0) + 1] lines
HT	= Horizontal Total	= [((REG[12h] bits 6-0) + 1) x 8] pixels
HPS	= FPLINE Pulse Start Position	= [(REG[23h] bits 1-0, REG[22h] bits 7-0) + 1] pixels
HPW	= FPLINE Pulse Width	= [(REG[20h] bits 6-0) + 1] pixels
HDPS	= Horizontal Display Period Start Position	= [(REG[17h] bits 1-0, REG[16h] bits 7-0) + 5] pixels
HDP	= Horizontal Display Period	= [((REG[14h] bits 6-0) + 1) x 8] pixels

*For TFT panels, the HDP must be a minimum of 8 pixels and must be increased by multiples of 8.
*Panel Type Bits (REG[10h] bits 1-0) = 01 (TFT)
*FPLINE Pulse Polarity Bit (REG[24h] bit 7) = 0 (active low)
*FPFRAME Polarity Bit (REG[20h] bit 7) = 0 (active low)

6.4.9 9/12/18-Bit TFT Panel Timing

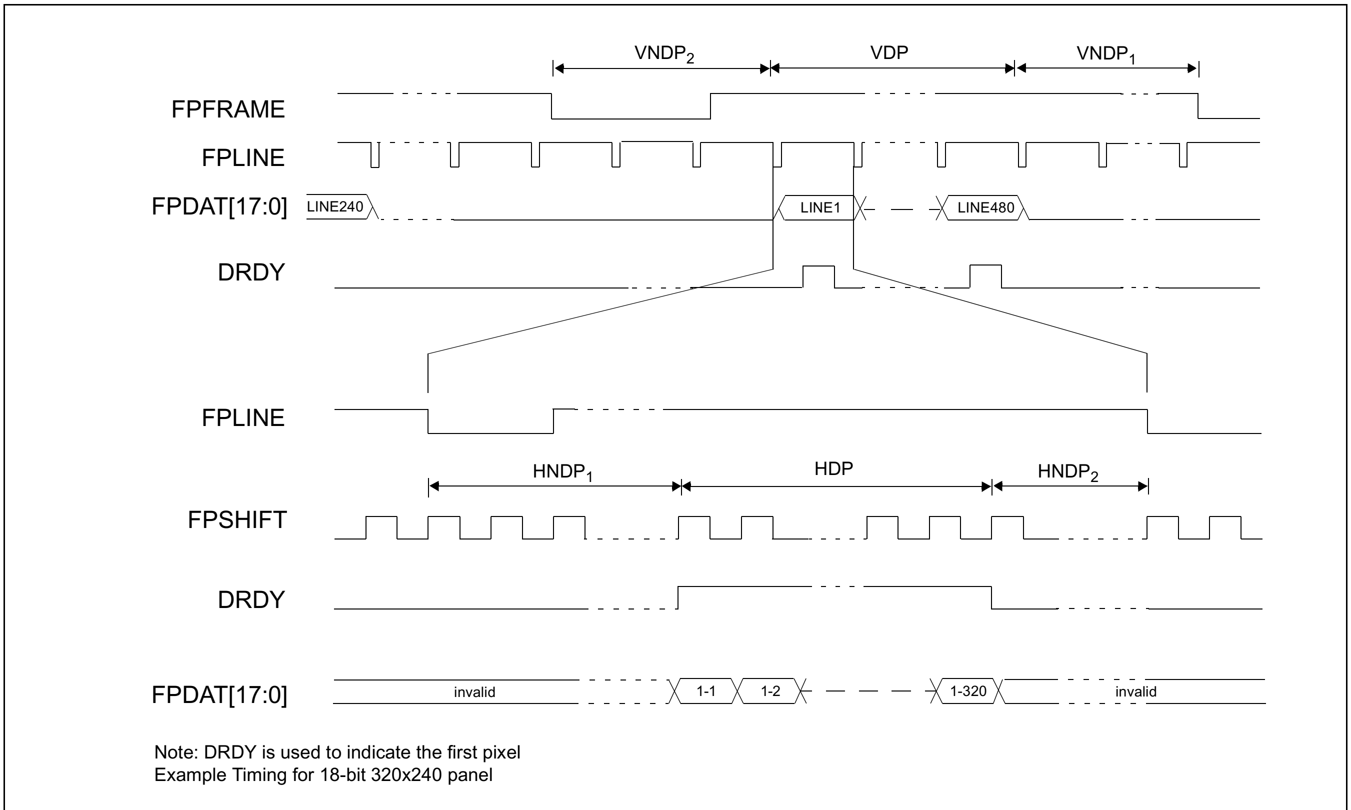


Figure 6-28: 18-Bit TFT Panel Timing

VDP	= Vertical Display Period	
	= VDP Lines	
VNDP	= Vertical Non-Display Period	
	= VNDP1 + VNDP2	
	= VT - VDP Lines	
VNDP1	= Vertical Non-Display Period 1	
	= VNDP - VNDP2 Lines	
VNDP2	= Vertical Non-Display Period 2	
	= VDPS - VPS Lines	if negative add VT
HDP	= Horizontal Display Period	
	= HDP Ts	
HNDP	= Horizontal Non-Display Period	
	= HNDP1 + HNDP2	
	= HT - HDP Ts	
HNDP1	= Horizontal Non-Display Period 1	
	= HDPS - HPS Ts	if negative add HT
HNDP2	= Horizontal Non-Display Period 2	
	= HPS - (HDP + HDPS) Ts	if negative add HT

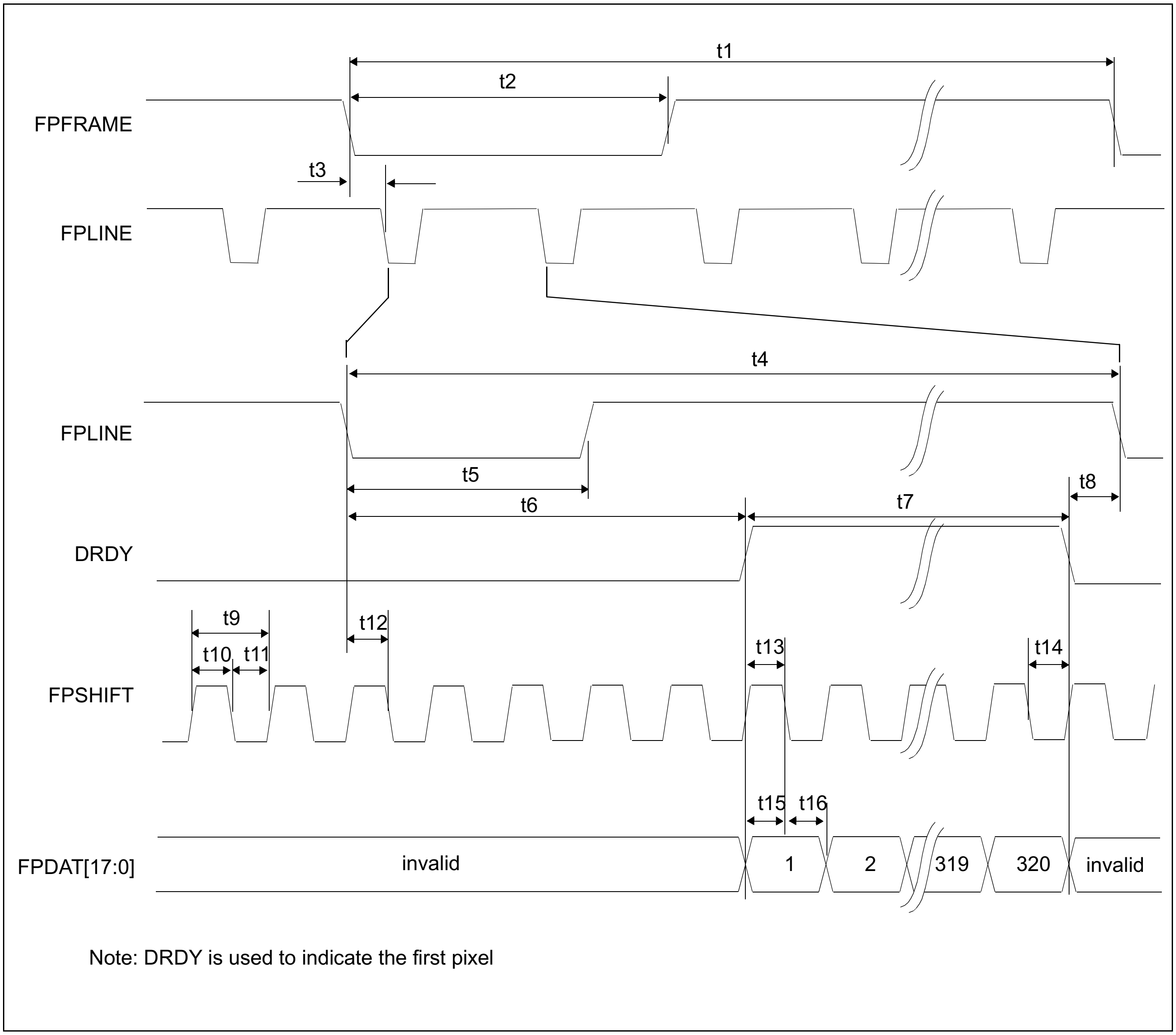


Figure 6-29: TFT A.C. Timing

Table 6-23: TFT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME cycle time	VT			Lines
t2	FPFRAME pulse width low	VPW			Lines
t3	FPFRAME falling edge to FPLINE falling edge phase difference	HPS			Ts (note 1)
t4	FPLINE cycle time	HT			Ts
t5	FPLINE pulse width low	HPW			Ts
t6	FPLINE Falling edge to DRDY active	note 2		250	Ts
t7	DRDY pulse width	HDP			Ts
t8	DRDY falling edge to FPLINE falling edge	note 3			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width high	0.5			Ts
t11	FPSHIFT pulse width low	0.5			Ts
t12	FPLINE setup to FPSHIFT falling edge	0.5			Ts
t13	DRDY to FPSHIFT falling edge setup time	0.5			Ts
t14	DRDY hold from FPSHIFT falling edge	0.5			Ts
t15	Data setup to FPSHIFT falling edge	0.5			Ts
t16	Data hold from FPSHIFT falling edge	0.5			Ts

1. Ts = pixel clock period
2. t6min = HDPS - HPS if negative add HT
3. t8min = HPS - (HDP + HDPS) if negative add HT

6.4.10 160x160 Sharp 'Direct' HR-TFT Panel Timing (e.g. LQ031B1DDxx)

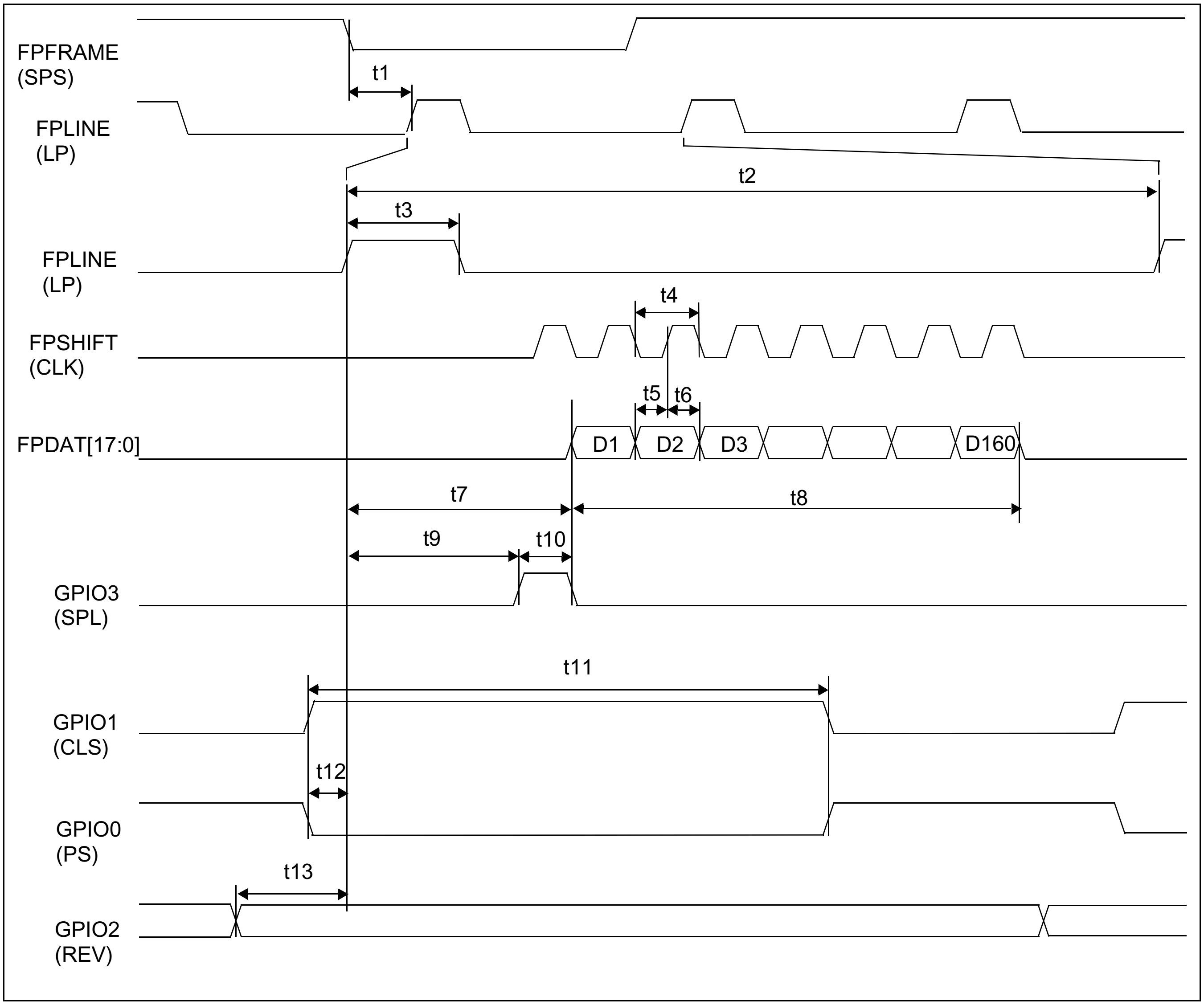


Figure 6-30: 160x160 Sharp 'Direct' HR-TFT Panel Horizontal Timing

Table 6-24: 160x160 Sharp 'Direct' HR-TFT Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE start position		13		Ts (note 1)
t2	Horizontal total period	180		220	Ts
t3	FPLINE width		2		Ts
t4	FPSHIFT period		1		Ts
t5	Data setup to FPSHIFT rising edge	0.5			Ts
t6	Data hold from FPSHIFT rising edge	0.5			Ts
t7	Horizontal display start position		5		Ts
t8	Horizontal display period		160		Ts
t9	FPLINE rising edge to GPIO3 rising edge		4		Ts
t10	GPIO3 pulse width		1		Ts
t11	GPIO1(GPIO0) pulse width		136		Ts
t12	GPIO1 rising edge (GPIO0 falling edge) to FPLINE rise edge		4		Ts
t13	GPIO2 toggle edge to FPLINE rise edge		10		Ts

1. Ts = pixel clock period
2. t1typ = (REG[22h] bits 7-0) + 1
3. t2typ = ((REG[12h] bits 6-0) + 1) x 8
4. t3typ = (REG[20h] bits 6-0) + 1
5. t7typ = ((REG[16h] bits 7-0) + 5) - ((REG[22h] bits 7-0) + 1)
6. t8typ = ((REG[14h] bits 6-0) + 1) x 8

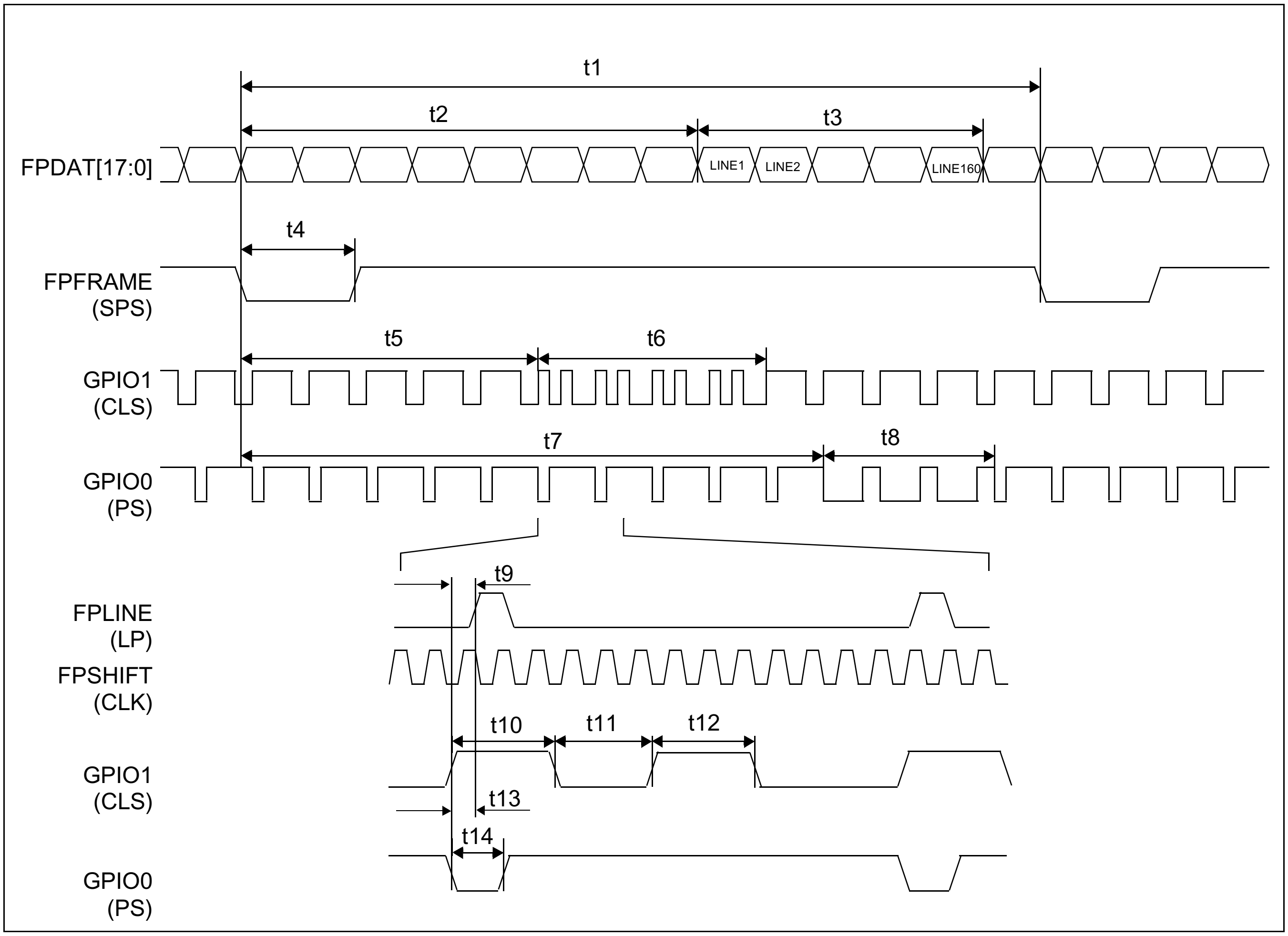


Figure 6-31: 160x160 Sharp 'Direct' HR-TFT Panel Vertical Timing

Table 6-25: 160x160 Sharp 'Direct' HR-TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	203		264	Lines
t2	Vertical display start position		40		Lines
t3	Vertical display period		160		Lines
t4	Vertical sync pulse width		2		Lines
t5	FPFRAME falling edge to GPIO1 alternate timing start		5		Lines
t6	GPIO1 alternate timing period		4		Lines
t7	FPFRAME falling edge to GPIO0 alternate timing start		40		Lines
t8	GPIO0 alternate timing period		162		Lines
t9	GPIO1 first pulse rising edge to FPLINE rising edge		4		Ts (note 1)
t10	GPIO1 first pulse width		48		Ts
t11	GPIO1 first pulse falling edge to second pulse rising edge		40		Ts
t12	GPIO1 second pulse width		48		Ts
t13	GPIO0 falling edge to FPLINE rising edge		4		Ts
t14	GPIO0 low pulse width		24		Ts

1. Ts = pixel clock period

6.4.11 320x240 Sharp 'Direct' HR-TFT Panel Timing (e.g. LQ039Q2DS01)

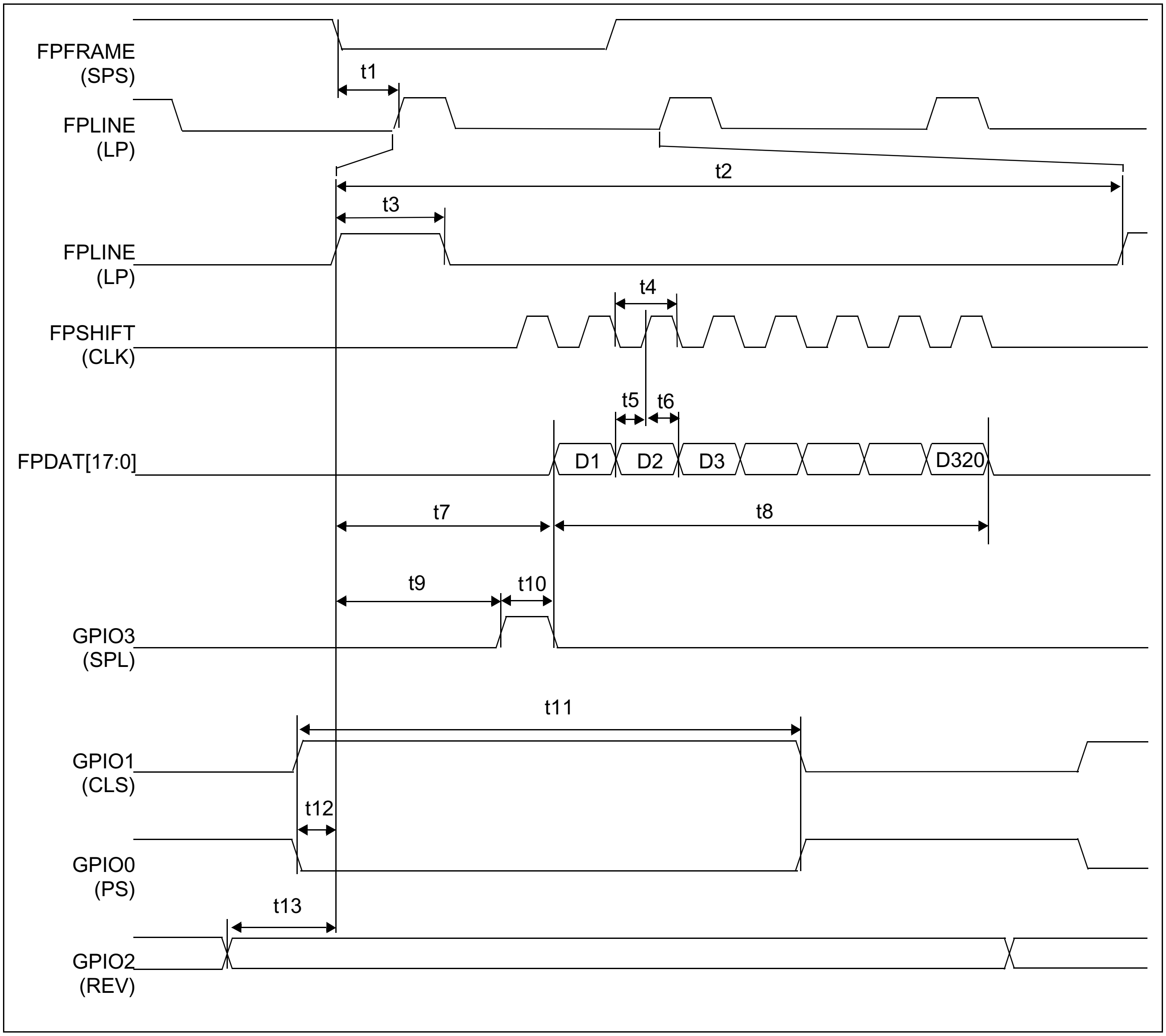


Figure 6-32: 320x240 Sharp 'Direct' HR-TFT Panel Horizontal Timing

Table 6-26: 320x240 Sharp 'Direct' HR-TFT Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE start position		14		Ts (note 1)
t2	Horizontal total period	400		440	Ts
t3	FPLINE width		1		Ts
t4	FPSHIFT period		1		Ts
t5	Data setup to FPSHIFT rising edge	0.5			Ts
t6	Data hold from FPSHIFT rising edge	0.5			Ts
t7	Horizontal display start position		60		Ts
t8	Horizontal display period		320		Ts
t9	FPLINE rising edge to GPIO3 rising edge		59		Ts
t10	GPIO3 pulse width		1		Ts
t11	GPIO1(GPIO0) pulse width		353		Ts
t12	GPIO1 rising edge (GPIO0 falling edge) to FPLINE rise edge		5		Ts
t13	GPIO2 toggle edge to FPLINE rise edge		11		Ts

1. Ts = pixel clock period
2. t1typ = (REG[22h] bits 7-0) + 1
3. t2typ = ((REG[12h] bits 6-0) + 1) x 8
4. t3typ = (REG[20h] bits 6-0) + 1
5. t7typ = ((REG[16h] bits 7-0) + 5) - ((REG[22h] bits 7-0) + 1)
6. t8typ = ((REG[14h] bits 6-0) + 1) x 8

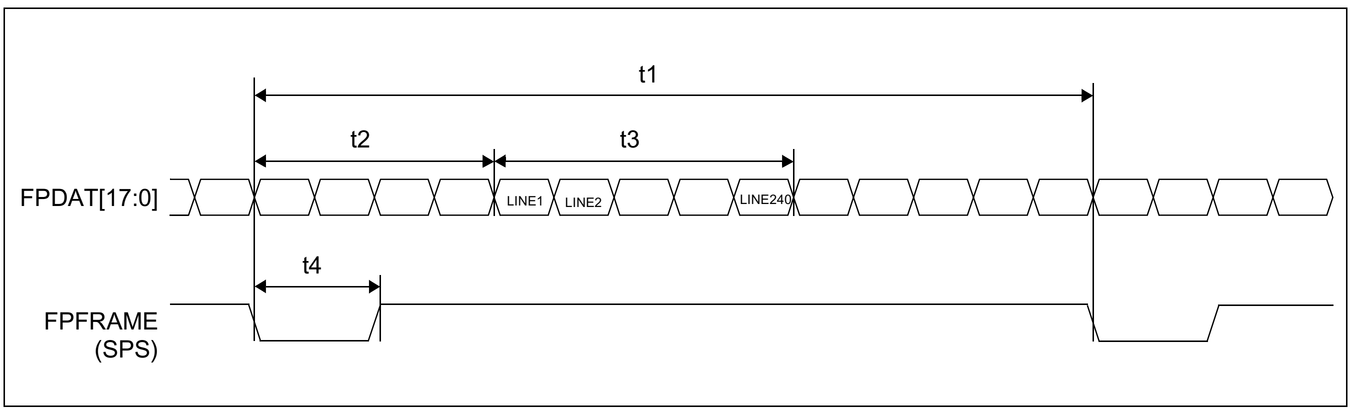


Figure 6-33: 320x240 Sharp 'Direct' HR-TFT Panel Vertical Timing

Table 6-27: 320x240 Sharp 'Direct' HR-TFT Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	245		330	Lines
t2	Vertical display start position		4		Lines
t3	Vertical display period		240		Lines
t4	Vertical sync pulse width		2		Lines

6.4.12 160x240 Epson D-TFD Panel Timing (e.g. LF26SCR)

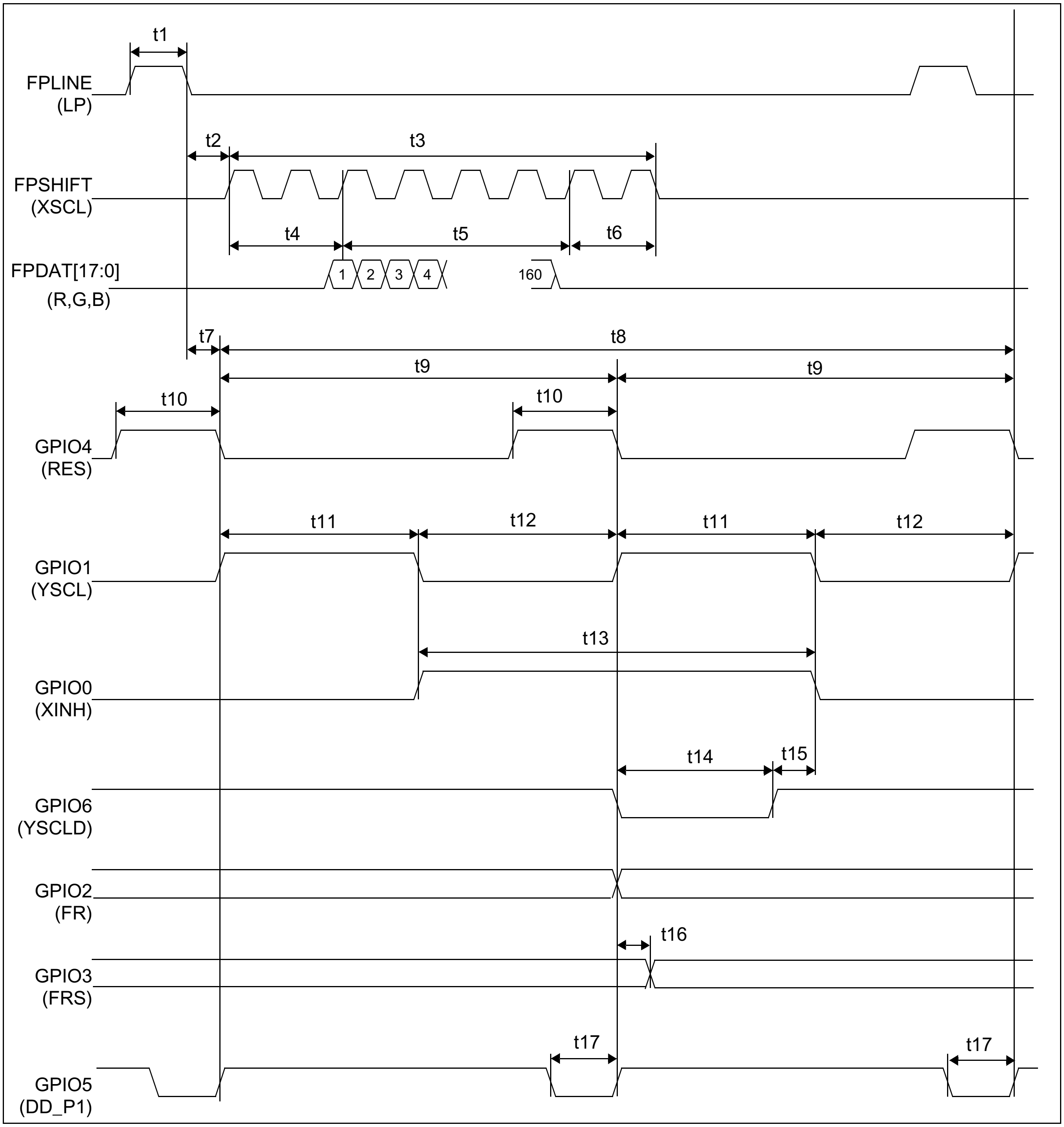


Figure 6-34: 160x240 Epson D-TFD Panel Horizontal Timing

Table 6-28: 160x240 Epson D-TFD Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE pulse width		9		Ts (note 1)
t2	FPLINE falling edge to FPSHIFT start position		8.5		Ts
t3	FPSHIFT active period		167		Ts
t4	FPSHIFT start to first data		4		Ts
t5	Horizontal display period		160		Ts
t6	Last data to FPSHIFT inactive		3		Ts
t7	FPLINE falling edge to GPIO4 first pulse falling edge		1		Ts
t8	Horizontal total period		400		Ts
t9	GPIO4 first pulse falling edge to second pulse falling edge		200		Ts
t10	GPIO4 pulse width		11		Ts
t11	GPIO1 pulse width		100		Ts
t12	GPIO1 low period		100)		Ts
t13	GPIO0 pulse width		200		Ts
t14	GPIO6 low pulse width		90		Ts
t15	GPIO6 rising edge to GPIO0 falling edge		10		Ts
t16	GPIO2 toggle to GPIO3 toggle		1		Ts
t17	GPIO5 low pulse width		7		Ts

1. Ts = pixel clock period

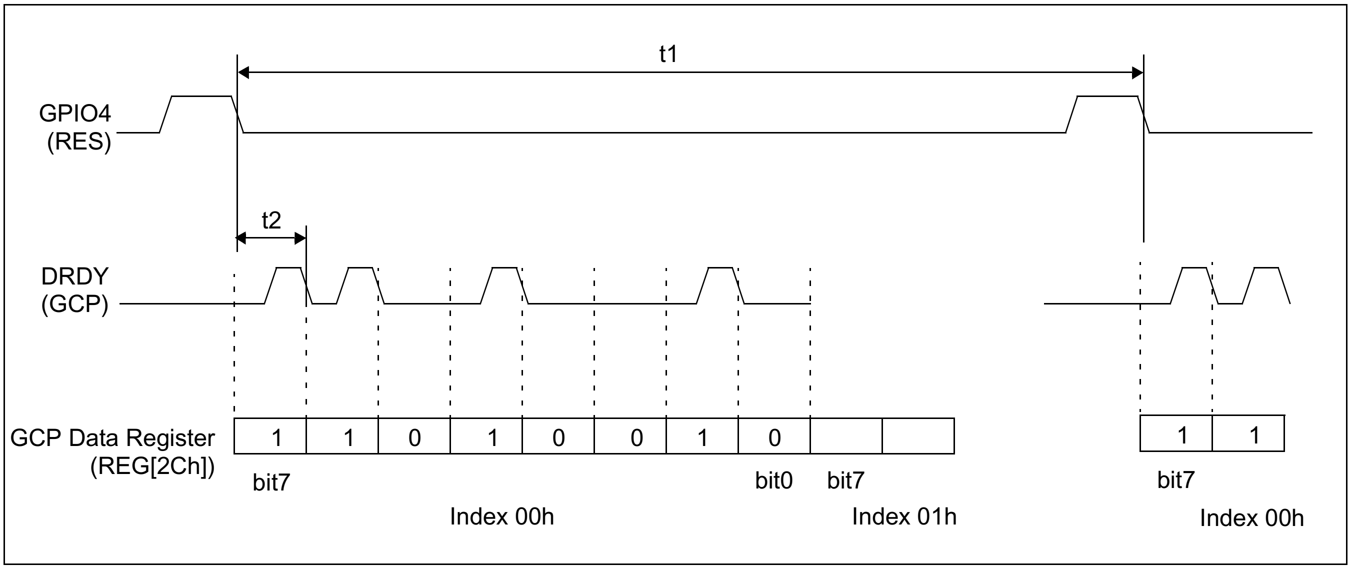


Figure 6-35: 160x240 Epson D-TFD Panel GCP Horizontal Timing

Table 6-29: 160x240 Epson D-TFD Panel GCP Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Half of the horizontal total period		200		Ts (note 1)
t2	GCP clock period		1		Ts

1. Ts = pixel clock period

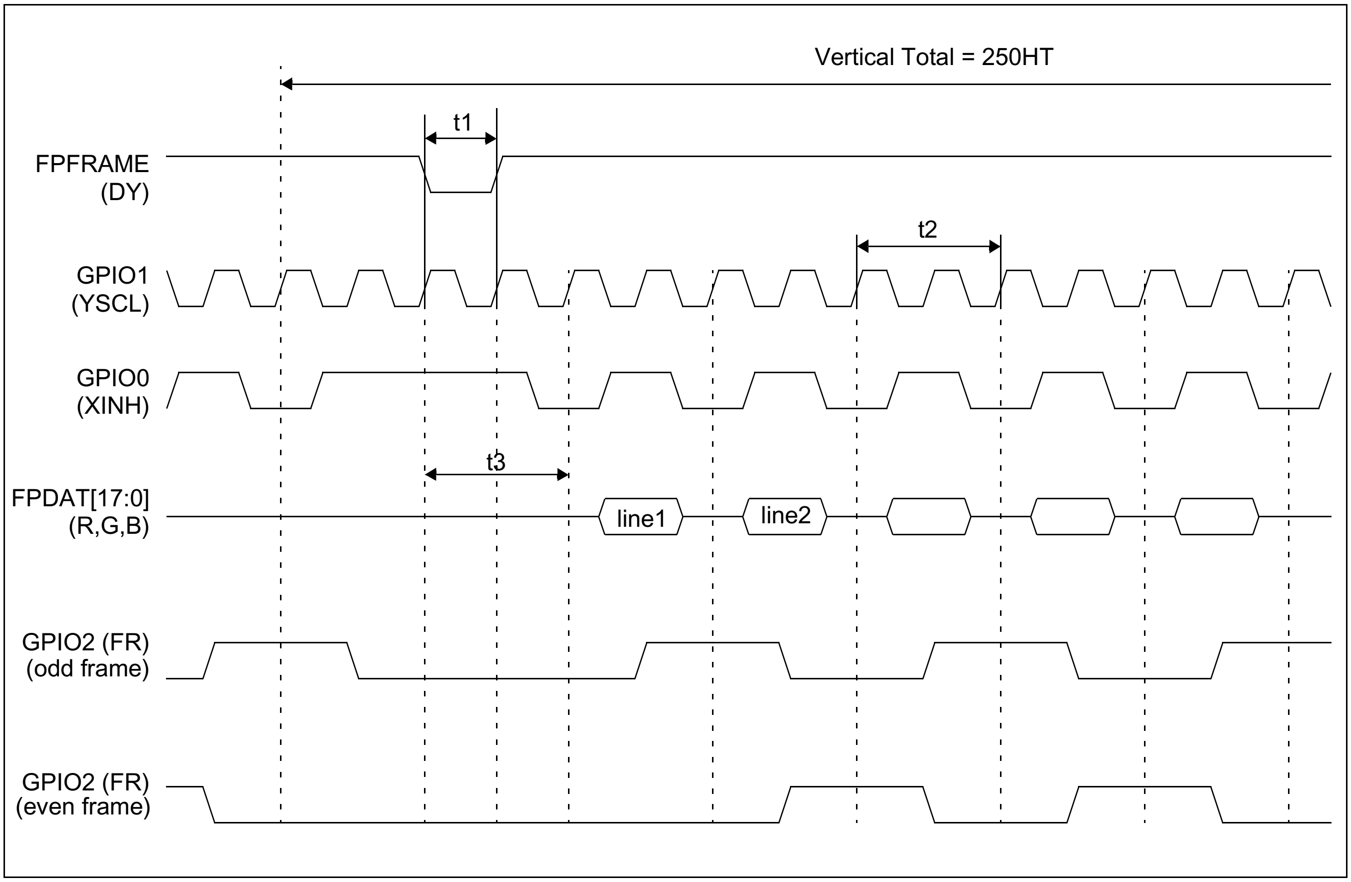


Figure 6-36: 160x240 Epson D-TFD Panel Vertical Timing

Table 6-30: 160x240 Epson D-TFD Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME pulse width		200		Ts (note 1)
t2	Horizontal total period		400		Ts
t3	Vertical display start		400		Ts

1. Ts = pixel clock period

6.4.13 320x240 Epson D-TFD Panel Timing (e.g. LF37SQR)

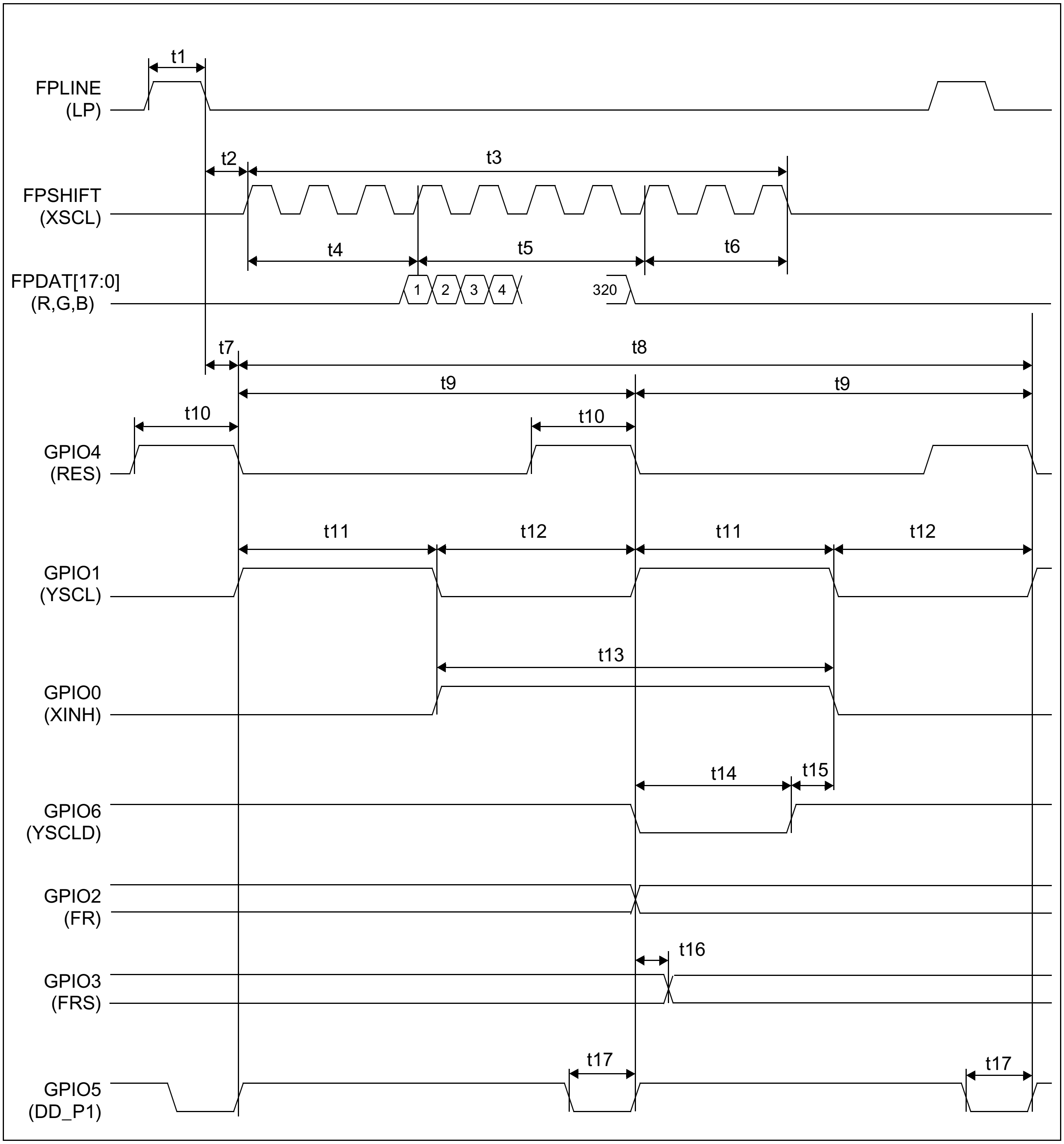


Figure 6-37: 320x240 Epson D-TFD Panel Horizontal Timing

Table 6-31: 320x240 Epson D-TFD Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPLINE pulse width		9		Ts (note 1)
t2	FPLINE falling edge to FPSHIFT start position		8.5		Ts
t3	FPSHIFT active period		331		Ts
t4	FPSHIFT start to first data		6		Ts
t5	Horizontal display period		320		Ts
t6	Last data to FPSHIFT inactive		5		Ts
t7	FPLINE falling edge to GPIO4 first pulse falling edge		1		Ts
t8	Horizontal total period		400		Ts
t9	GPIO4 first pulse falling edge to second pulse falling edge		200		Ts
t10	GPIO4 pulse width		11		Ts
t11	GPIO1 pulse width		100		Ts
t12	GPIO1 low period		100		Ts
t13	GPIO0 pulse width		200		Ts
t14	GPIO6 low pulse width		90		Ts
t15	GPIO6 rising edge to GPIO0 falling edge		10		Ts
t16	GPIO2 toggle to GPIO3 toggle		1		Ts
t17	GPIO5 low pulse width		7		Ts

1. Ts = pixel clock period

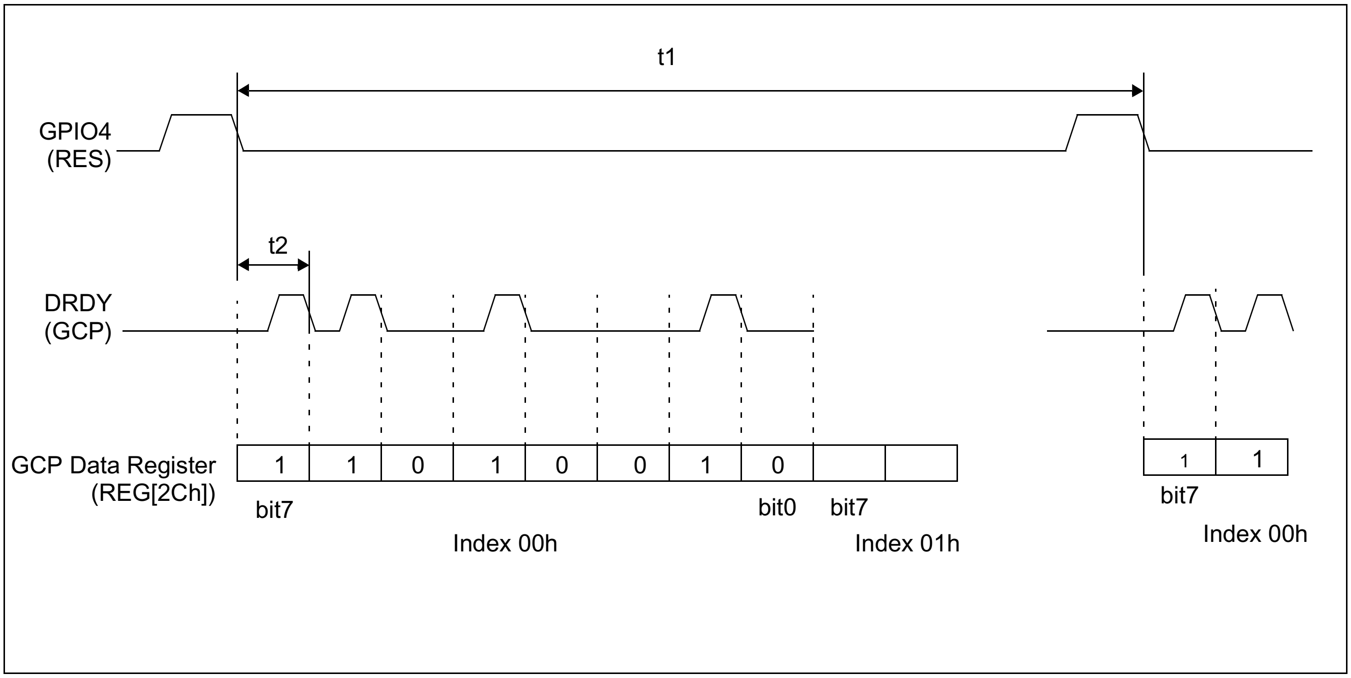


Figure 6-38: 320x240 Epson D-TFD Panel GCP Horizontal Timing

Table 6-32: 320x240 Epson D-TFD Panel GCP Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Half of the horizontal total period		200		Ts (note 1)
t2	GCP clock period		1		Ts

1. Ts = pixel clock period

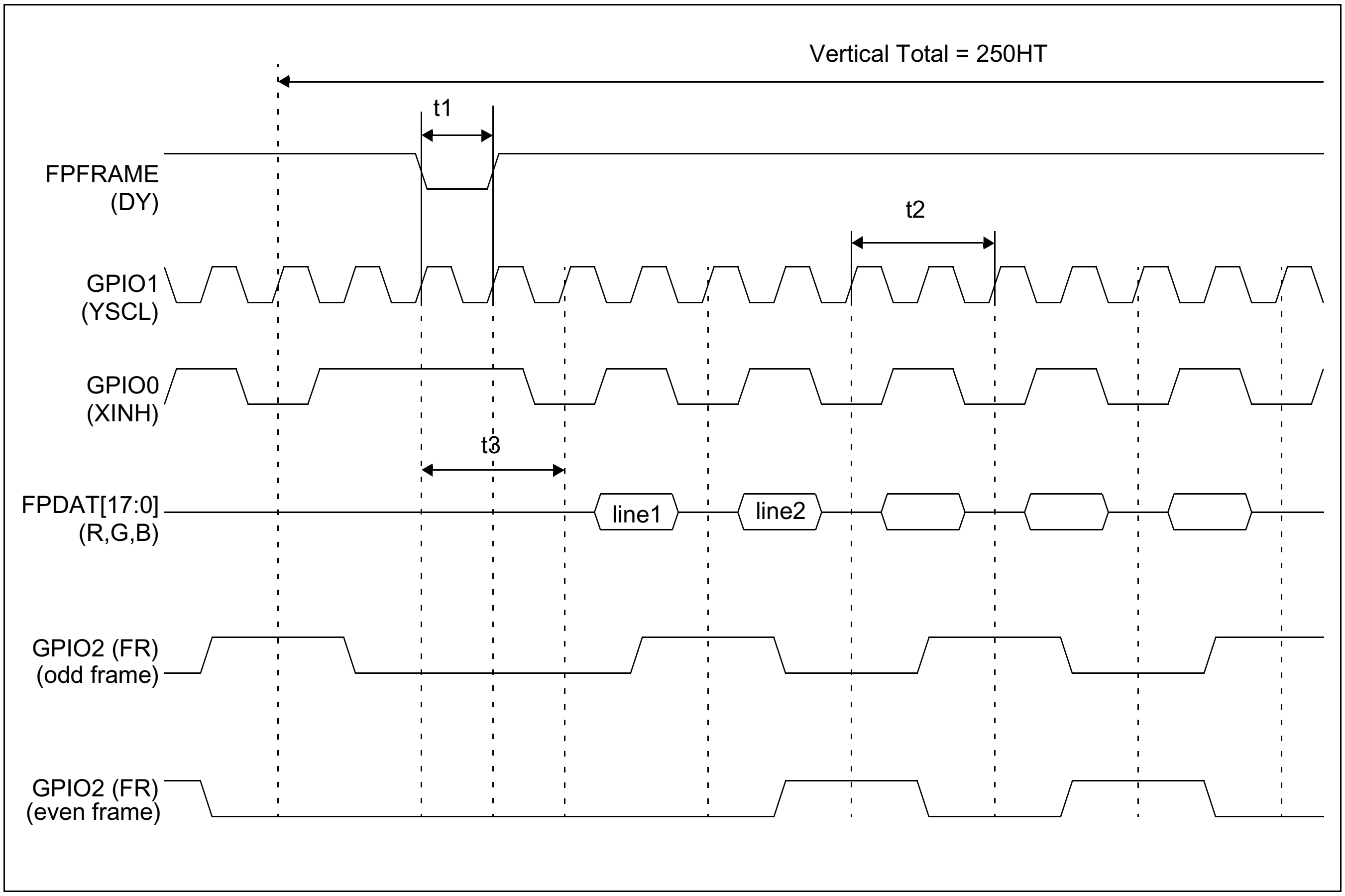


Figure 6-39: 320x240 Epson D-TFD Panel Vertical Timing

Table 6-33: 320x240 Epson D-TFD Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME pulse width		200		Ts (note 1)
t2	Horizontal total period		400		Ts
t3	Vertical display start		400		Ts

1. Ts = pixel clock period

7 Clocks

7.1 Clock Descriptions

7.1.1 BCLK

BCLK is an internal clock derived from CLKI. BCLK can be a divided version (÷1, ÷2, ÷3, ÷4) of CLKI. CLKI is typically derived from the host CPU bus clock.

The source clock options for BCLK may be selected as in the following table.

Table 7-1: BCLK Clock Selection

Source Clock Options	BCLK Selection
CLKI	CNF[7:6] = 00
CLKI ÷2	CNF[7:6] = 01
CLKI ÷3	CNF[7:6] = 10
CLKI ÷4	CNF[7:6] = 11

Note
For synchronous bus interfaces, it is recommended that BCLK be set the same as the CPU bus clock (not a divided version of CLKI) e.g. SH-3, SH-4.

Note
The CLKI ÷ 3 and CLKI ÷ 4 options may not work properly with bus interfaces with short back-to-back cycle timing.

7.1.2 MCLK

MCLK provides the internal clock required to access the embedded SRAM. The S1D13706 is designed with efficient power saving control for clocks (clocks are turned off when not used); reducing the frequency of MCLK does not necessarily save more power. Furthermore, reducing the MCLK frequency relative to the BCLK frequency increases the CPU cycle latency and so reduces screen update performance. For a balance of power saving and performance, the MCLK should be configured to have a high enough frequency setting to provide sufficient screen refresh as well as acceptable CPU cycle latency.

The source clock options for MCLK may be selected as in the following table.

Table 7-2: MCLK Clock Selection

Source Clock Options	MCLK Selection
BCLK	REG[04h] bit 5,4 = 00
BCLK ÷2	REG[04h] bit 5,4 = 01
BCLK ÷3	REG[04h] bit 5,4 = 10
BCLK ÷4	REG[04h] bit 5,4 = 11

7.1.3 PCLK

PCLK is the internal clock used to control the LCD panel. PCLK should be chosen to match the optimum frame rate of the LCD panel. See Section 9, “Frame Rate Calculation” on page 130 for details on the relationship between PCLK and frame rate.

Some flexibility is possible in the selection of PCLK. Firstly, LCD panels typically have a range of permissible frame rates. Secondly, it may be possible to choose a higher PCLK frequency and tailor the horizontal and vertical non-display periods to lower the frame-rate to its optimal value.

The source clock options for PCLK may be selected as in the following table.

Table 7-3: PCLK Clock Selection

Source Clock Options	PCLK Selection
MCLK	REG[05h] = 00h
MCLK ÷2	REG[05h] = 10h
MCLK ÷3	REG[05h] = 20h
MCLK ÷4	REG[05h] = 30h
MCLK ÷8	REG[05h] = 40h
BCLK	REG[05h] = 01h
BCLK ÷2	REG[05h] = 11h
BCLK ÷3	REG[05h] = 21h
BCLK ÷4	REG[05h] = 31h
BCLK ÷8	REG[05h] = 41h
CLKI	REG[05h] = 02h
CLKI ÷2	REG[05h] = 12h
CLKI ÷3	REG[05h] = 22h
CLKI ÷4	REG[05h] = 32h
CLKI ÷8	REG[05h] = 42h
CLKI2	REG[05h] = 03h
CLKI2 ÷2	REG[05h] = 13h
CLKI2 ÷3	REG[05h] = 23h
CLKI2 ÷4	REG[05h] = 33h
CLKI2 ÷8	REG[05h] = 43h

There is a relationship between the frequency of MCLK and PCLK that must be maintained.

Table 7-4: Relationship between MCLK and PCLK

SwivelView Orientation	Color Depth (bpp)	MCLK to PCLK Relationship
SwivelView 0° and 180°	16	$f_{MCLK} \geq f_{PCLK}$
	8	$f_{MCLK} \geq f_{PCLK} \div 2$
	4	$f_{MCLK} \geq f_{PCLK} \div 4$
	2	$f_{MCLK} \geq f_{PCLK} \div 8$
	1	$f_{MCLK} \geq f_{PCLK} \div 16$
SwivelView 90° and 270°	16/8/4/2/1	$f_{MCLK} \geq 1.25 f_{PCLK}$

7.1.4 PWMCLK

PWMCLK is the internal clock used by the Pulse Width Modulator for output to the panel.

The source clock options for PWMCLK may be selected as in the following table.

Table 7-5: PWMCLK Clock Selection

Source Clock Options	PWMCLK Selection
CLKI	REG[B1h] bit 0 = 0
CLKI2	REG[B1h] bit 0 = 1

For further information on controlling PWMCLK, see Section 8.3.9, “Pulse Width Modulation (PWM) Clock and Contrast Voltage (CV) Pulse Configuration Registers” on page 126.

Note

The S1D13706 provides Pulse Width Modulation output on the pin PWMOUT. PWMOUT can be used to control LCD panels which support PWM control of the back-light inverter.

7.2 Clock Selection

The following diagram provides a logical representation of the S1D13706 internal clocks.

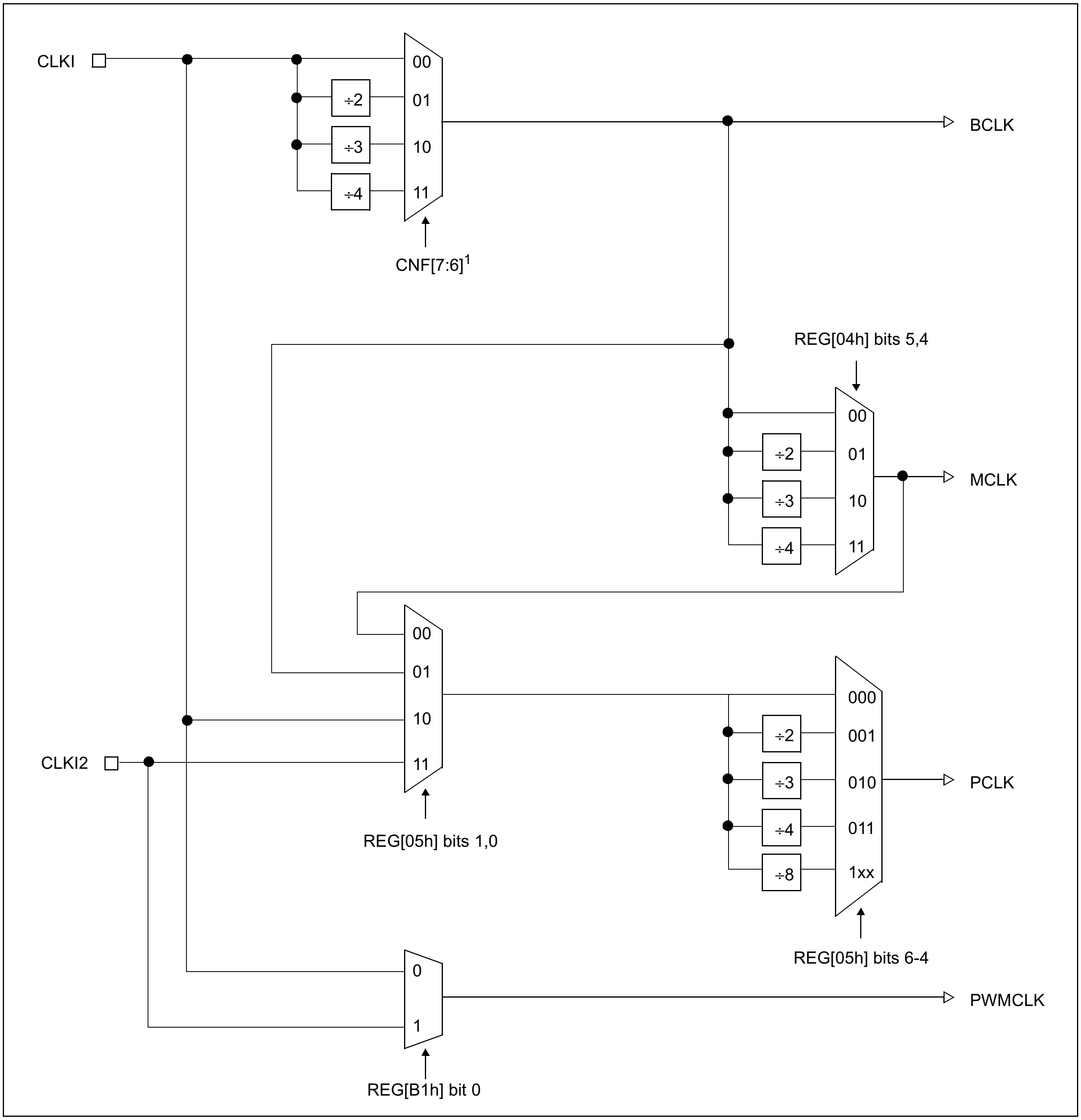


Figure 7-1: Clock Selection

Note
[1] CNF[7:6] must be set at RESET#.

7.3 Clocks versus Functions

Table 7-6: "S1D13706 Internal Clock Requirements", lists the internal clocks required for the following S1D13706 functions.

Table 7-6: S1D13706 Internal Clock Requirements

Function	Bus Clock (BCLK)	Memory Clock (MCLK)	Pixel Clock (PCLK)	PWM Clock (PWMCLK)
Register Read/Write	Required	Not Required	Not Required	Not Required[1]
Memory Read/Write	Required	Required	Not Required	Not Required[1]
Look-Up Table Register Read/Write	Required	Required	Not Required	Not Required[1]
Software Power Save	Required	Not Required	Not Required	Not Required[1]
LCD Output	Required	Required	Required	Not Required[1]

Note
[1]PWMCLK is an optional clock (see Section 7.1.4, "PWMCLK" on page 92).

8 Registers

This section discusses how and where to access the S1D13706 registers. It also provides detailed information about the layout and usage of each register.

8.1 Register Mapping

The S1D13706 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed. The register space is decoded by A[16:0].

8.2 Register Set

The S1D13706 register set is as follows.

Table 8-1: S1D13706 Register Set

Register	Pg	Register	Pg
Read-Only Configuration Registers			
REG[00h] Revision Code Register	96	REG[01h] Display Buffer Size Register	97
REG[02h] Configuration Readback Register	97		
Clock Configuration Registers			
REG[04h] Memory Clock Configuration Register	97	REG[05h] Pixel Clock Configuration Register	98
Look-Up Table Registers			
REG[08h] Look-Up Table Blue Write Data Register	99	REG[09h] Look-Up Table Green Write Data Register	99
REG[0Ah] Look-Up Table Red Write Data Register	99	REG[0Bh] Look-Up Table Write Address Register	100
REG[0Ch] Look-Up Table Blue Read Data Register	100	REG[0Dh] Look-Up Table Green Read Data Register	100
REG[0Eh] Look-Up Table Red Read Data Register	101	REG[0Fh] Look-Up Table Read Address Register	101
Panel Configuration Registers			
REG[10h] Panel Type Register	101	REG[11h] MOD Rate Register	103
REG[12h] Horizontal Total Register	103	REG[14h] Horizontal Display Period Register	103
REG[16h] Horizontal Display Period Start Position Register 0	104	REG[17h] Horizontal Display Period Start Position Register 1	104
REG[18h] Vertical Total Register 0	105	REG[19h] Vertical Total Register 1	105
REG[1Ch] Vertical Display Period Register 0	105	REG[1Dh] Vertical Display Period Register 1	105
REG[1Eh] Vertical Display Period Start Position Register 0	106	REG[1Fh] Vertical Display Period Start Position Register 1	106
REG[20h] FPLINE Pulse Width Register	106	REG[22h] FPLINE Pulse Start Position Register 0	107
REG[23h] FPLINE Pulse Start Position Register 1	107	REG[24h] FPFRAME Pulse Width Register	107
REG[26h] FPFRAME Pulse Start Position Register 0	108	REG[27h] FPFRAME Pulse Start Position Register 1	108
REG[28h] D-TFD GCP Index Register	108	REG[2Ch] D-TFD GCP Data Register	108
Display Mode Registers			
REG[70h] Display Mode Register	109	REG[71h] Special Effects Register	111
REG[74h] Main Window Display Start Address Register 0	113	REG[75h] Main Window Display Start Address Register 1	113
REG[76h] Main Window Display Start Address Register 2	113	REG[78h] Main Window Line Address Offset Register 0	114
REG[79h] Main Window Line Address Offset Register 1	114		

Table 8-1: S1D13706 Register Set

Register	Pg	Register	Pg
Picture-in-Picture Plus (PIP$^+$) Registers			
REG[7Ch] PIP$^+$ Window Display Start Address Register 0	115	REG[7Dh] PIP$^+$ Window Display Start Address Register 1	115
REG[7Eh] PIP$^+$ Window Display Start Address Register 2	115	REG[80h] PIP$^+$ Window Line Address Offset Register 0	115
REG[81h] PIP$^+$ Window Line Address Offset Register 1	115	REG[84h] PIP$^+$ Window X Start Position Register 0	116
REG[85h] PIP$^+$ Window X Start Position Register 1	116	REG[88h] PIP$^+$ Window Y Start Position Register 0	117
REG[89h] PIP$^+$ Window Y Start Position Register 1	117	REG[8Ch] PIP$^+$ Window X End Position Register 0	118
REG[8Dh] PIP$^+$ Window X End Position Register 1	118	REG[90h] PIP$^+$ Window Y End Position Register 0	119
REG[91h] PIP$^+$ Window Y End Position Register 1	119		
Miscellaneous Registers			
REG[A0h] Power Save Configuration Register	120	REG[A1h] Reserved	120
REG[A2h] Reserved	121	REG[A3h] Reserved	121
REG[A4h] Scratch Pad Register 0	121	REG[A5h] Scratch Pad Register 1	121
General Purpose IO Pins Registers			
REG[A8h] General Purpose IO Pins Configuration Register 0	122	REG[A9h] General Purpose IO Pins Configuration Register 1	122
REG[ACh] General Purpose IO Pins Status/Control Register 0	123	REG[ADh] General Purpose IO Pins Status/Control Register 1	125
PWM Clock and CV Pulse Configuration Registers			
REG[B0h] PWM Clock / CV Pulse Control Register	126	REG[B1h] PWM Clock / CV Pulse Configuration Register	128
REG[B2h] CV Pulse Burst Length Register	129	REG[B3h] PWMOUT Duty Cycle Register	129

8.3 Register Descriptions

Unless specified otherwise, all register bits are set to 0 during power-on.

8.3.1 Read-Only Configuration Registers

Revision Code Register REG[00h]							Read Only
Product Code Bits 5-0						Revision Code Bits 1-0	
7	6	5	4	3	2	1	0

Note
The S1D13706 returns a value of 28h.

bits 7-2 Product Code
These are read-only bits that indicates the product code. The product code is 001010.

bits 1-0 Revision Code
These are read-only bits that indicates the revision code. The revision code is 00.

Display Buffer Size Register REG[01h]							Read Only
Display Buffer Size Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Display Buffer Size Bits [7:0]
This is a read-only register that indicates the size of the SRAM display buffer measured in 4K byte increments. The S1D13706 display buffer is 80K bytes and therefore this register returns a value of 20 (14h).

Value of this register = display buffer size ÷ 4K bytes
= 80K bytes ÷ 4K bytes
= 20 (14h)

Configuration Readback Register REG[02h]							Read Only
CNF7 Status	CNF6 Status	CNF5 Status	CNF4 Status	CNF3 Status	CNF2 Status	CNF1 Status	CNF0 Status
7	6	5	4	3	2	1	0

bits 7-0 CNF[7:0] Status
These read-only status bits return the status of the configuration pins CNF[7:0]. CNF[7:0] are latched at the rising edge of RESET#.

8.3.2 Clock Configuration Registers

Memory Clock Configuration Register REG[04h]							Read/Write
n/a		MCLK Divide Select Bits 1-0		n/a			Reserved
7	6	5	4	3	2	1	0

bits 5-4 MCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the Memory Clock (MCLK) from the Bus Clock (BCLK).

Table 8-2: MCLK Divide Selection

MCLK Divide Select Bits	BCLK to MCLK Frequency Ratio
00	1:1
01	2:1
10	3:1
11	4:1

bit 0 Reserved.
This bit must remain at 0.

Pixel Clock Configuration Register REG[05h]							Read/Write
n/a	PCLK Divide Select Bits 2-0			n/a		PCLK Source Select Bits 1-0	
7	6	5	4	3	2	1	0

bits 6-4 PCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the Pixel Clock (PCLK) from the Pixel Clock Source.

Table 8-3: PCLK Divide Selection

PCLK Divide Select Bits	PCLK Source to PCLK Frequency Ratio
000	1:1
001	2:1
010	3:1
011	4:1
1XX	8:1

bits 1-0 PCLK Source Select Bits [1:0]
These bits determine the source of the Pixel Clock (PCLK).

Table 8-4: PCLK Source Selection

PCLK Source Select Bits	PCLK Source
00	MCLK
01	BCLK
10	CLKI
11	CLKI2

8.3.3 Look-Up Table Registers

Note
The S1D13706 has three 256-position, 6-bit wide LUTs, one for each of red, green, and blue (see Section 11, “Look-Up Table Architecture” on page 132).

Look-Up Table Blue Write Data Register REG[08h]							Write Only
LUT Blue Write Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Blue Write Data Bits [5:0]
This register contains the data to be written to the blue component of the Look-Up Table. The data is stored in this register until a write to the LUT Write Address register (REG[0Bh]) moves the data into the Look-Up Table.

Note
The LUT entry is updated only when the LUT Write Address Register (REG[0Bh]) is written to.

Look-Up Table Green Write Data Register REG[09h]							Write Only
LUT Green Write Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Green Write Data Bits [5:0]
This register contains the data to be written to the green component of the Look-Up Table. The data is stored in this register until a write to the LUT Write Address register (REG[0Bh]) moves the data into the Look-Up Table.

Note
The LUT entry is updated only when the LUT Write Address Register (REG[0Bh]) is written to.

Look-Up Table Red Write Data Register REG[0Ah]							Write Only
LUT Red Write Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Red Write Data Bits [5:0]
This register contains the data to be written to the red component of the Look-Up Table. The data is stored in this register until a write to the LUT Write Address register (REG[0Bh]) moves the data into the Look-Up Table.

Note
The LUT entry is updated only when the LUT Write Address Register (REG[0Bh]) is written to.

Look-Up Table Write Address Register REG[0Bh]							Write Only
LUT Write Address Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 LUT Write Address Bits [7:0]
This register forms a pointer into the Look-Up Table (LUT) which is used to write LUT blue, green, and red data stored in REG[08h], REG[09h], and REG[0Ah]. **The data is updated to the LUT only with the completion of a write to this register**. This is a write-only register and returns 00h if read.

Note
When a value is written to the LUT Write Address register, the same value is automatically written to the LUT Read Address register (REG[0Fh].

Look-Up Table Blue Read Data Register REG[0Ch]							Read Only
LUT Blue Read Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Blue Read Data Bits [5:0]
This register contains the data from the blue component of the Look-Up Table. The LUT position is controlled by the LUT Read Address Register (REG[0Fh]). This is a read-only register.

Note
This register is updated only when the LUT Read Address Register (REG[0Fh]) is written to.

Look-Up Table Green Read Data Register REG[0Dh]							Read Only
LUT Green Read Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Green Read Data Bits [5:0]
This register contains the data from the green component of the Look-Up Table. The LUT position is controlled by the LUT Read Address Register (REG[0Fh]). This is a read-only register.

Note
This register is updated only when the LUT Read Address Register (REG[0Fh]) is written to.

Look-Up Table Red Read Data Register REG[0Eh]							Read Only
LUT Red Read Data Bits 5-0						n/a	
7	6	5	4	3	2	1	0

bits 7-2 LUT Red Read Data Bits [5:0]
This register contains the data from the red component of the Look-Up Table. The LUT position is controlled by the LUT Read Address Register (REG[0Fh]). This is a read-only register.

Note
This register is updated only when the LUT Read Address Register (REG[0Fh]) is written to.

Look-Up Table Read Address Register REG[0Fh]							Write Only
LUT Read Address Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 LUT Read Address Bits [7:0]
This register forms a pointer into the Look-Up Table (LUT) which is used to read LUT blue, green, and red data. Blue data is read from REG[0Ch], green data from REG[0Dh], and red data from REG[0Eh]. This is a write-only register and returns 00h if read.

Note
If a write to the LUT Write Address register (REG[0Bh]) is made, the LUT Read Address register is automatically updated with the same value.

8.3.4 Panel Configuration Registers

Panel Type Register REG[10h]							Read/Write
Panel Data Format Select	Color/Mono. Panel Select	Panel Data Width Bits 1-0		Active Panel Resolution Select	n/a	Panel Type Bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Panel Data Format Select
When this bit = 0, 8-bit single color passive LCD panel data format 1 is selected. For AC timing see Section 6.4.5, “Single Color 8-Bit Panel Timing (Format 1)” on page 66.
When this bit = 1, 8-bit single color passive LCD panel data format 2 is selected. For AC timing see Section 6.4.6, “Single Color 8-Bit Panel Timing (Format 2)” on page 68.

bit 6 Color/Mono Panel Select
When this bit = 0, a monochrome LCD panel is selected.
When this bit = 1, a color LCD panel is selected.

bits 5-4 Panel Data Width Bits [1:0]
These bits select the data width size of the LCD panel.

Table 8-5: Panel Data Width Selection

Panel Data Width Bits [1:0]	Passive Panel Data Width Size	Active Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	18-bit
11	Reserved	Reserved

bit 3 Active Panel Resolution Select
This bit selects one of two panel resolutions when an HR-TFT or D-TFD panel is selected. This bit has no effect for other panel types.

Table 8-6: Active Panel Resolution Selection

Active Panel Resolution Select Bit	HR-TFT Resolution	D-TFD Resolution
0	160x160	160x240
1	320x240	320x240

Note
This bit sets some internal non-configurable timing values for the selected panel. However, all panel configuration registers (REG[12h] - REG[27h]) still require programming with the appropriate values for the selected panel. For panel AC timing, see Section 6.4, “Display Interface” on page 56.

bits 1-0 Panel Type Bits[1:0]
These bits select the panel type.

Table 8-7: LCD Panel Type Selection

REG[10h] Bits[1:0]	Panel Type
00	STN
01	TFT
10	HR-TFT
11	D-TFD

MOD Rate Register REG[11h]							Read/Write
n/a		MOD Rate Bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 MOD Rate Bits [5:0]
These bits are for passive LCD panels only.
When these bits are all 0, the MOD output signal (DRDY) toggles every FPFRAME.
For a non-zero value *n*, the MOD output signal (DRDY) toggles every n FPLINE.

Horizontal Total Register REG[12h]							Read/Write
n/a	Horizontal Total Bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 Horizontal Total Bits [6:0]
These bits specify the LCD panel Horizontal Total period, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display period and the Horizontal Non-Display period. Since the maximum Horizontal Total is 1024 pixels, the maximum panel resolution supported is 800x600.

Horizontal Total in number of pixels = ((REG[12h] bits 6:0) + 1) $\times$ 8

Note
[1] This register must be programmed such that the following formulas are valid.
HDPS + HDP < HT
[2] For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

Horizontal Display Period Register REG[14h]							Read/Write
n/a	Horizontal Display Period Bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 Horizontal Display Period Bits [6:0]
These bits specify the LCD panel Horizontal Display Period (HDP), in 8 pixel resolution. The Horizontal Display Period should be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.

Horizontal Display Period in number of pixels = ((REG[14h] bits 6:0) + 1) $\times$ 8

Note
For passive panels, HDP must be a minimum of 32 pixels and can be increased by multiples of 16. For TFT panels, HDP must be a minimum of 16 pixels and can be increased by multiples of 8.

For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

Horizontal Display Period Start Position Register 0 REG[16h]							Read/Write
Horizontal Display Period Start Position Bits 7-0							
7	6	5	4	3	2	1	0

Horizontal Display Period Start Position Register 1 REG[17h]							Read/Write
n/a						Horizontal Display Period Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 Horizontal Display Period Start Position Bits [9:0]
These bits specify a value used in the calculation of the Horizontal Display Period Start Position (in 1 pixel resolution) for TFT, HR-TFT and D-TFD panels.

For passive LCD panels these bits must be set to 00h which will result in HDPS = 22.
HDPS = (REG[17h] bits 1-0, REG[16h] bits 7-0) + 22

For TFT/HR-TFT/D-TFD panels, HDPS is calculated using the following formula.
HDPS = (REG[17h] bits 1-0, REG[16h] bits 7-0) + 5

For further information on calculating the HDPS, see the specific panel AC Timing in Section 6.4, “Display Interface” on page 56.

Note
This register must be programmed such that the following formula is valid.
HDPS + HDP < HT

Vertical Total Register 0 REG[18h]							Read/Write
Vertical Total Bits 7-0							
7	6	5	4	3	2	1	0

Vertical Total Register 1 REG[19h]							Read/Write
n/a						Vertical Total Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 Vertical Total Bits [9:0]
These bits specify the LCD panel Vertical Total period, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

Vertical Total in number of lines = (REG[18h] bits 7:0, REG[19h] bits 1:0) + 1

Note
[1] This register must be programmed such that the following formula is valid.
VDPS + VDP < VT
[2] For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

Vertical Display Period Register 0 REG[1Ch]							Read/Write
Vertical Display Period Bits 7-0							
7	6	5	4	3	2	1	0

Vertical Display Period Register 1 REG[1Dh]							Read/Write
n/a						Vertical Display Period Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 Vertical Display Period Bits [9:0]
These bits specify the LCD panel Vertical Display period, in 1 line resolution. The Vertical Display period should be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

Vertical Display Period in number of lines = (REG[1Ch] bits 7:0, REG[1Dh] bits 1:0) + 1

Note
For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

Vertical Display Period Start Position Register 0 REG[1Eh]							Read/Write
Vertical Display Period Start Position Bits 7-0							
7	6	5	4	3	2	1	0

Vertical Display Period Start Position Register 1 REG[1Fh]							Read/Write
n/a						Vertical Display Period Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 Vertical Display Period Start Position Bits [9:0]
These bits specify the Vertical Display Period Start Position for panels in 1 line resolution.

For passive LCD panels these bits must be set to 00h.

For TFT panels, VDPS is calculated using the following formula.
VDPS = (REG[1Fh] bits 1-0, REG[1Eh] bits 7-0)

Note
[1] This register must be programmed such that the following formula is valid.
VDPS + VDP < VT
[2] For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

FPLINE Pulse Width Register REG[20h]							Read/Write
FPLINE Pulse Polarity	FPLINE Pulse Width Bits 6-0						
7	6	5	4	3	2	1	0

bit 7 FPLINE Pulse Polarity
This bit selects the polarity of the horizontal sync signal. For passive panels, this bit must be set to 1. For TFT panels, this bit is set according to the horizontal sync signal of the panel (typically FPLINE or LP).
When this bit = 0, the horizontal sync signal is active low.
When this bit = 1, the horizontal sync signal is active high.

bits 6-0 FPLINE Pulse Width Bits [6:0]
These bits specify the width of the panel horizontal sync signal, in 1 pixel resolution. The horizontal sync signal is typically FPLINE or LP, depending on the panel type.

FPLINE Pulse Width in number of pixels = (REG[20h] bits 6:0) + 1

Note
For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

FPLINE Pulse Start Position Register 0 REG[22h] Read/Write							
FPLINE Pulse Start Position Bits 7-0							
7	6	5	4	3	2	1	0

FPLINE Pulse Start Position Register 1 REG[23h] Read/Write							
n/a						FPLINE Pulse Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 FPLINE Pulse Start Position Bits [9:0]
These bits specify the start position of the horizontal sync signal, in 1 pixel resolution.

FPLINE Pulse Start Position in pixels = (REG[23h] bits 1-0, REG[22h] bits 7-0) + 1

Note
For passive panels, these bits must be programmed such that the following formula is valid.
HPW + HPS < HT

Note
For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

FPFRAME Pulse Width Register REG[24h] Read/Write							
FPFRAME Pulse Polarity	n/a				FPFRAME Pulse Width Bits 2-0		
7	6	5	4	3	2	1	0

bit 7 FPFRAME Pulse Polarity
This bit selects the polarity of the vertical sync signal. For passive panels, this bit must be set to 1. For TFT panels, this bit is set according to the horizontal sync signal of the panel (typically FPFRAME, SPS or DY).
When this bit = 0, the vertical sync signal is active low.
When this bit = 1, the vertical sync signal is active high.

bits 2-0 FPFRAME Pulse Width Bits [2:0]
These bits specify the width of the panel vertical sync signal, in 1 line resolution. The vertical sync signal is typically FPFRAME, SPS or DY, depending on the panel type.

FPFRAME Pulse Width in number of lines = (REG[24h] bits 2:0) + 1

Note
For panel AC timing and timing parameter definitions, see Section 6.4, “Display Interface” on page 56.

FPFRAME Pulse Start Position Register 0 REG[26h]							Read/Write
FPFRAME Pulse Start Position Bits 7-0							
7	6	5	4	3	2	1	0

FPFRAME Pulse Start Position Register 1 REG[27h]							Read/Write
n/a						FPFRAME Pulse Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 FPFRAME Pulse Start Position Bits [9:0]
These bits specify the start position of the vertical sync signal, in 1 line resolution.

For passive panels, these bits must be set to 00h.

For TFT/HR-TFT/D-TFD panels, VDPS is calculated using the following formula:
VPS = (REG[27h] bits 1-0, REG[26h] bits 7-0)

Note
For panel AC timing and timing parameter definitions, see Section 6.4, "Display Interface" on page 56.

D-TFD GCP Index Register REG[28h]							Read/Write
n/a			D-TFD GCP Index Bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 D-TFD GCP Index Bits [4:0]
For D-TFD panels only. These bits form the index that points to 32 8-bit GCP data registers.

D-TFD GCP Data Register REG[2Ch]							Read/Write
D-TFD GCP Data Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 D-TFD GCP Data Bits [7:0]
For D-TFD panel only. This register stores the data to be written to the GCP data bits and is controlled by the D-TFD GCP Index register (REG[28h]). For further information on the use of this register, see *Connecting to the Epson D-TFD Panels*, document number X31B-G-012-xx.

Note
The Panel Type bits (REG[10h] bits 1:0) must be set to 11 (D-TFD) for the GCP Data bits to have any hardware effect.

8.3.5 Display Mode Registers

Display Mode Register REG[70h]							Read/Write
Display Blank	Dithering Disable	Hardware Video Invert Enable	Software Video Invert	n/a	Bit-per-pixel Select Bits 2-0		
7	6	5	4	3	2	1	0

bit 7 Display Blank
When this bit = 0, the LCD display pipeline is enabled.
When this bit = 1, the LCD display pipeline is disabled and all LCD data outputs are forced to zero (i.e., the screen is blanked).

bit 6 Dithering Disable
Dithering allows 64 intensity levels for each color component (RGB). In monochrome modes where only the Green color component of the Look-Up-Table is used, 64 shades of gray are available for each position used in the LUT. In color modes, 64 shades of color are available for each color component resulting in 256K possible color combinations.
When this bit = 0, dithering is enabled for passive LCD panels.
When this bit = 1, dithering is disabled for passive LCD panels.

Note
This bit does not refer to the number of simultaneously displayed colors but rather the maximum available colors (refer to Table 8-9: “LCD Bit-per-pixel Selection,” on page 111 for the maximum number of simultaneously displayed colors).

bit 5 Hardware Video Invert Enable
This bit allows the Video Invert feature to be controlled using the General Purpose IO pin GPIO0. **This option is not available if configured for a HR-TFT or D-TFD as GPIO0 is used as an LCD control signal by both panels.**
When this bit = 0, GPIO0 has no effect on the video data.
When this bit = 1, video data may be inverted via GPIO0.

Note
The S1D13706 requires some configuration before the hardware video invert feature can be enabled.
- CNF3 must be set to 1 at RESET#
- GPIO Pin Input Enable (REG[A9h] bit 7) must be set to 1
- GPIO0 Pin IO Configuration (REG[A8h] bit 0) must be set to 0

If Hardware Video Invert is not available (i.e. HR-TFT panel is used), the video invert function can be controlled by software using REG[70h] bit 4. The following table summarizes the video invert options available.

Table 8-8: Inverse Video Mode Select Options

Hardware Video Invert Enable	Software Video Invert	GPIO0	Video Data
0	0	X	Normal
0	1	X	Inverse
1	X	0	Normal
1	X	1	Inverse

Note
Video data is inverted after the Look-Up Table.

bit 4 Software Video Invert
When this bit = 0, video data is normal.
When this bit = 1, video data is inverted.
See Table 8-8: “Inverse Video Mode Select Options”.

Note
Video data is inverted after the Look-Up Table

bits 2-0 Bit-per-pixel Select Bits [2:0]
These bits select the color depth (bit-per-pixel) for the displayed data for both the main window and the PIP+ window (if active).

Note
1, 2, 4 and 8 bpp color depths use the 18-bit LUT, allowing a maximum number of 256K available colors on TFT panels. 16 bpp mode bypasses the LUT, allowing a maximum of only 64K available colors.

Table 8-9: LCD Bit-per-pixel Selection

Bit-per-pixel Select Bits [2:0]	Color Depth (bpp)	Maximum Number of Available Colors/Shades		Max. No. Of Simultaneously Displayed Colors/Shades
		Passive Panel (Dithering On)	TFT Panel	
000	1 bpp	64K/64	256K/64	2/2
001	2 bpp	64K/64	256K/64	4/4
010	4 bpp	64K/64	256K/64	16/16
011	8 bpp	64K/64	256K/64	256/64
100	16 bpp	64K/64	64K/64	64K/64
101, 110, 111	Reserved			

Special Effects Register REG[71h]							Read/Write
Display Data Word Swap	Display Data Byte Swap	n/a	PIP+ Window Enable	n/a		SwivelView Mode Select Bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Display Data Word Swap
The display pipe fetches 32-bits of data from the display buffer. This bit enables the lower 16-bit word and the upper 16-bit word to be swapped before sending them to the LCD display. If the Display Data Byte Swap bit is also enabled, then the byte order of the fetched 32-bit data is reversed.

Note
For further information on byte swapping for Big Endian mode, see Section 14, “Big-Endian Bus Interface” on page 146.

bit 6 Display Data Byte Swap
The display pipe fetches 32-bits of data from the display buffer. This bit enables byte 0 and byte 1 to be swapped, and byte 2 and byte 3 to be swapped, before sending them to the LCD display. If the Display Data Word Swap bit is also enabled, then the byte order of the fetched 32-bit data is reversed.

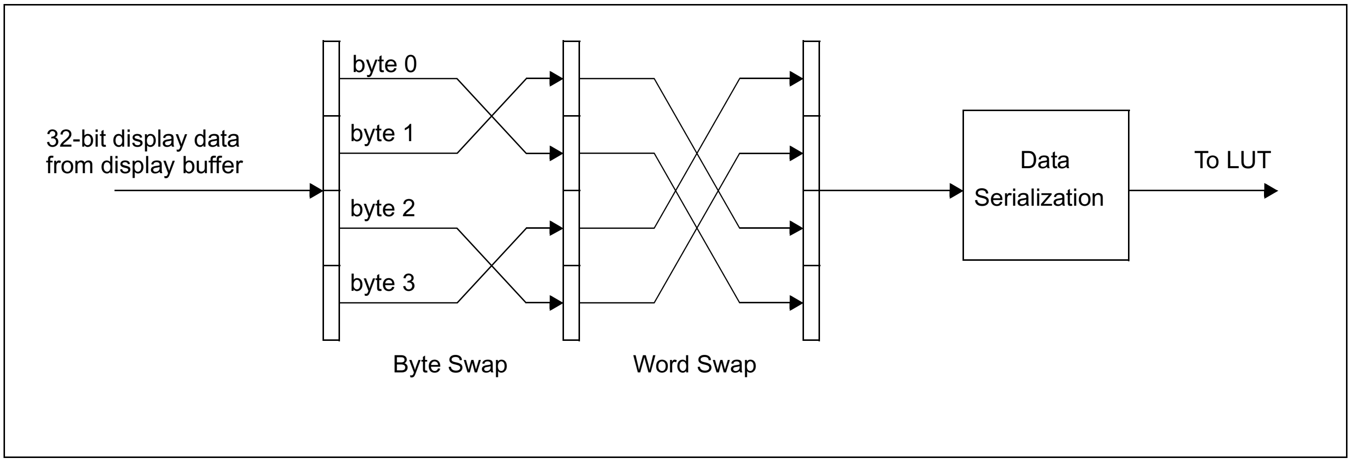


Figure 8-1: Display Data Byte/Word Swap

Note
For further information on byte swapping for Big Endian mode, see Section 14, “Big-Endian Bus Interface” on page 146.

bit 4 Picture-in-Picture Plus (PIP$^+$) Window Enable
This bit enables the PIP$^+$ window within the main window used for the Picture-in-Picture Plus feature. The location of the PIP$^+$ window within the landscape window is determined by the PIP$^+$ Window X Position registers (REG[84h], REG[85h], REG[8Ch], REG[8Dh]) and PIP$^+$ Window Y Position registers (REG[88h], REG[89h], REG[90h], REG[91h]). The PIP$^+$ window has its own Display Start Address register (REG[7Ch], REG[7Dh], REG[7Eh]) and Memory Address Offset register (REG[80h], REG[81h]). The PIP$^+$ window shares the same color depth and SwivelView™ orientation as the main window.

bit 1-0 SwivelView Mode Select Bits [1:0]
These bits select different SwivelView™ orientations:

Table 8-10: SwivelView™ Mode Select Options

SwivelView Mode Select Bits	SwivelView Orientation
00	0° (Normal)
01	90°
10	180°
11	270°

Main Window Display Start Address Register 0 REG[74h]							Read/Write
Main window Display Start Address Bits 7-0							
7	6	5	4	3	2	1	0

Main Window Display Start Address Register 1 REG[75h]							Read/Write
Main window Display Start Address Bits 15-8							
7	6	5	4	3	2	1	0

Main Window Display Start Address Register 2 REG[76h]							Read/Write
n/a							Main window Display Start Address Bit 16
7	6	5	4	3	2	1	0

bits 16-0 Main Window Display Start Address Bits [16:0]
This register specifies the starting address, in DWORDS, for the LCD image in the display buffer for the main window.

Note that this is a double-word (32-bit) address. An entry of 00000h into these registers represents the first double-word of display memory, an entry of 00001h represents the second double-word of the display memory, and so on. Calculate the Display Start Address as follows:

Main Window Display Start Address bits 16:0
= image address ÷ 4 (valid only for SwivelView 0°)

Note

For information on setting this register for other SwivelView orientations, see Section 12, “SwivelView™” on page 138.

Main Window Line Address Offset Register 0 REG[78h]							Read/Write
Main window Line Address Offset Bits 7-0							
7	6	5	4	3	2	1	0

Main Window Line Address Offset Register 1 REG[79h]							Read/Write
n/a						Main window Line Address Offset Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 Main Window Line Address Offset Bits [9:0]
This register specifies the offset, in DWORDS, from the beginning of one display line to the beginning of the next display line in the main window. **Note that this is a 32-bit address increment.** Calculate the Line Address Offset as follows:

Main Window Line Address Offset bits 9:0
= display width in pixels ÷ (32 ÷ bpp)

Note
A virtual display can be created by programming this register with a value greater than the formula requires. When a virtual display is created the image width is larger than the display width and the displayed image becomes a window into the larger virtual image.

8.3.6 Picture-in-Picture Plus (PIP+) Registers

PIP+ Window Display Start Address Register 0 REG[7C]							Read/Write
PIP+ Window Display Start Address Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window Display Start Address Register 1 REG[7Dh]							Read/Write
PIP+ Window Display Start Address Bits 15-8							
7	6	5	4	3	2	1	0

PIP+ Window Display Start Address Register 2 REG[7Eh]							Read/Write
n/a							PIP+ Window Display Start Address Bit 16
7	6	5	4	3	2	1	0

bits 16-0 PIP+ Window Display Start Address Bits [16:0]
These bits form the 17-bit address for the starting double-word of the PIP+ window.

Note that this is a double-word (32-bit) address. An entry of 00000h into these registers represents the first double-word of display memory, an entry of 00001h represents the second double-word of the display memory, and so on.

Note
These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).

PIP+ Window Line Address Offset Register 0 REG[80h]							Read/Write
PIP+ Window Line Address Offset Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window Line Address Offset Register 1 REG[81h]							Read/Write
n/a						PIP+ Window Line Address Offset Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window Line Address Offset Bits [9:0]
These bits are the LCD display's 10-bit address offset from the starting double-word of line "n" to the starting double-word of line "n + 1" for the PIP+ window. **Note that this is a 32-bit address increment.**

Note
These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).

PIP+ Window X Start Position Register 0 REG[84h]							Read/Write
PIP+ Window X Start Position Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window X Start Position Register 1 REG[85h]							Read/Write
n/a						PIP+ Window X Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window X Start Position Bits [9:0]

These bits determine the X start position of the PIP+ window in relation to the origin of the panel. Due to the S1D13706 SwivelView feature, the X start position may not be a horizontal position value (only true in 0° and 180° SwivelView). For further information on defining the value of the X Start Position register, see Section 13, “Picture-in-Picture Plus (PIP+)” on page 143.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the X start position is incremented by *x* pixels where *x* is relative to the current color depth.

Table 8-11: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (x)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

For 90° and 270° SwivelView the X start position is incremented in 1 line increments.

Depending on the color depth, some of the higher bits in this register are unused because the maximum horizontal display width is 1024 pixels.

Note

[1] These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).

[2] The effect of REG[84h] through REG[91h] takes place only after REG[91h] is written and at the next vertical non-display period.

PIP+ Window Y Start Position Register 0 REG[88h]							Read/Write
PIP+ Window Y Start Position Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window Y Start Position Register 1 REG[89h]							Read/Write
n/a						PIP+ Window Y Start Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window Y Start Position Bits [9:0]
These bits determine the Y start position of the PIP+ window in relation to the origin of the panel. Due to the S1D13706 SwivelView feature, the Y start position may not be a vertical position value (only true in 0° and 180° SwivelView). For further information on defining the value of the Y Start Position register, see Section 13, “Picture-in-Picture Plus (PIP+)” on page 143.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the Y start position is incremented in 1 line increments. For 90° and 270° SwivelView the Y start position is incremented by *y* pixels where *y* is relative to the current color depth.

Table 8-12: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (y)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

Depending on the color depth, some of the higher bits in this register are unused because the maximum vertical display height is 1024 pixels.

Note
[1] These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).
[2] The effect of REG[84h] through REG[91h] takes place only after REG[91h] is written and at the next vertical non-display period.

PIP+ Window X End Position Register 0 REG[8Ch]							Read/Write
PIP+ Window X End Position Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window X End Position Register 1 REG[8Dh]							Read/Write
n/a						PIP+ Window X End Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0

PIP+ Window X End Position Bits [9:0]
These bits determine the X end position of the PIP+ window in relation to the origin of the panel. Due to the S1D13706 SwivelView feature, the X end position may not be a horizontal position value (only true in 0° and 180° SwivelView). For further information on defining the value of the X End Position register, see Section 13, "Picture-in-Picture Plus (PIP+)" on page 143.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the X end position is incremented by *x* pixels where *x* is relative to the current color depth.

Table 8-13: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (x)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

For 90° and 270° SwivelView the X end position is incremented in 1 line increments.

Depending on the color depth, some of the higher bits in this register are unused because the maximum horizontal display width is 1024 pixels.

Note

[1] These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).
[2] The effect of REG[84h] through REG[91h] takes place only after REG[91h] is written and at the next vertical non-display period.

PIP+ Window Y End Position Register 0 REG[90h]							Read/Write
PIP+ Window Y End Position Bits 7-0							
7	6	5	4	3	2	1	0

PIP+ Window Y End Position Register 1 REG[91h]							Read/Write
n/a						PIP+ Window Y End Position Bits 9-8	
7	6	5	4	3	2	1	0

bits 9-0 PIP+ Window Y End Position Bits [9:0]
These bits determine the Y end position of the PIP+ window in relation to the origin of the panel. Due to the S1D13706 SwivelView feature, the Y end position may not be a vertical position value (only true in 0° and 180° SwivelView). For further information on defining the value of the Y End Position register, see Section 13, “Picture-in-Picture Plus (PIP+)” on page 143.

The register is also incremented differently based on the SwivelView orientation. For 0° and 180° SwivelView the Y end position is incremented in 1 line increments. For 90° and 270° SwivelView the Y end position is incremented by *y* pixels where *y* is relative to the current color depth.

Table 8-14: 32-bit Address Increments for Color Depth

Color Depth	Pixel Increment (y)
1 bpp	32
2 bpp	16
4 bpp	8
8 bpp	4
16 bpp	2

Depending on the color depth, some of the higher bits in this register are unused because the maximum vertical display height is 1024 pixels.

Note
[1] These bits have no effect unless the PIP+ Window Enable bit is set to 1 (REG[71h] bit 4).
[2] The effect of REG[84h] through REG[91h] takes place only after REG[91h] is written and at the next vertical non-display period.

8.3.7 Miscellaneous Registers

Power Save Configuration Register REG[A0h]							Read/Write
Vertical Non-Display Period Status (RO)	n/a			Memory Controller Power Save Status (RO)	n/a		Power Save Mode Enable
7	6	5	4	3	2	1	0

bit 7 Vertical Non-Display Period Status
This is a read-only status bit.
When this bit = 0, the LCD panel output is in a Vertical Display Period.
When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 3 Memory Controller Power Save Status
This read-only status bit indicates the power save state of the memory controller.
When this bit = 0, the memory controller is powered up.
When this bit = 1, the memory controller is powered down and the MCLK source can be turned off.

Note
Memory writes are possible during power save mode because the S1D13706 dynamically enables the memory controller for display buffer writes.

bit 0 Power Save Mode Enable
When this bit = 1, the software initiated power save mode is enabled.
When this bit = 0, the software initiated power save mode is disabled.
At reset, this bit is set to 1. For a summary of Power Save Mode, see Section 15, "Power Save Mode" on page 149.

Note
Memory writes are possible during power save mode because the S1D13706 dynamically enables the memory controller for display buffer writes.

Reserved REG[A1h]							Read/Write
n/a							Reserved
7	6	5	4	3	2	1	0

bit 0 Reserved.
This bit must remain at 0.

Reserved REG[A2h]							Read/Write
Reserved	n/a						Reserved
7	6	5	4	3	2	1	0

bit 7 Reserved.
This bit must remain at 0.

bit 0 Reserved.
This bit must remain at 0.

Reserved REG[A3h]							Read/Write
Reserved	n/a						
7	6	5	4	3	2	1	0

bit 7 Reserved.
This bit must remain at 0.

Scratch Pad Register 0 REG[A4h]							Read/Write
Scratch Pad Bits 7-0							
7	6	5	4	3	2	1	0

Scratch Pad Register 1 REG[A5h]							Read/Write
Scratch Pad Bits 15-8							
7	6	5	4	3	2	1	0

bits 15-0 Scratch Pad Bits [15:0]
This register contains general purpose read/write bits. These bits have no effect on hardware.

8.3.8 General IO Pins Registers

General Purpose IO Pins Configuration Register 0 REG[A8h]							Read/Write
n/a	GPIO6 Pin IO Configuration	GPIO5 Pin IO Configuration	GPIO4 Pin IO Configuration	GPIO3 Pin IO Configuration	GPIO2 Pin IO Configuration	GPIO1 Pin IO Configuration	GPIO0 Pin IO Configuration
7	6	5	4	3	2	1	0

Note
[1] If CNF3 = 0 at RESET#, then all GPIO pins are configured as outputs only and this register has no effect. This case allows the GPIO pins to be used by the HR-TFT/D-TFD panel interfaces. For a summary of GPIO usage for HR-TFT/D-TFD, see Table 4-9: "LCD Interface Pin Mapping," on page 30.
[2] The input functions of the GPIO pins are not enabled until REG[A9h] bit 7 is set to 1.

bit 6 GPIO6 Pin IO Configuration
When this bit = 0 (default), GPIO6 is configured as an input pin.
When this bit = 1, GPIO6 is configured as an output pin.

bit 5 GPIO5 Pin IO Configuration
When this bit = 0 (default), GPIO5 is configured as an input pin.
When this bit = 1, GPIO5 is configured as an output pin.

bit 4 GPIO4 Pin IO Configuration
When this bit = 0 (default), GPIO4 is configured as an input pin.
When this bit = 1, GPIO4 is configured as an output pin.

bit 3 GPIO3 Pin IO Configuration
When this bit = 0 (default), GPIO3 is configured as an input pin.
When this bit = 1, GPIO3 is configured as an output pin.

bit 2 GPIO2 Pin IO Configuration
When this bit = 0 (default), GPIO2 is configured as an input pin.
When this bit = 1, GPIO2 is configured as an output pin.

bit 1 GPIO1 Pin IO Configuration
When this bit = 0 (default), GPIO1 is configured as an input pin.
When this bit = 1, GPIO1 is configured as an output pin.

bit 0 GPIO0 Pin IO Configuration
When this bit = 0 (default), GPIO0 is configured as an input pin.
When this bit = 1, GPIO0 is configured as an output pin.

General Purpose IO Pins Configuration Register 1 REG[A9h]							Read/Write
GPIO Pin Input Enable	n/a						
7	6	5	4	3	2	1	0

bit 7 GPIO Pin Input Enable
This bit is used to enable the input function of the GPIO pins. It must be changed to a 1 after power-on reset to enable the input function of the GPIO pins (default is 0).

General Purpose IO Pins Status/Control Register 0 REG[ACh] Read/Write							
n/a	GPIO6 Pin IO Status	GPIO5 Pin IO Status	GPIO4 Pin IO Status	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	GPIO0 Pin IO Status
7	6	5	4	3	2	1	0

Note
For information on GPIO pin mapping when HR-TFT/D-TFD panels are selected, see Table 4-9: “LCD Interface Pin Mapping,” on page 30.

bit 6 GPIO6 Pin IO Status
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO6 is configured as an output, writing a 1 to this bit drives GPIO6 high and writing a 0 to this bit drives GPIO6 low.
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO6 is configured as an input, a read from this bit returns the status of GPIO6.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO6 outputs the YSCLD signal automatically and writing to this bit has no effect.

bit 5 GPIO5 Pin IO Status
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO5 is configured as an output, writing a 1 to this bit drives GPIO5 high and writing a 0 to this bit drives GPIO5 low.
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO5 is configured as an input, a read from this bit returns the status of GPIO5.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11) and a 1 is written to this bit, the D-TFD signal DD_P1 signal is enabled.
When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11) and a 0 is written to this bit, the D-TFD signal DD_P1 signal is forced low.

bit 4 GPIO4 Pin IO Status
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO4 is configured as an output, writing a 1 to this bit drives GPIO4 high and writing a 0 to this bit drives GPIO4 low.
When a D-TFD panel is not selected (REG[10h] bits 1:0) and GPIO4 is configured as an input, a read from this bit returns the status of GPIO4.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO4 outputs the RES signal automatically and writing to this bit has no effect.

bit 3 GPIO3 Pin IO Status
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO3 is configured as an output, writing a 1 to this bit drives GPIO3 high and writing a 0 to this bit drives GPIO3 low.
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO3 is configured as an input, a read from this bit returns the status of GPIO3.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO3 outputs the FRS signal automatically and writing to this bit has no effect.

When a HR-TFT panel is enabled (REG[10h] bits 1:0 = 10), GPIO3 outputs the SPL signal automatically and writing to this bit has no effect.

bit 2 GPIO2 Pin IO Status
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO2 is configured as an output, writing a 1 to this bit drives GPIO2 high and writing a 0 to this bit drives GPIO2 low.
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO2 is configured as an input, a read from this bit returns the status of GPIO2.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO2 outputs the FR signal automatically and writing to this bit has no effect.

When a HR-TFT panel is enabled (REG[10h] bits 1:0 = 10), GPIO2 outputs the REV signal automatically and writing to this bit has no effect.

bit 1 GPIO1 Pin IO Status
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO1 is configured as an output, writing a 1 to this bit drives GPIO1 high and writing a 0 to this bit drives GPIO1 low.
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO1 is configured as an input, a read from this bit returns the status of GPIO1.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO1 outputs the YSCL signal automatically and writing to this bit has no effect.

When a HR-TFT panel is enabled (REG[10h] bits 1:0 = 10), GPIO1 outputs the CLS signal automatically and writing to this bit has no effect.

bit 0 GPIO0 Pin IO Status
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO0 is configured as an output, writing a 1 to this bit drives GPIO0 high and writing a 0 to this bit drives GPIO0 low.
When neither a D-TFD panel or a HR-TFT are selected (REG[10h] bits 1:0) and GPIO0 is configured as an input, a read from this bit returns the status of GPIO0.

When a D-TFD panel is enabled (REG[10h] bits 1:0 = 11), GPIO0 outputs the XINH signal automatically and writing to this bit has no effect.

When a HR-TFT panel is enabled (REG[10h] bits 1:0 = 10), GPIO0 outputs the PS signal automatically and writing to this bit has no effect.

General Purpose IO Pins Status/Control Register 1 REG[ADh]							Read/Write
GPO Control	n/a						
7	6	5	4	3	2	1	0

bit 7 GPO Control
This bit controls the General Purpose Output pin.
Writing a 0 to this bit drives GPO to low.
Writing a 1 to this bit drives GPO to high.

Note
Many implementations use the GPO pin to control the LCD bias power (see Section 6.3, "LCD Power Sequencing" on page 54).

8.3.9 Pulse Width Modulation (PWM) Clock and Contrast Voltage (CV) Pulse Configuration Registers

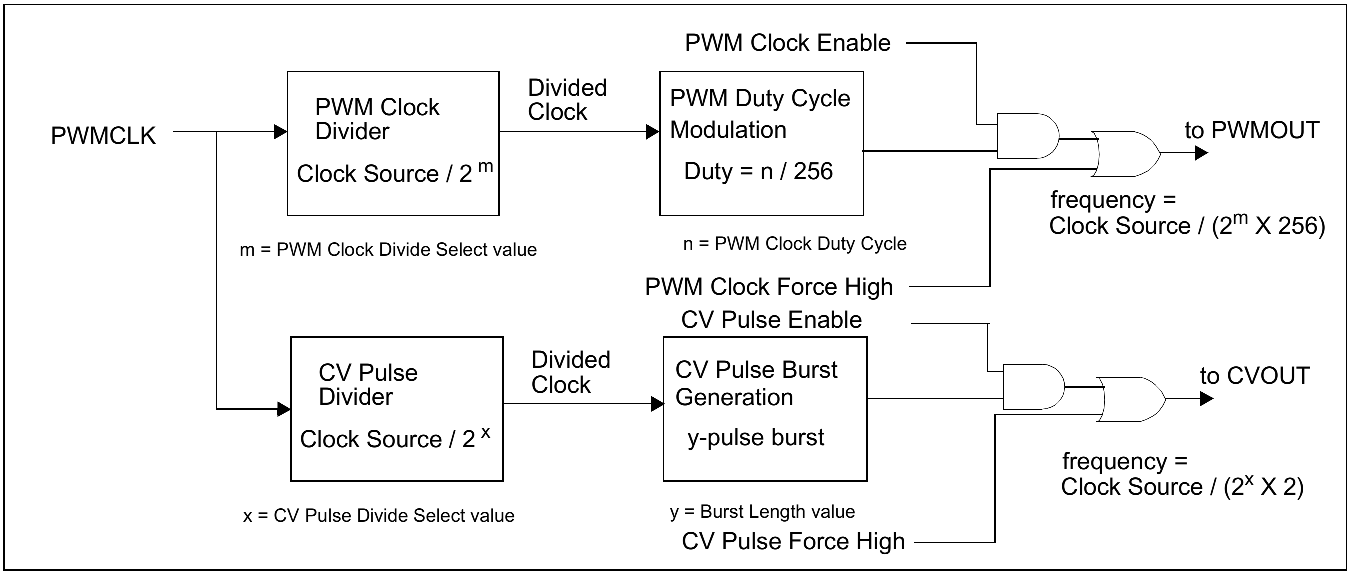


Figure 8-2: PWM Clock/CV Pulse Block Diagram

Note
For further information on PWMCLK, see Section 7.1.4, "PWMCLK" on page 92.

PWM Clock / CV Pulse Control Register REG[B0h]							Read/Write
PWM Clock Force High	n/a		PWM Clock Enable	CV Pulse Force High	CV Pulse Burst Status (RO)	CV Pulse Burst Start	CV Pulse Enable
7	6	5	4	3	2	1	0

bit 7 and bit 4 PWM Clock Force High (bit 7) and PWM Clock Enable (bit 4)
These bits control the PWMOUT pin and PWM Clock circuitry as follows.

Table 8-15: PWM Clock Control

Bit 7	**Bit 4**	**Result**
0	1	PWM Clock circuitry enabled (controlled by REG[B1h] and REG[B3h])
0	0	PWMOUT forced low
1	x	PWMOUT forced high

x = don't care

When PWMOUT is forced low or forced high it can be used as a general purpose output.

Note
The PWM Clock circuitry is disabled when Power Save Mode is enabled.

bit 3 and bit 0 — CV Pulse Force High (bit 3) and CV Pulse Enable (bit 0)
These bits control the CVOUT pin and CV Pulse circuitry as follows.

Table 8-16: CV Pulse Control

Bit 3	Bit 0	Result
0	1	CV Pulse circuitry enabled (controlled by REG[B1h] and REG[B2h])
0	0	CVOUT forced low
1	x	CVOUT forced high

x = don't care

When CVOUT is forced low or forced high it can be used as a general purpose output.

Note
[1] Bit 3 must be set to 0 and bit 0 must be set to 1 before initiating a new burst using the CV Pulse Burst Start bit.
[2] The CV Pulse circuitry is disabled when Power Save Mode is enabled.

bit 2 — CV Pulse Burst Status
This is a read-only bit. A "1" indicates a CV pulse burst is occurring. A "0" indicates no CV pulse burst is occurring. Software should wait for this bit to clear before starting another burst.

bit 1 — CV Pulse Burst Start
A 1 in this bit initiates a single CVOUT pulse burst. The number of clock pulses generated is programmable from 1 to 256. The frequency of the pulses is the divided CV Pulse source divided by 2, with 50/50 duty cycle. This bit should be cleared to 0 by software before initiating a new burst.

Note
This bit has effect only if the CV Pulse Enable bit is 1.

bit 0 — CV Pulse Enable
See description for bit 3.

PWM Clock / CV Pulse Configuration Register REG[B1h]							Read/Write
PWM Clock Divide Select Bits 3-0				CV Pulse Divide Select Bits 2-0			PWMCLK Source Select
7	6	5	4	3	2	1	0

bits 7-4 PWM Clock Divide Select Bits [3:0]
The value of these bits represents the power of 2 by which the selected PWM clock source is divided.

Table 8-17: PWM Clock Divide Select Options

PWM Clock Divide Select Bits [3:0]	PWM Clock Divide Amount
0h	1
1h	2
2h	4
3h	8
...	...
Ch	4096
Dh-Fh	Reserved

Note
This divided clock is further divided by 256 before it is output at PWMOUT.

bits 3-1 CV Pulse Divide Select Bits [2:0]
The value of these bits represents the power of 2 by which the selected CV Pulse source is divided.

Table 8-18: CV Pulse Divide Select Options

CV Pulse Divide Select Bits [2:0]	CV Pulse Divide Amount
0h	1
1h	2
2h	4
3h	8
...	...
7h	128

Note
This divided clock is further divided by 2 before it is output at the CVOUT.

bit 0 PWMCLK Source Select
When this bit = 0, the clock source for PWMCLK is CLKI.
When this bit = 1, the clock source for PWMCLK is CLKI2.

Note
For further information on the PWMCLK source select, see Section 7.2, “Clock Selection” on page 93.

CV Pulse Burst Length Register REG[B2h]							Read/Write
CV Pulse Burst Length Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 CV Pulse Burst Length Bits [7:0]
The value of this register determines the number of pulses generated in a single CV Pulse burst:

Number of pulses in a burst = (ContentsOfThisRegister) + 1

PWMOUT Duty Cycle Register REG[B3h]							Read/Write
PWMOUT Duty Cycle Bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PWMOUT Duty Cycle Bits [7:0]
This register determines the duty cycle of the PWMOUT output.

Table 8-19: PWMOUT Duty Cycle Select Options

PWMOUT Duty Cycle [7:0]	PWMOUT Duty Cycle
00h	Always Low
01h	High for 1 out of 256 clock periods
02h	High for 2 out of 256 clock periods
...	...
FFh	High for 255 out of 256 clock periods

9 Frame Rate Calculation

The following formula is used to calculate the display frame rate.

$$\text{FrameRate} = \frac{f_{PCLK}}{(HT) \times (VT)}$$

Where:

f_{PCLK} = PClk frequency (Hz)

HT = Horizontal Total
= ((REG[12h] bits 6-0) + 1) x 8 Pixels

VT = Vertical Total
= ((REG[19h] bits 1-0, REG[18h] bits 7-0) + 1) Lines

10 Display Data Formats

The following diagrams show the display mode data formats for a little-endian system.

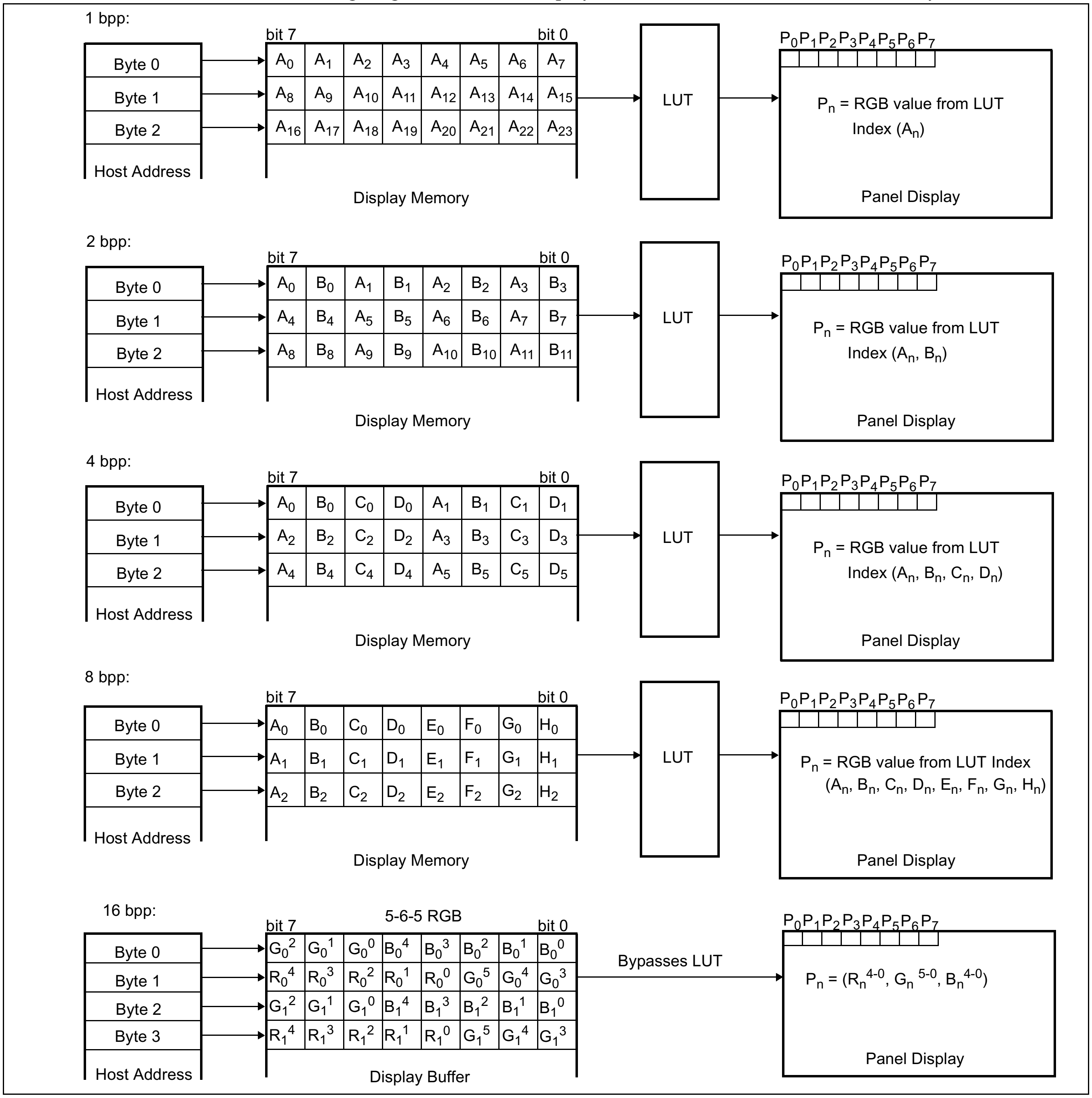


Figure 10-1: 4/8/16 Bit-Per-Pixel Display Data Memory Organization

Note

1. The Host-to-Display mapping shown here is for a little endian system.
2. For 16 bpp format, R_n, G_n, B_n represent the red, green, and blue color components.

11 Look-Up Table Architecture

The following figures are intended to show the display data output path only.

Note
When Video Data Invert is enabled the video data is inverted after the Look-Up Table.

11.1 Monochrome Modes

The green Look-Up Table (LUT) is used for all monochrome modes.

1 Bit-per-pixel Monochrome Mode

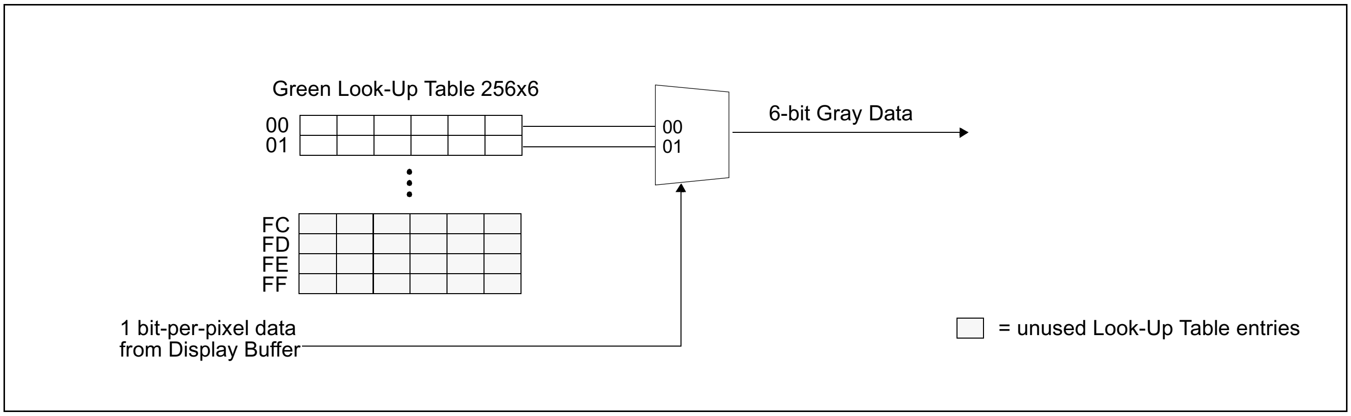


Figure 11-1: 1 Bit-per-pixel Monochrome Mode Data Output Path

2 Bit-per-pixel Monochrome Mode

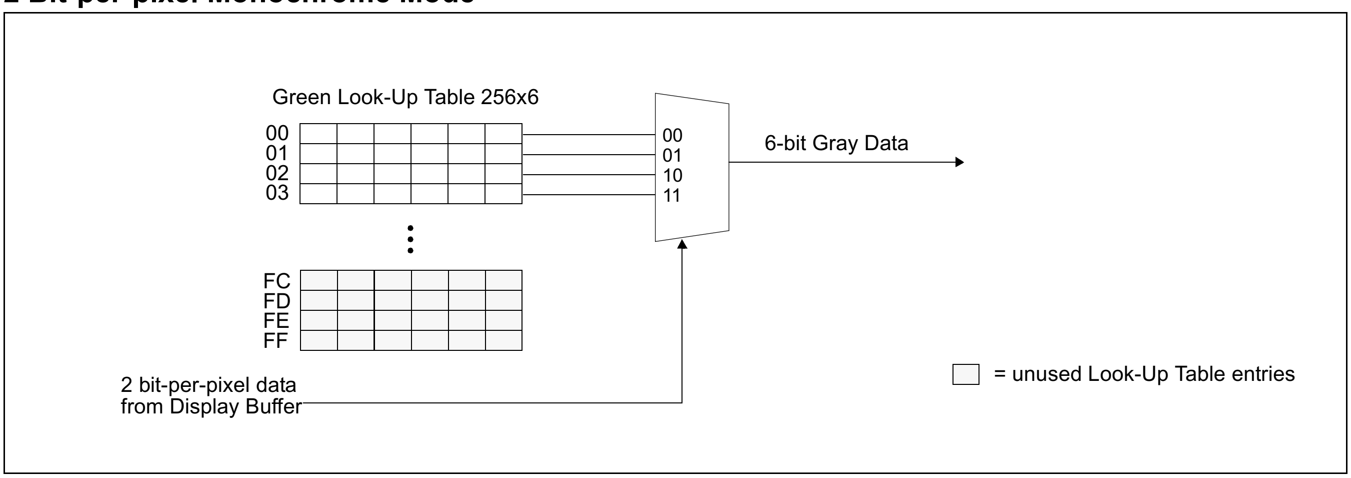


Figure 11-2: 2 Bit-per-pixel Monochrome Mode Data Output Path

4 Bit-per-pixel Monochrome Mode

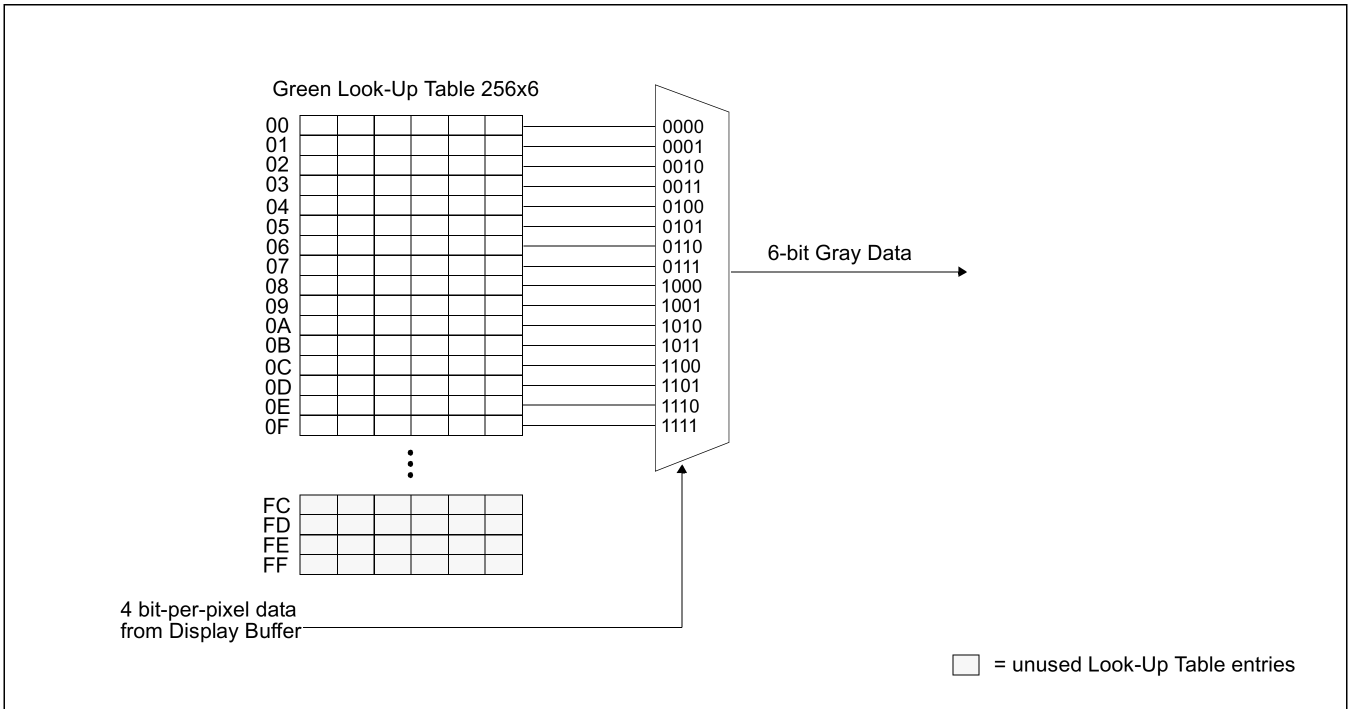


Figure 11-3: 4 Bit-per-pixel Monochrome Mode Data Output Path

8 Bit-per-pixel Monochrome Mode

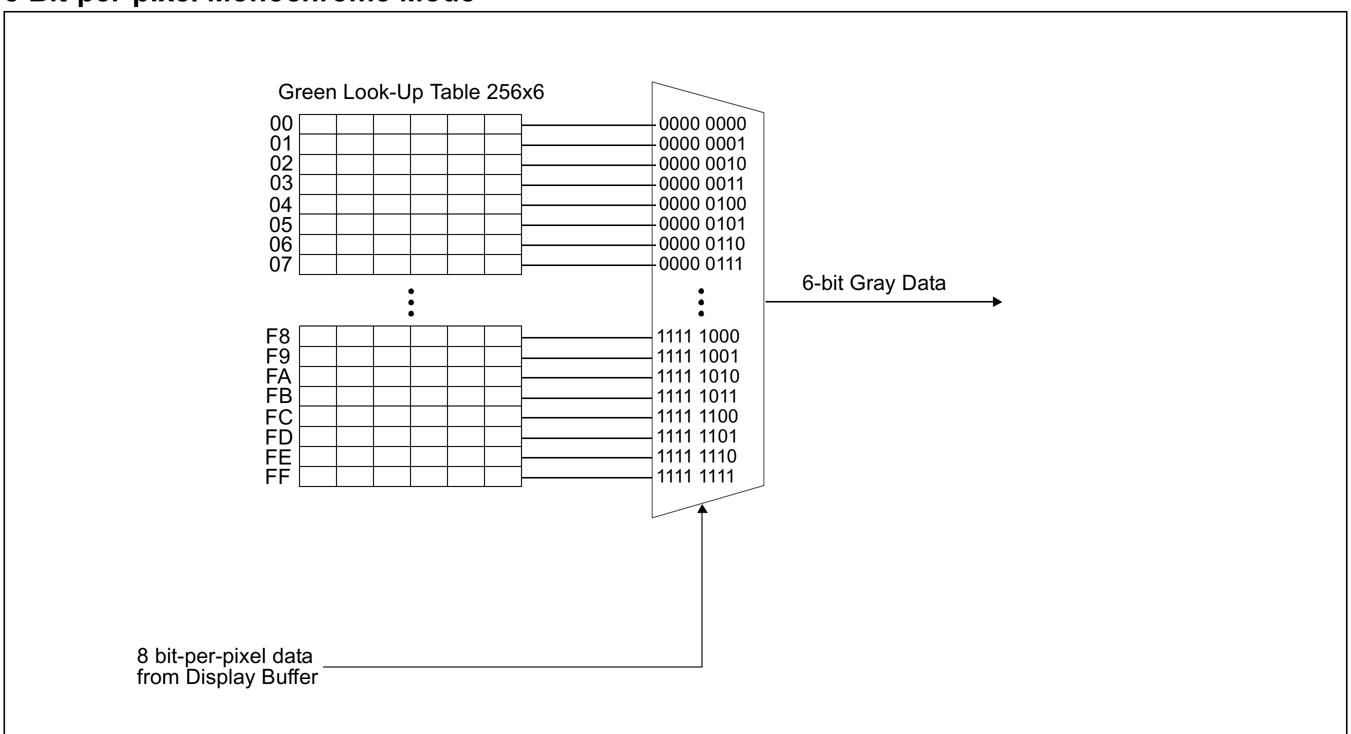


Figure 11-4: 8 Bit-per-pixel Monochrome Mode Data Output Path

16 Bit-Per-Pixel Monochrome Mode

The LUT is bypassed and the green data is directly mapped for this color depth– See “Display Data Formats” on page 131..

11.2 Color Modes

1 Bit-Per-Pixel Color

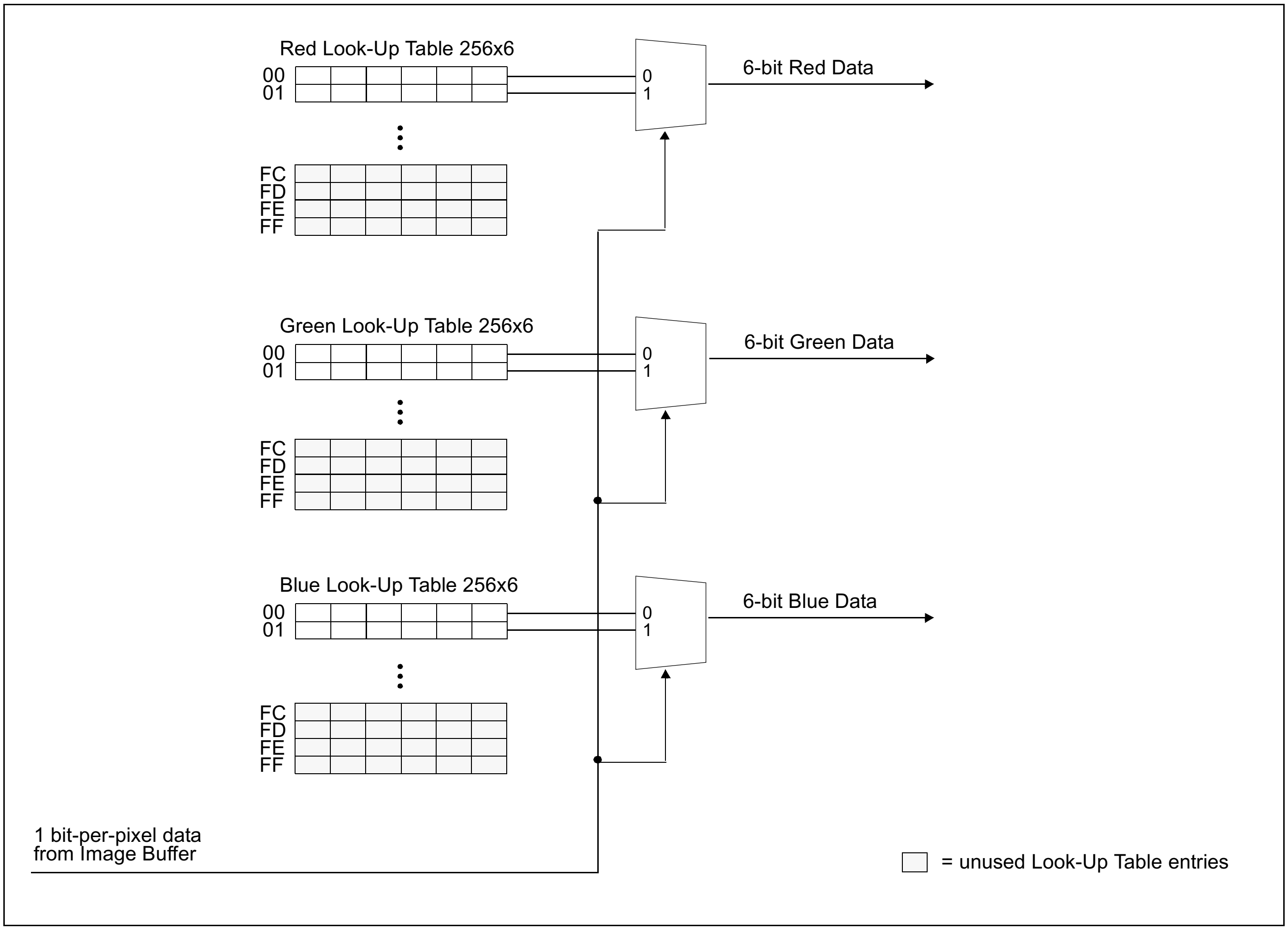


Figure 11-5: 1 Bit-Per-Pixel Color Mode Data Output Path

2 Bit-Per-Pixel Color

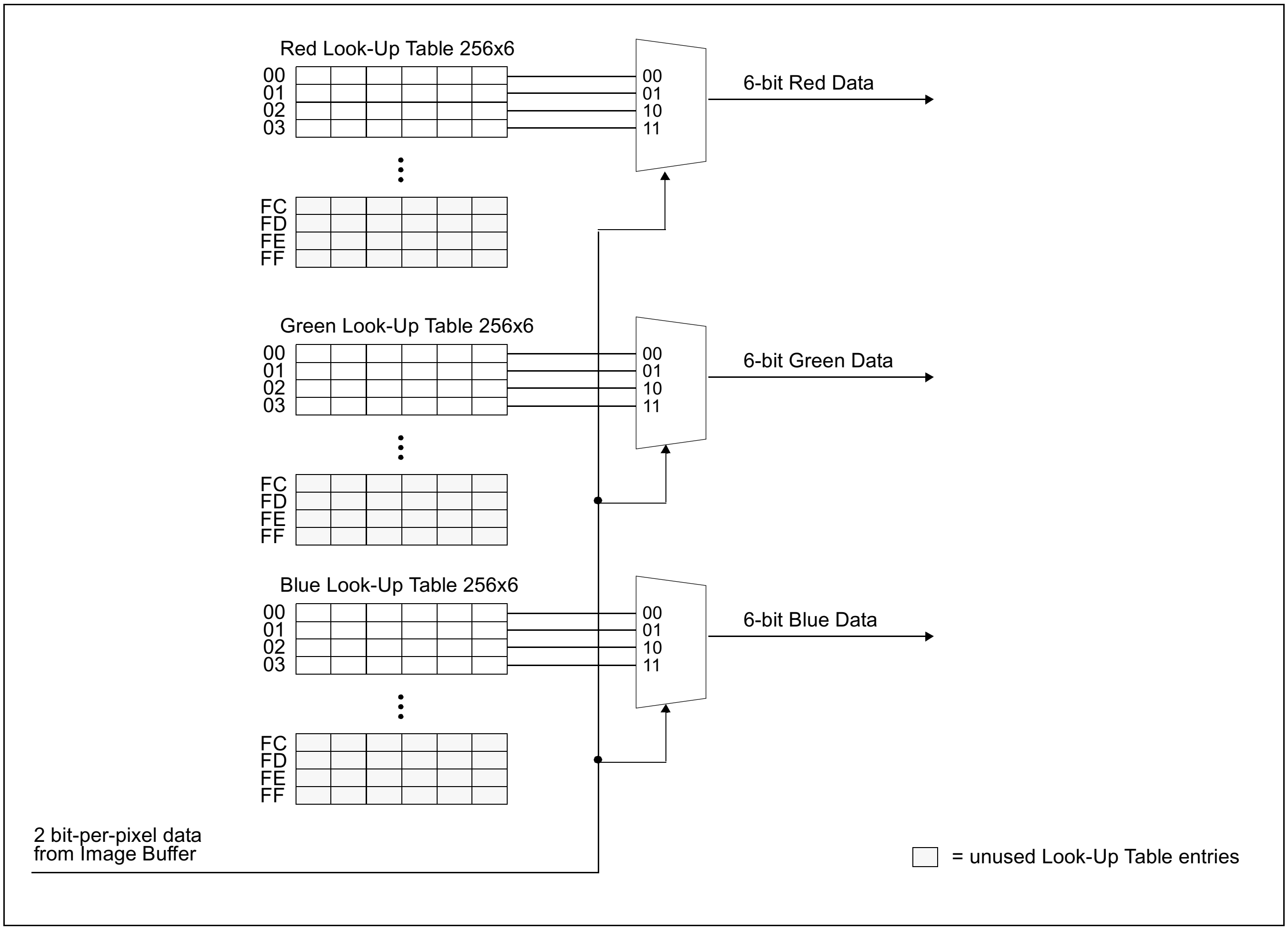


Figure 11-6: 2 Bit-Per-Pixel Color Mode Data Output Path

4 Bit-Per-Pixel Color

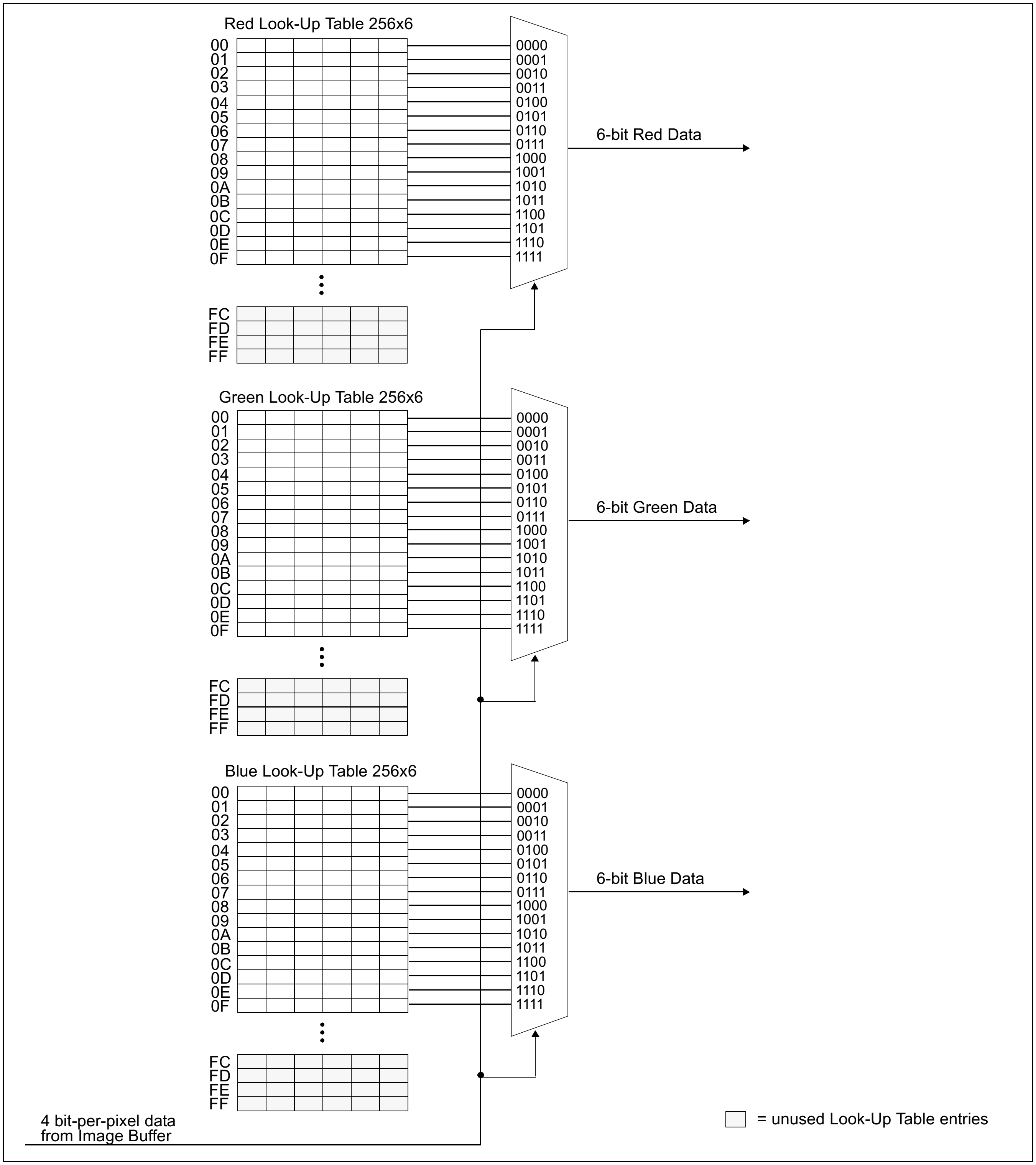


Figure 11-7: 4 Bit-Per-Pixel Color Mode Data Output Path

8 Bit-per-pixel Color Mode

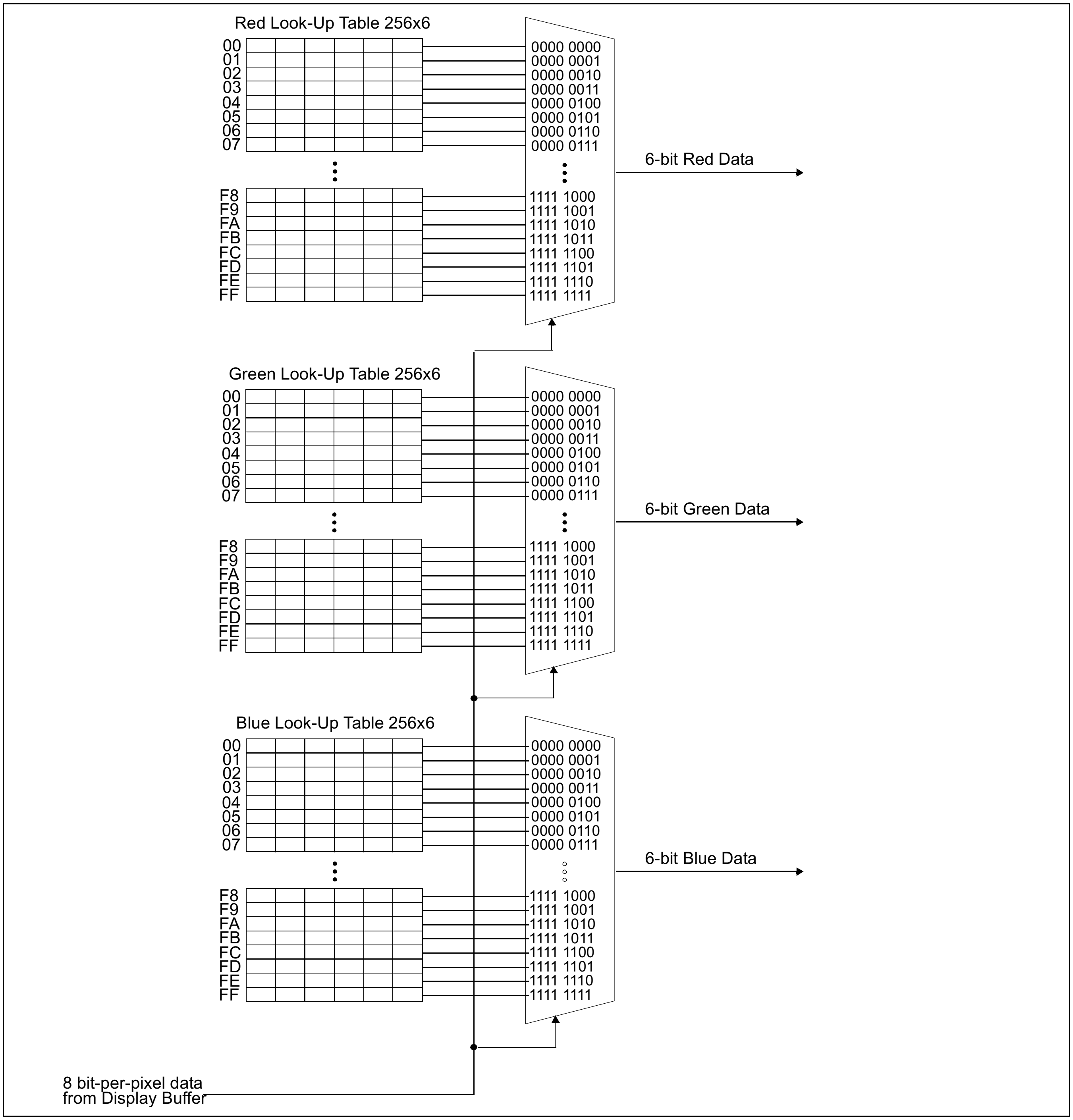


Figure 11-8: 8 Bit-per-pixel Color Mode Data Output Path

16 Bit-Per-Pixel Color Mode

The LUT is bypassed and the color data is directly mapped for this color depth– See “Display Data Formats” on page 131.

12 SwivelView™

12.1 Concept

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in an counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

The image is not actually rotated in the display buffer since there is no address translation during CPU read/write. The image is rotated during display refresh.

12.2 90° SwivelView™

90° SwivelView™ requires the Memory Clock (MCLK) to be at least 1.25 times the frequency of the Pixel Clock (PCLK), i.e. MCLK ≥ 1.25PCLK.

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13706 in the following sense: A–B–C–D. The display is refreshed by the S1D13706 in the following sense: B-D-A-C.

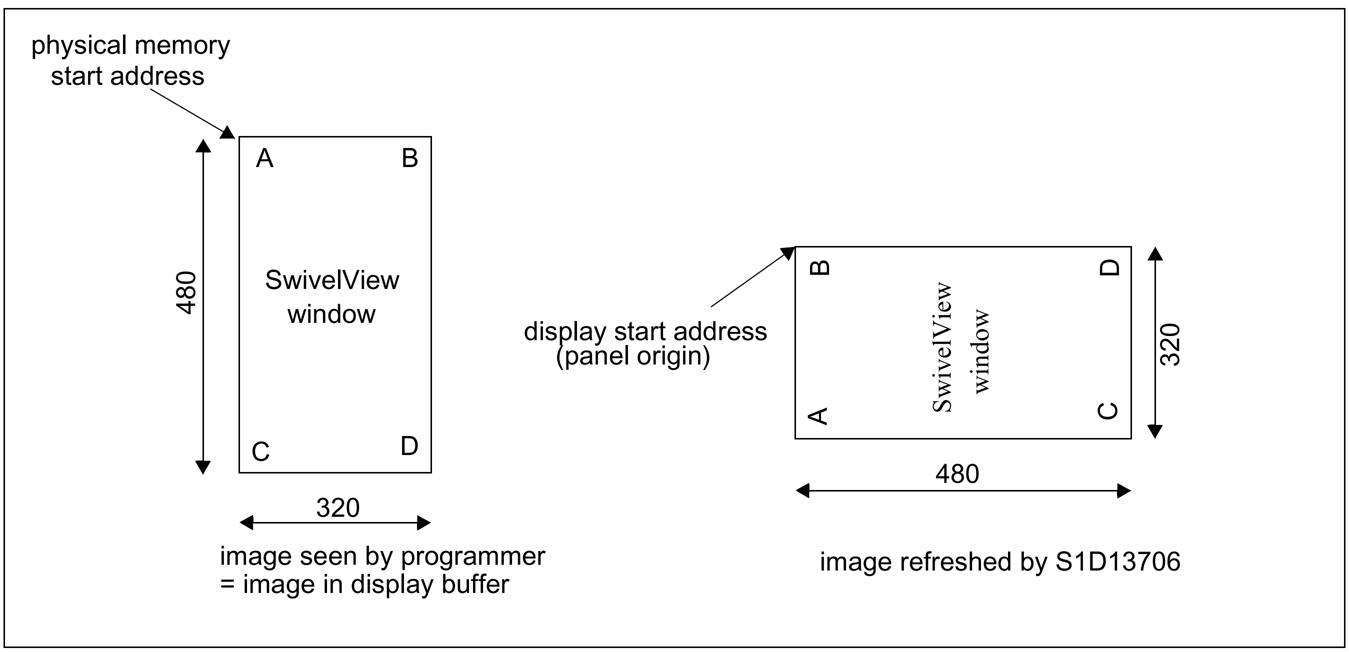


Figure 12-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView.

12.2.1 Register Programming

Enable 90° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[71h] bits 1:0) to 01.

Display Start Address

The display refresh circuitry starts at pixel “B”, therefore the Main Window Display Start Address registers (REG[74h], REG[75h], REG[76h]) must be programmed with the address of pixel “B”. To calculate the value of the address of pixel “B” use the following formula (assumes 8 bpp color depth).

Main Window Display Start Address bits 16:0
= ((image address + (panel height x bpp ÷ 8)) ÷ 4) - 1
= ((0 + (320 pixels x 8 bpp ÷ 8)) ÷ 4) -1
= 79 (4Fh)

Line Address Offset

The Main Window Line Address Offset registers (REG[78h], REG[79h]) is based on the display width and programmed using the following formula.

Main Window Line Address Offset bits 9:0
= display width in pixels ÷ (32 ÷ bpp)
= 320 pixels ÷ 32 ÷ 8 bpp
= 80 (50h)

12.3 180° SwivelView™

The following figure shows how the programmer sees a 480x320 landscape image and how the image is being displayed. The application image is written to the S1D13706 in the following sense: A–B–C–D. The display is refreshed by the S1D13706 in the following sense: D-C-B-A.

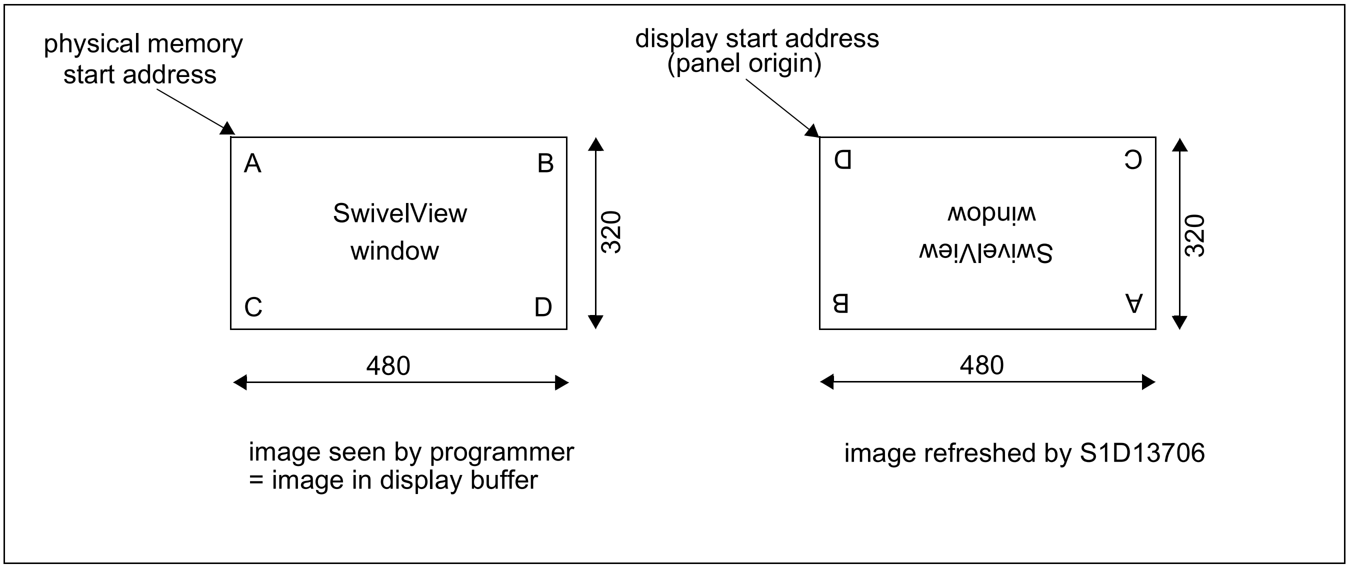


Figure 12-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView.

12.3.1 Register Programming

Enable 180° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[71h] bits 1:0) to 10.

Display Start Address

The display refresh circuitry starts at pixel “D”, therefore the Main Window Display Start Address registers (REG[74h], REG[75h], REG[76h]) must be programmed with the address of pixel “D”. To calculate the value of the address of pixel “D” use the following formula (assumes 8 bpp color depth).

Main Window Display Start Address bits 16:0
= ((image address + (offset x (panel height - 1) + panel width) x bpp ÷ 8) ÷ 4) - 1
= ((0 + (480 pixels x 319 pixels + 480 pixels) x 8 bpp ÷ 8) ÷ 4) - 1
= 38399 (95FFh)

Line Address Offset

The Main Window Line Address Offset registers (REG[78h], REG[79h]) is based on the display width and programmed using the following formula.

Main Window Line Address Offset bits 9:0
= display width in pixels ÷ (32 ÷ bpp)
= 480 pixels ÷ 32 ÷ 8 bpp
= 120 (78h)

12.4 270° SwivelView™

270° SwivelView™ requires the Memory Clock (MCLK) to be at least 1.25 times the frequency of the Pixel Clock (PCLK), i.e. MCLK ≥ 1.25PCLK.

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13706 in the following sense: A–B–C–D. The display is refreshed by the S1D13706 in the following sense: C-A-D-B.

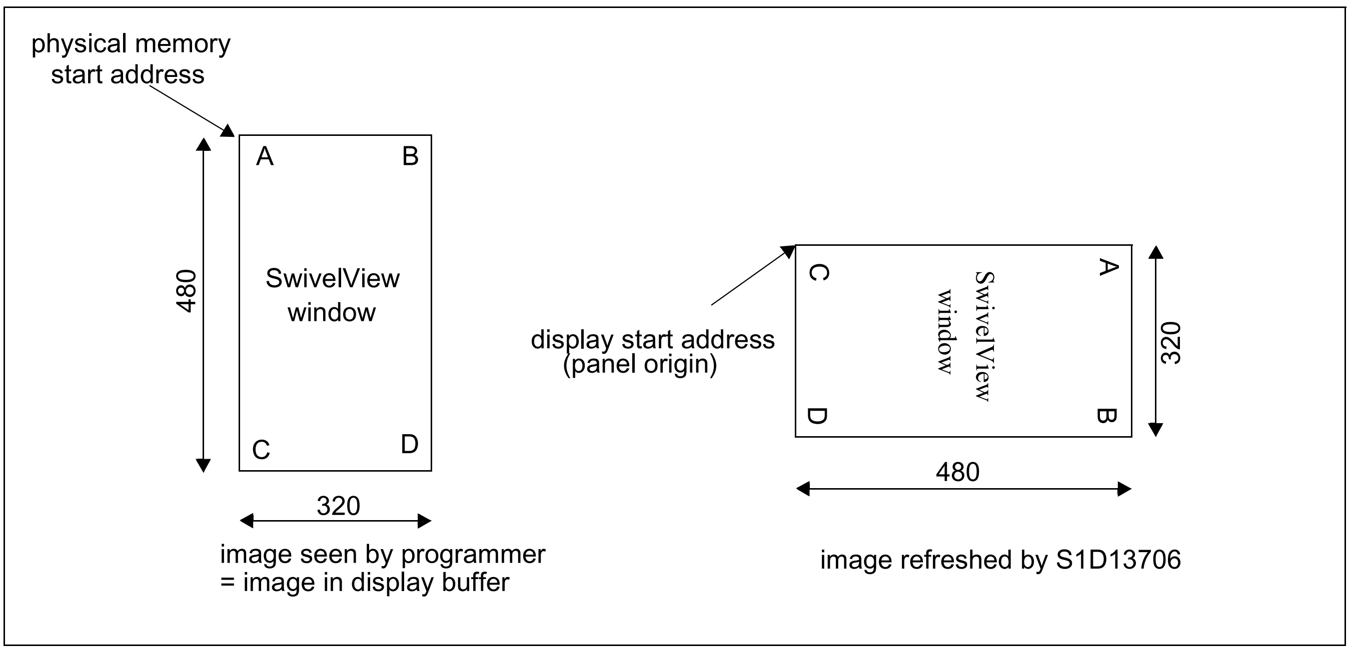


Figure 12-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView.

12.4.1 Register Programming

Enable 270° SwivelView™ Mode

Set SwivelView™ Mode Select bits (REG[71h] bits 1:0) to 11.

The display refresh circuitry starts at pixel "C", therefore the Main Window Display Start Address registers (REG[74h], REG[75h], REG[76h]) must be programmed with the address of pixel "C". To calculate the value of the address of pixel "C" use the following formula (assumes 8 bpp color depth).

Main Window Display Start Address bits 16:0
= (image address + ((panel width - 1) x offset x bpp ÷ 8) ÷ 4)
= (0 + ((480 pixels - 1) x 320 pixels x 8 bpp ÷ 8) ÷ 4)
= 38320 (95B0h)

Line Address Offset

The Main Window Line Address Offset registers (REG[78h], REG[79h]) is based on the display width and programmed using the following formula.

Main Window Line Address Offset bits 9:0
= display width in pixels ÷ (32 ÷ bpp)
= 320 pixels ÷ 32 ÷ 8 bpp
= 80 (50h)

13 Picture-in-Picture Plus (PIP$^+$)

13.1 Concept

Picture-in-Picture Plus enables a secondary window (or PIP$^+$ window) within the main display window. The PIP$^+$ window may be positioned anywhere within the virtual display and is controlled through the PIP$^+$ window control registers (REG[7Ch] through REG[91h]). The PIP$^+$ window retains the same color depth and SwivelView orientation as the main window.

The following diagram shows an example of a PIP$^+$ window within a main window and the registers used to position it.

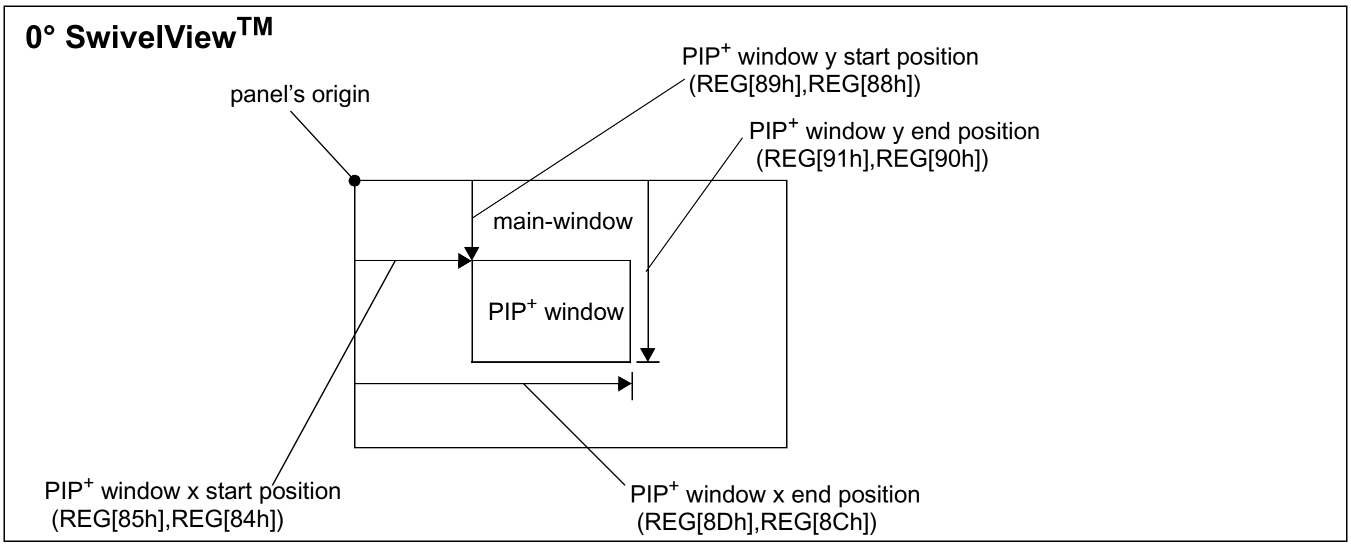


Figure 13-1: Picture-in-Picture Plus with SwivelView disabled

13.2 With SwivelView Enabled

13.2.1 SwivelView 90°

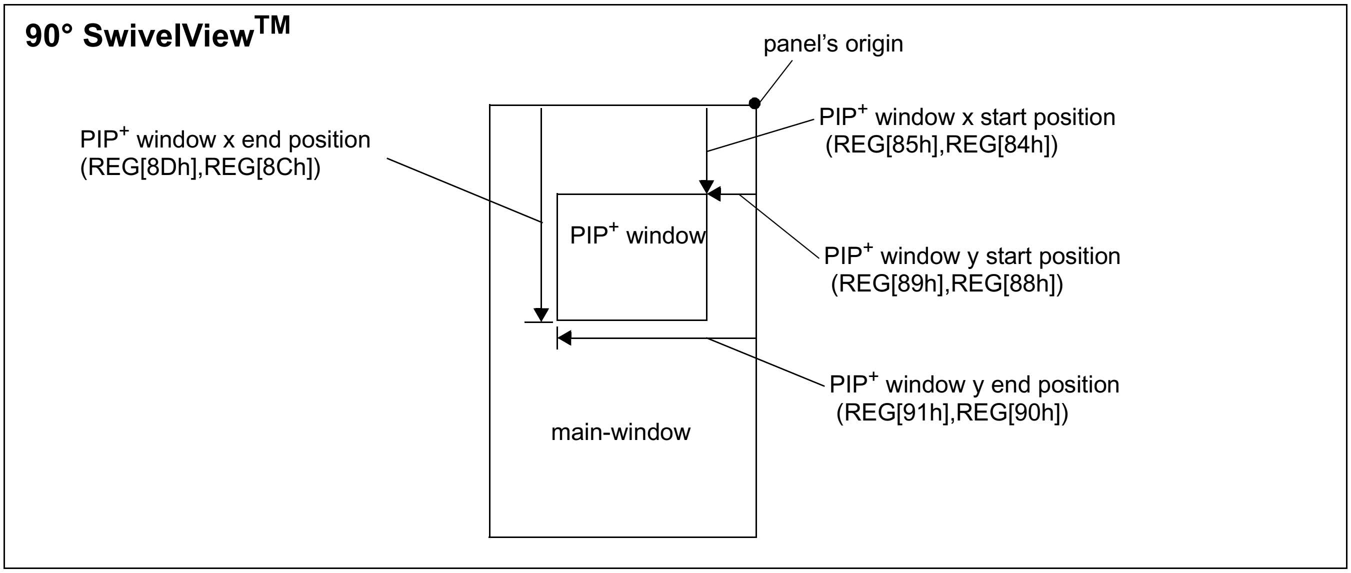


Figure 13-2: Picture-in-Picture Plus with SwivelView 90° enabled

13.2.2 SwivelView 180°

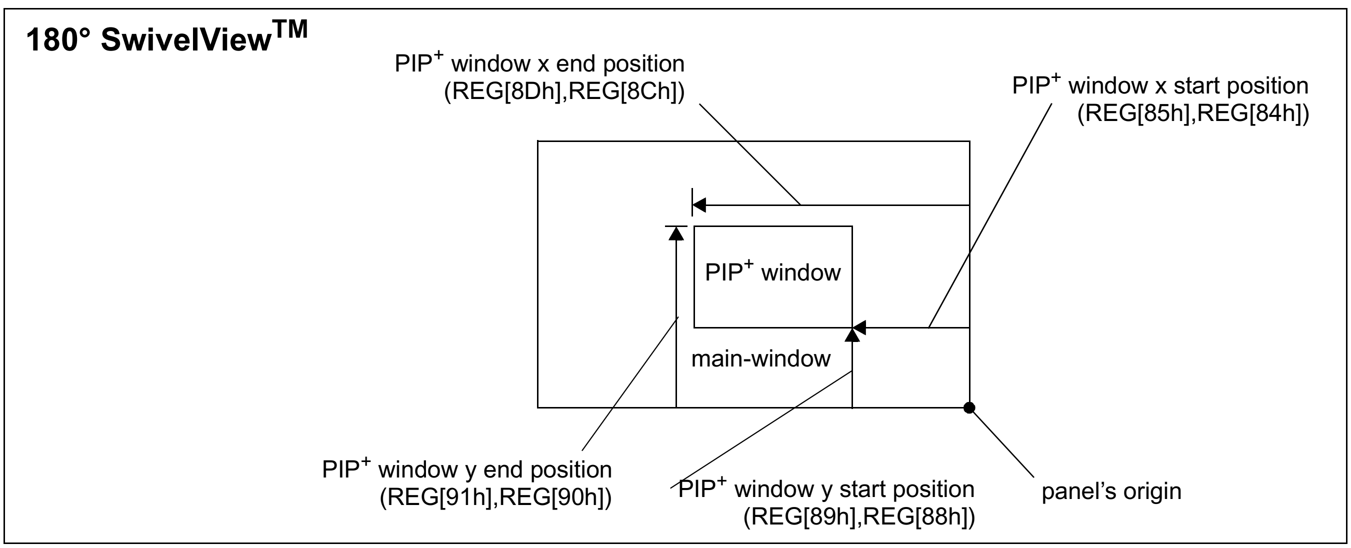


Figure 13-3: Picture-in-Picture Plus with SwivelView 180° enabled

13.2.3 SwivelView 270°

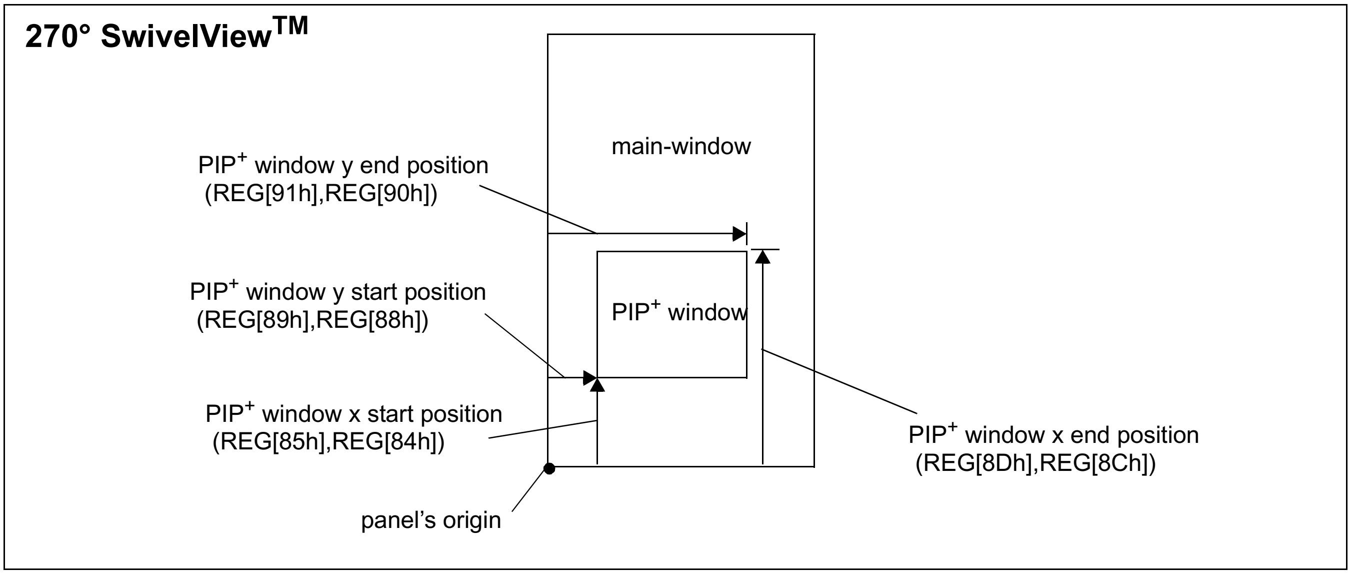


Figure 13-4: Picture-in-Picture Plus with SwivelView 270° enabled

14 Big-Endian Bus Interface

14.1 Byte Swapping Bus Data

The display buffer and register architecture of the S1D13706 is inherently little-endian. If a host bus interface is configured as big-endian (CNF4 = 1 at reset), bus accesses are automatically handled by byte swapping all read/write data to/from the internal display buffer and registers.

Bus data byte swapping translates all byte accesses correctly to the S1D13706 register and display buffer locations. To maintain the correct translation for 16-bit word access, even address bytes must be mapped to the MSB of the 16-bit word, and odd address bytes to the LSB of the 16-bit word. For example:

Byte write 11h to register address 1Eh -> REG[1Eh] <= 11h
Byte write 22h to register address 1Fh -> REG[1Fh] <= 22h

Word write 1122h to register address 1Eh-> REG[1Eh] <= 11h
REG[1Fh] <= 22h

14.1.1 16 Bpp Color Depth

For 16 bpp color depth, the Display Data Byte Swap bit (REG[71h] bit 6) must be set to 1.

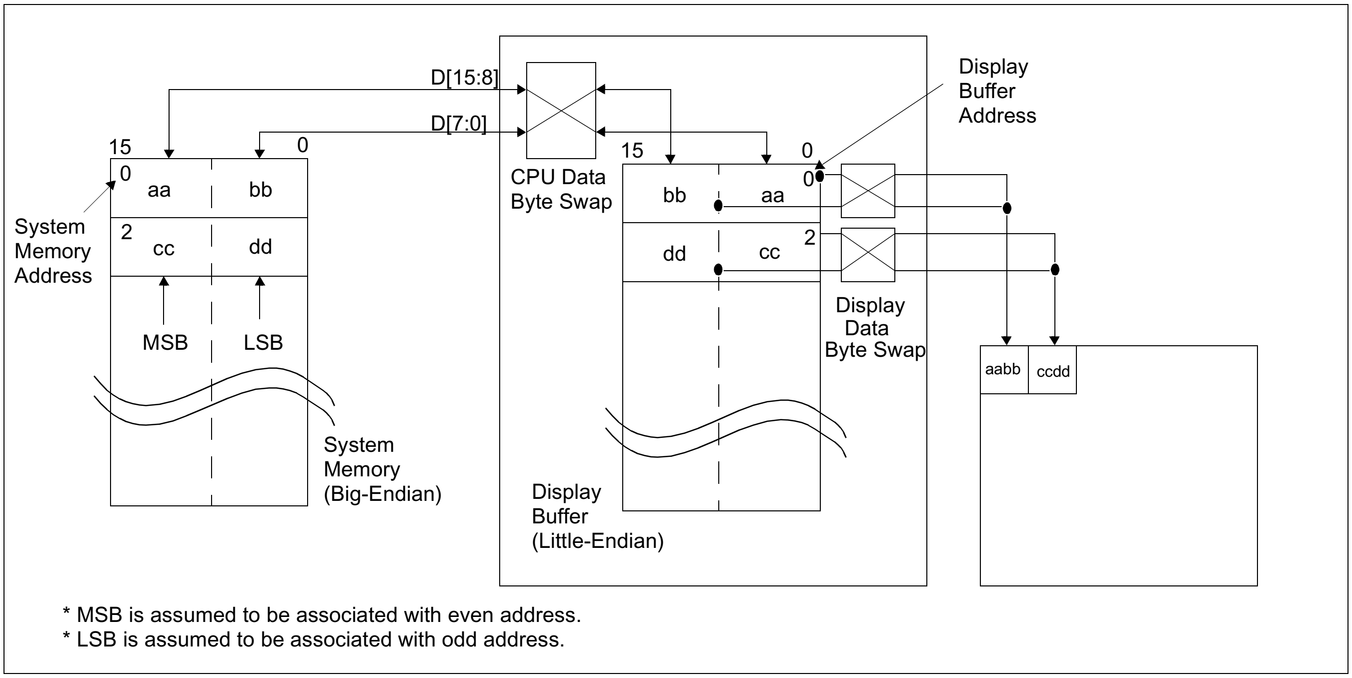


Figure 14-1: Byte-swapping for 16 Bpp

For 16 bpp color depth, the MSB of the 16-bit pixel data is stored at the even system memory address location and the LSB of the 16-bit pixel data is stored at the odd system memory address location. Bus data byte swapping (automatic when the S1D13706 is configured for Big-Endian) causes the 16-bit pixel data to be stored byte-swapped in the S1D13706 display buffer. During display refresh this stored data must be byte-swapped again before it is sent to the display.

14.1.2 1/2/4/8 Bpp Color Depth

For 1/2/4/8 bpp color depth, byte swapping must be performed on the bus data but not the display data.

For 1/2/4/8 bpp color depth, the Display Data Byte Swap bit (REG[71h] bit 6) must be set to 0.

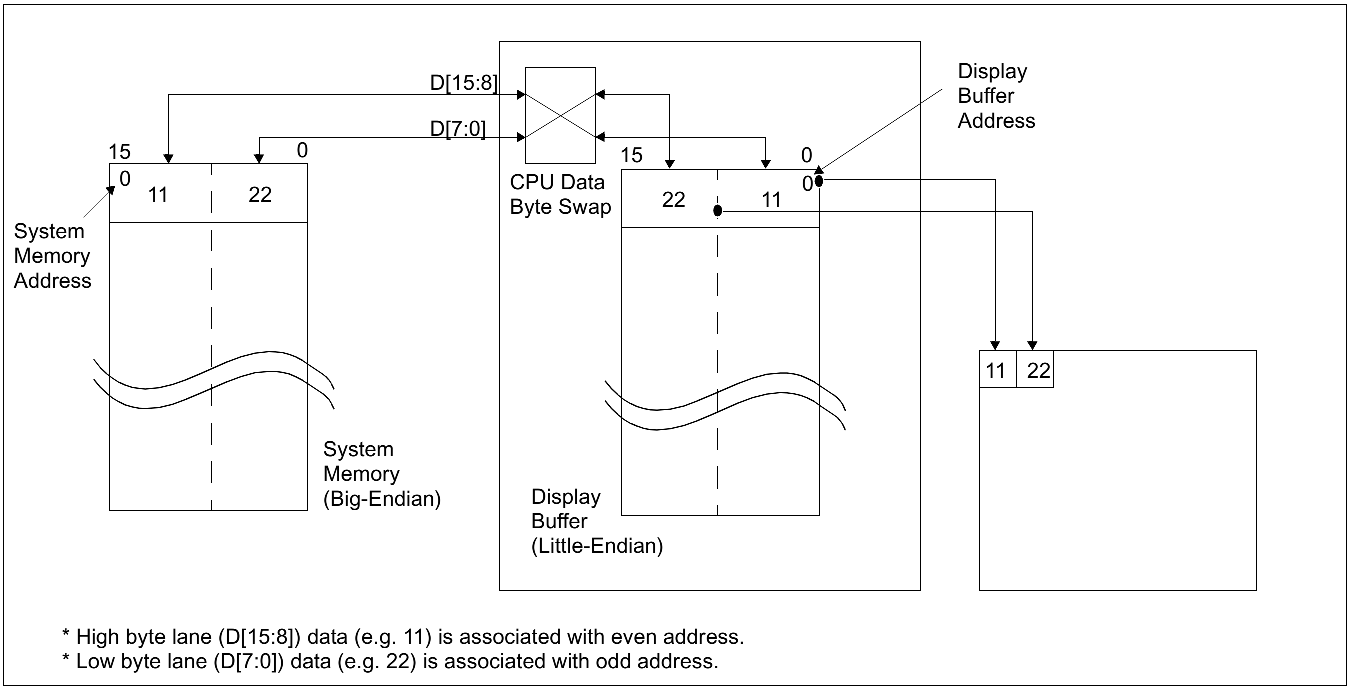


Figure 14-2: Byte-swapping for 1/2/4/8 Bpp

15 Power Save Mode

A software initiated Power Save Mode is incorporated into the S1D13706 to accommodate the need for power reduction in the hand-held devices market. This mode is enabled via the Power Save Mode Enable bit (REG[A0h] bit 0).

Software Power Save Mode saves power by powering down the panel and stopping display refresh accesses to the display buffer.

Table 15-1: Power Save Mode Function Summary

	Software Power Save	**Normal**
IO Access Possible?	Yes	Yes
Memory Writes Possible?	Yes[1]	Yes
Memory Reads Possible?	No[1]	Yes
Look-Up Table Registers Access Possible?	Yes	Yes
Sequence Controller Running?	No	Yes
Display Active?	No	Yes
LCD I/F Outputs	Forced Low	Active
PWMCLK	Stopped	Active
GPIO Pins configured for HR-TFT/D-TFD[2]	Forced Low	Active
GPIO Pins configured as GPIOs Access Possible?[2]	Yes[3]	Yes

Note

[1] When power save mode is enabled, the memory controller is powered down and the status of the memory controller is indicated by the Memory Controller Power Save Status bit (REG[A0h] bit 3). However, memory writes are possible during power save mode because the S1D13706 dynamically enables the memory controller for display buffer writes.
[2] GPIO Pins are configured using the configuration pin CNF3 which is latched on the rising edge of RESET#. For information on CNF3, see Table 4-7: “Summary of Power-On/Reset Options,” on page 28.
[3] GPIOs can be accessed and if configured as outputs can be changed.

After reset, the S1D13706 is always in Power Save Mode. Software must initialize the chip (i.e. programs all registers) and then clear the Power Save Mode Enable bit.

16 Mechanical Data

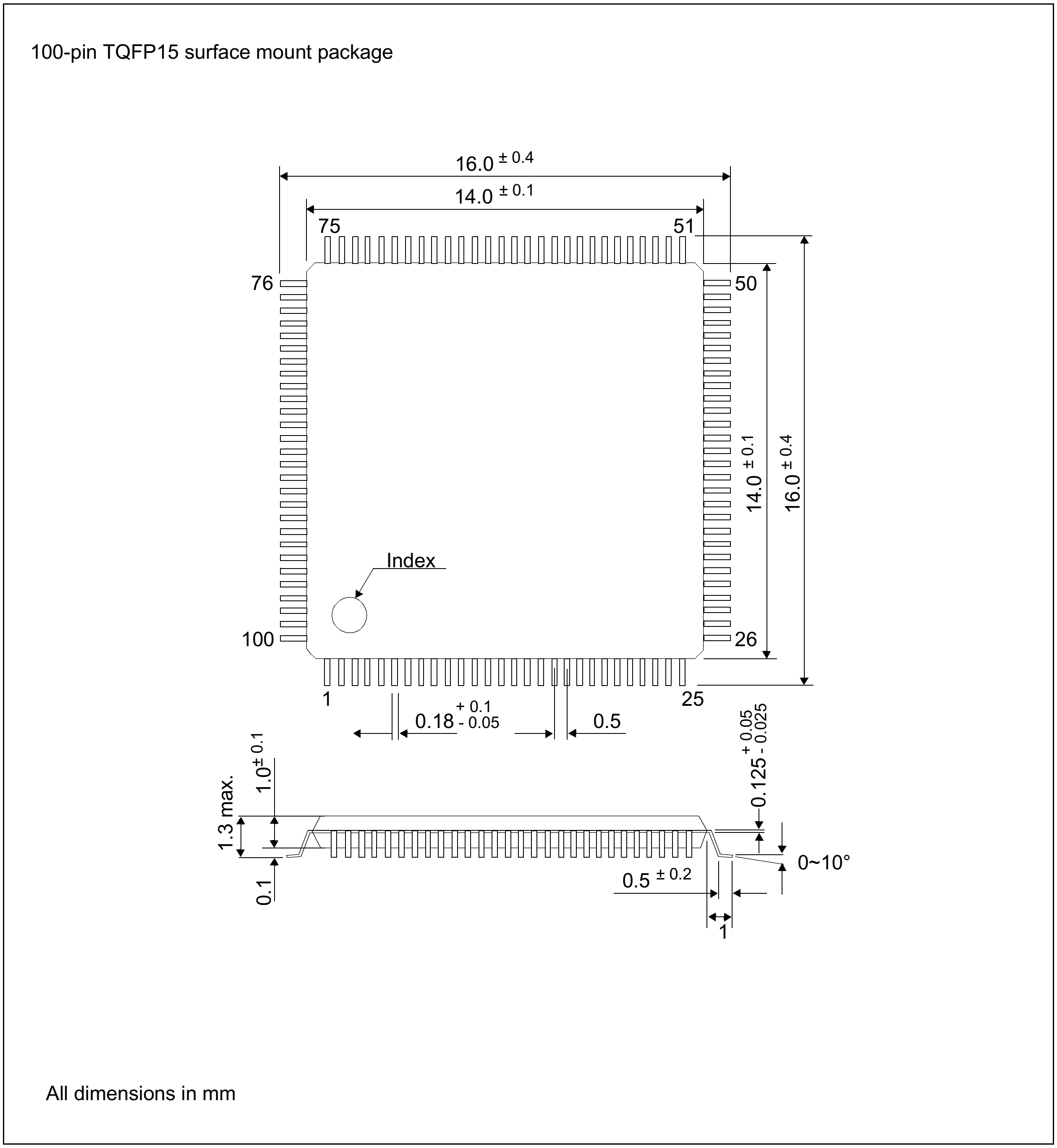


Figure 16-1: Mechanical Data 100pin TQFP15 (S1D13706F00A)

17 References

The following documents contain additional information related to the S1D13706. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- 13706CFG Configuration Utility Users Manual (X31B-B-001-xx)
- 13706SHOW Demonstration Program Users Manual (X31B-B-002-xx)
- 13706PLAY Diagnostic Utility Users Manual (X31B-B-003-xx)
- 13706BMP Demonstration Program Users Manual (X31B-B-004-xx)
- S1D13706 Product Brief (X31B-C-001-xx)
- S1D13706 Windows CE Display Drivers (X31B-E-001-xx)
- Interfacing to the Toshiba TMPR3905/3912 Microprocessor (X31B-G-002-xx)
- S1D13706 Programming Notes And Examples (X31B-G-003-xx)
- S5U13706B00C Rev. 1.0 Evaluation Board User Manual (X31B-G-004-xx)
- Interfacing to the PC Card Bus (X31B-G-005-xx)
- S1D13706 Power Consumption (X31B-G-006-xx)
- Interfacing to the NEC VR4102/VR4111 Microprocessors (X31B-G-007-xx)
- Interfacing to the NEC VR4181 Microprocessor (X31B-G-008-xx)
- Interfacing to the Motorola MPC821 Microprocessor (X31B-G-009-xx)
- Interfacing to the Motorola MCF5307 "Coldfire" Microprocessors (X31B-G-010-xx)
- Connecting to the Sharp HR-TFT Panels (X31B-G-011-xx)
- Connecting to the Epson D-TFD Panels (X31B-G-012-xx)
- Interfacing to the Motorola MC68030 Microprocessor (X31B-G-013-xx)
- Interfacing to the Motorola RedCap2 DSP with Integrated MCU (X31B-G-014-xx)
- Interfacing to 8-Bit Processors (X31B-G-015-xx)
- Interfacing to the Motorola MC68VZ328 Dragonball Microprocessor (X31B-G-016-xx)
- Integrating the CFLGA 104-pin Chip Scale Package (X31B-G-018-xx)
- Interfacing to the Intel StrongARM SA-1110 Microprocessor (X31B-G-019-xx)
- S1D13706 Register Summary (X31B-R-001-xx)

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