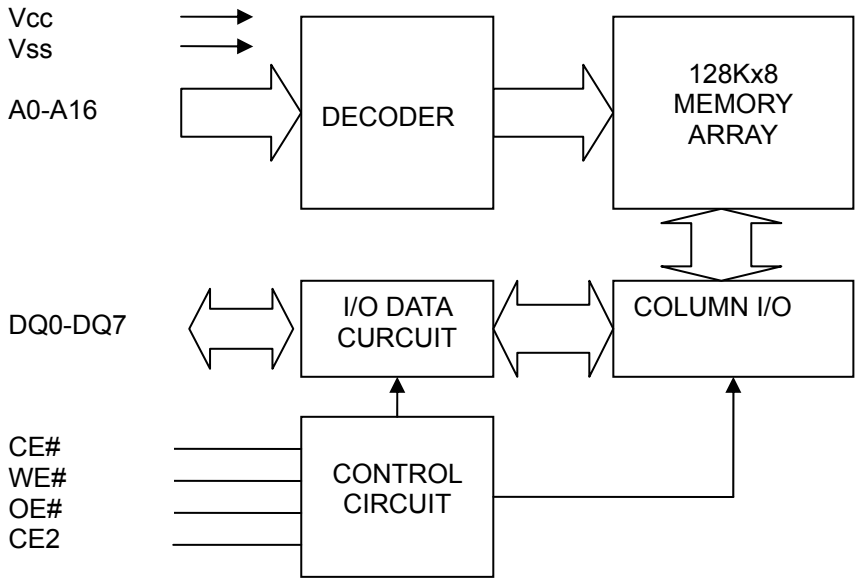
GENERAL DESCRIPTION

The EM6128K800V is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.
The EM6128K800V is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.
The EM6128K800V operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

FEATURES

- Fast access time: 35/55/70ns
- Low power consumption:
  Operating current:
  12/10/7mA (TYP.)
  Standby current: -L/-LL version
  20/1µA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 1.5V (MIN.)
- Package:
  32-pin 450 mil SOP
  32-pin 600 mil P-DIP
  32-pin 8mm x 20mm TSOP-I
  32-pin 8mm x 13.4mm STSOP
  36-ball 6mm x 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM

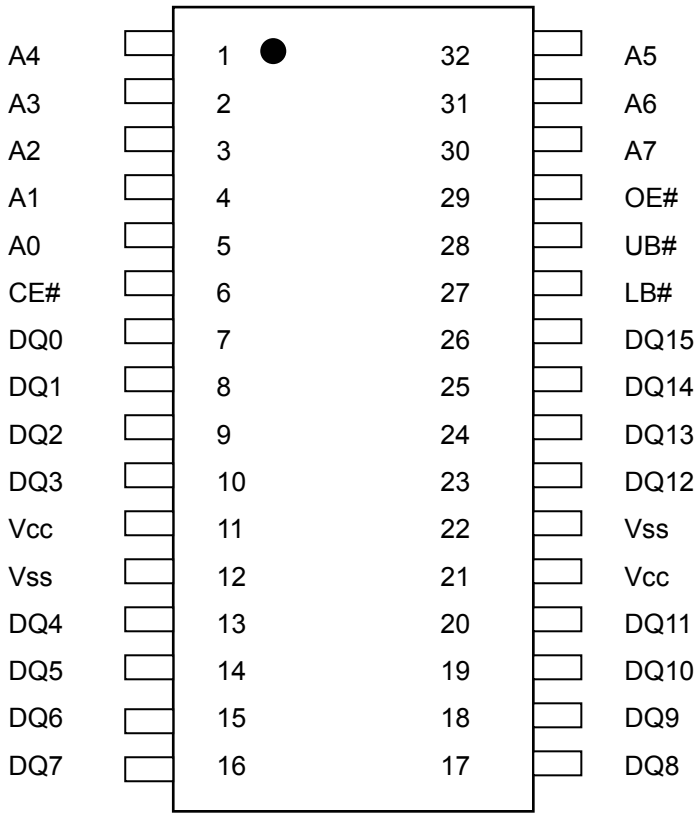


PIN DESCRIPTION

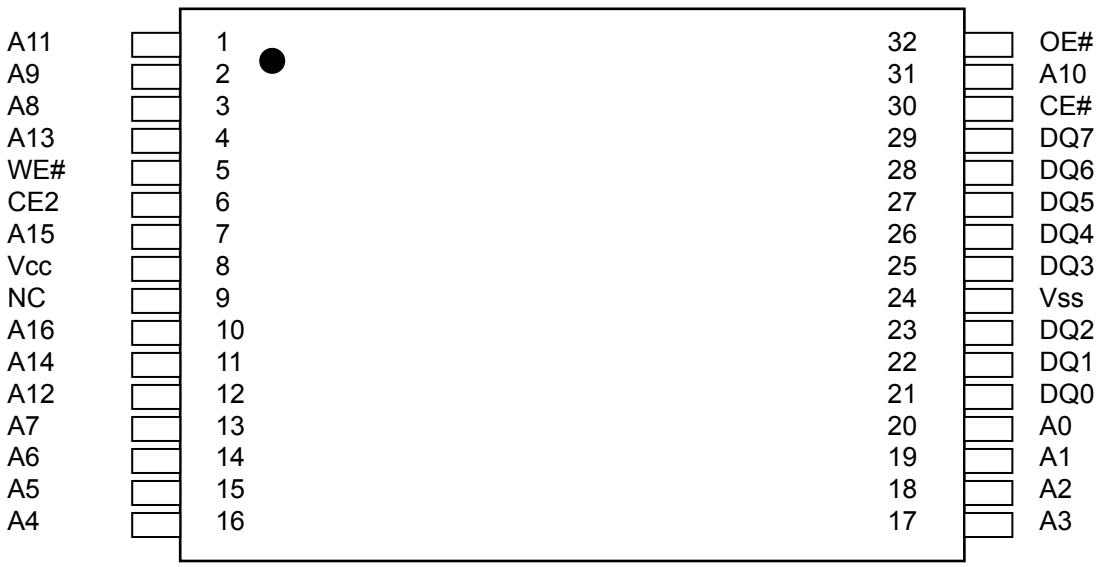
SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

SOP/P-DIP



TSOP-I/STSOP



TFBGA

A	**A0**	**A1**	**CE2**	**A3**	**A6**	**A8**
B	**DQ4**	**A2**	**WE#**	**A4**	**A7**	**DQ0**
C	**DQ5**		**NC**	**A5**		**DQ1**
D	**Vss**					**Vcc**
E	**Vcc**					**Vss**
F	**DQ6**		**NC**	**NC**		**DQ2**
G	**DQ7**	**OE#**	**CE#**	**A16**	**A15**	**DQ3**
H	**A9**	**A10**	**A11**	**A12**	**A13**	**A14**
	1	**2**	**3**	**4**	**5**	**6**

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB},I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC},I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = VIH, L = VIL, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *5	MAX.	UNIT
Supply Voltage	Vcc			2.7	3.0	3.6	V
Input High Voltage	V_{IH}*1			2.0	-	Vcc+ 0.3	V
Input Low Voltage	V_{IL}*2			-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		-1	-	+1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		-1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} , $I_{I/O}$ = 0mA	-35	-	12	35	mA
			-55	-	10	30	mA
			-70	-	7	25	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and $I_{I/O}$ = 0mA other pins at 0.2V or V_{CC}-0.2V		-	1	5	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH}		-	0.3	0.5	mA
	I_{SB1}	CE# V $\geqq$ V_{CC} - 0.2V	-L	-	20	80	µA
			-LL		1	10	µA

Notes:
1. VIH(max) = VCC + 3.0V for pulse width less than 10ns.
2. VIL(min) = VSS - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10µA for special request
5. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at VCC = VCC(TYP.) and TA = 25°C

CAPACITANCE (T_A = 25°C , f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

READ CYCLE

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

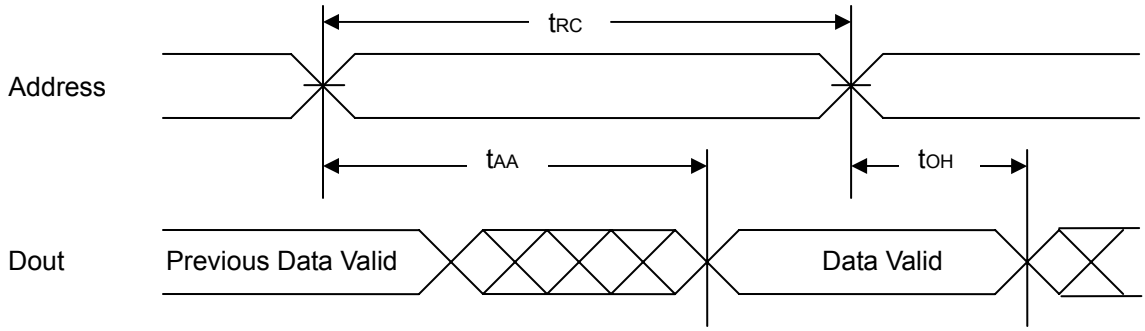
WRITE CYCLE

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	45	-	55	-	ns
Write Recovery Time	t_{wr}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

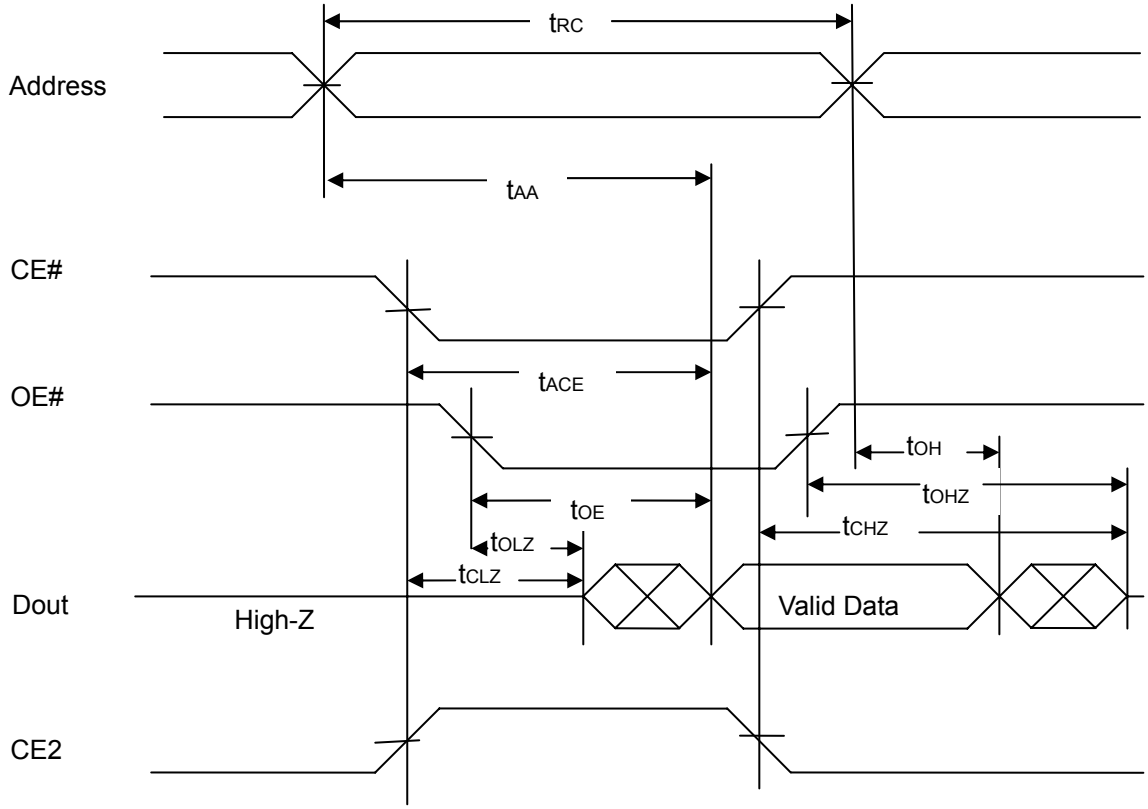
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

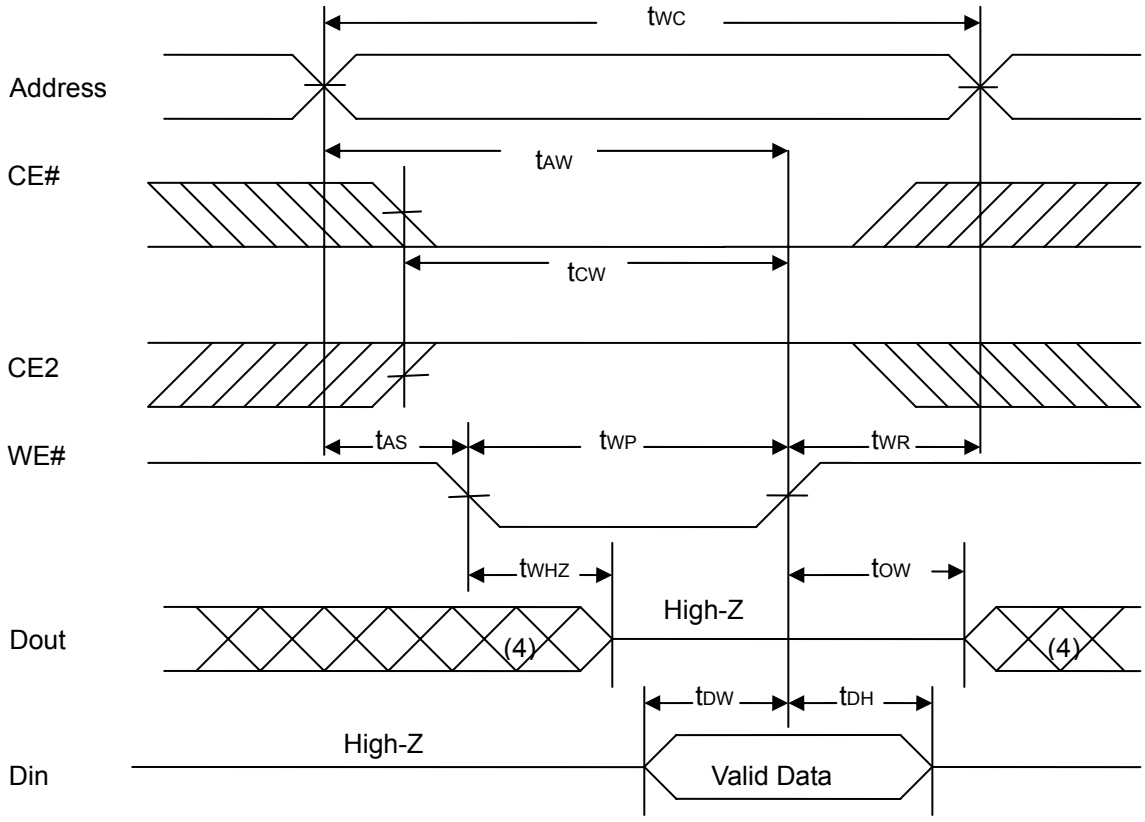


READ CYCLE 2 (CE#, CE2 and OE# controlled) (1,3,4,5)

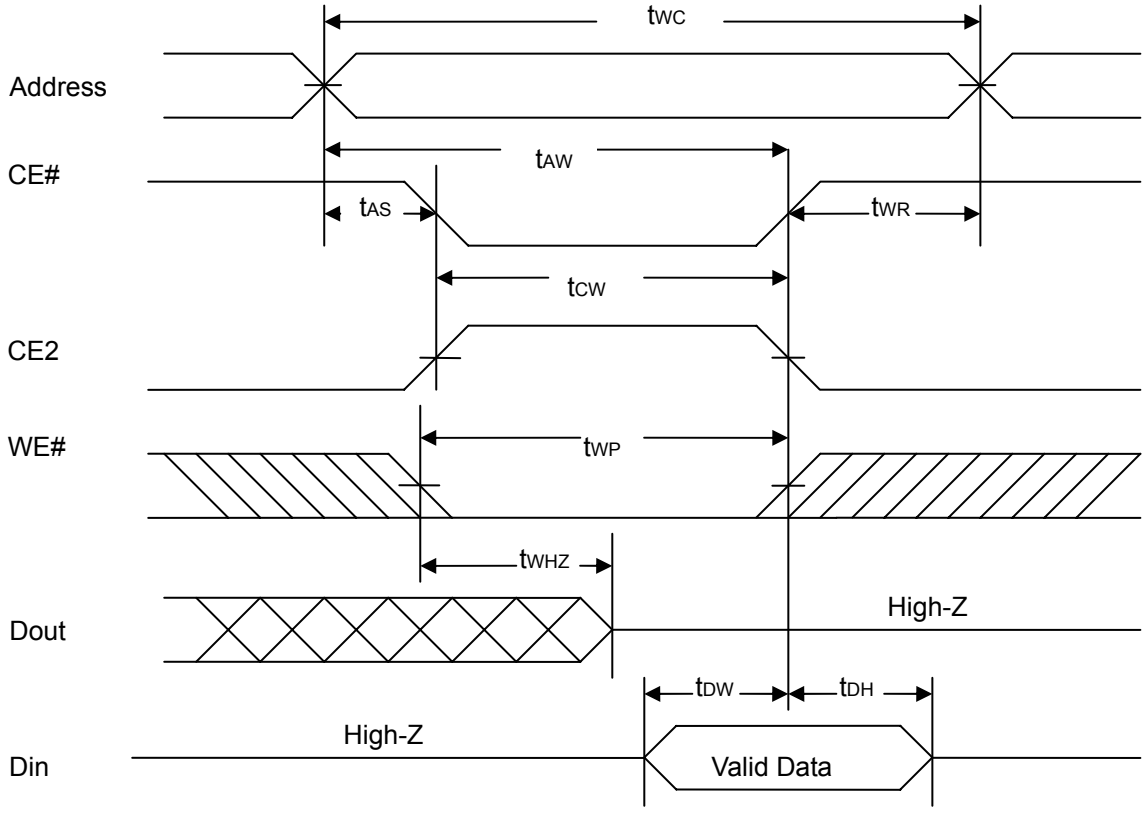


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, CE2 = high.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4.tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, tCHZ is less than tCLZ , tOHZ is less than tOLZ.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.

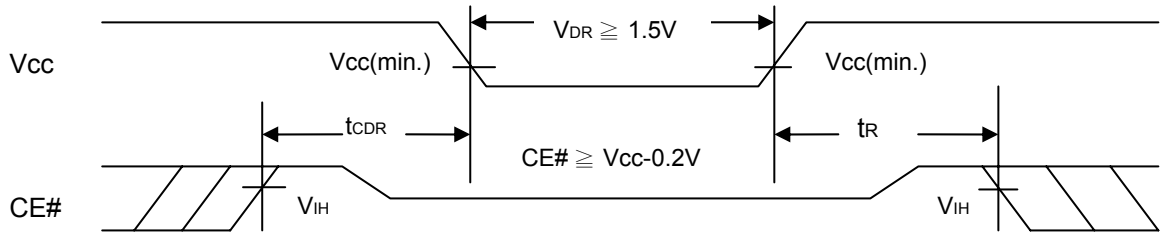
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# V ≧ V_{CC} - 0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# V ≧ V_{CC} - 0.2V	-L	-	1	50	µA
			-LL	-	0.5	5	µA
			-LLE -LLI		0.5	10	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

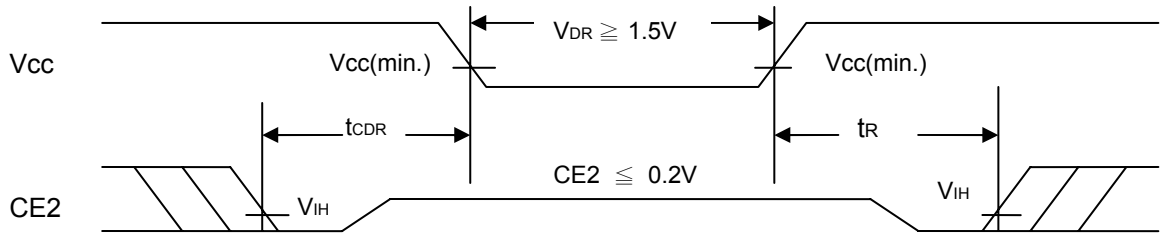
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



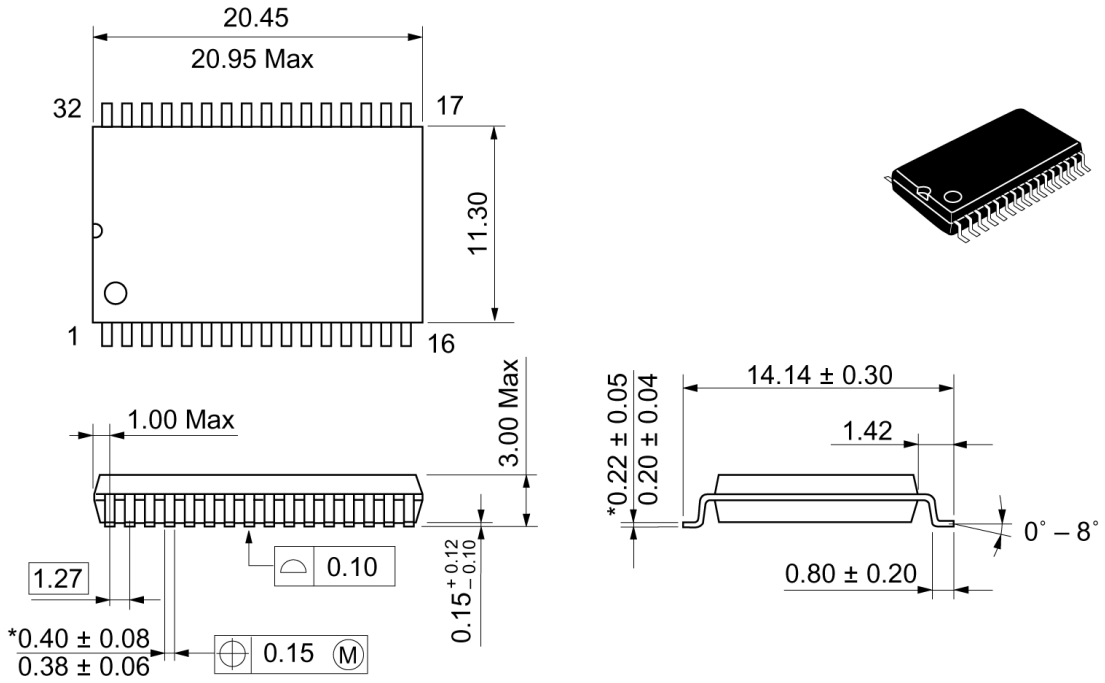
Low Vcc Data Retention Waveform (2) (CE2 controlled)



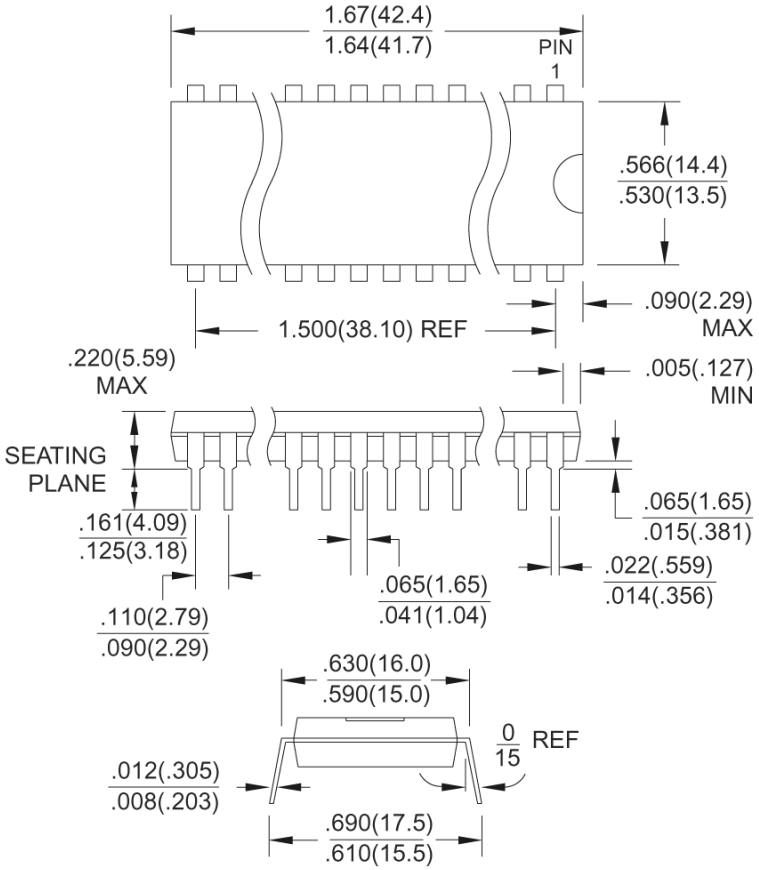
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension

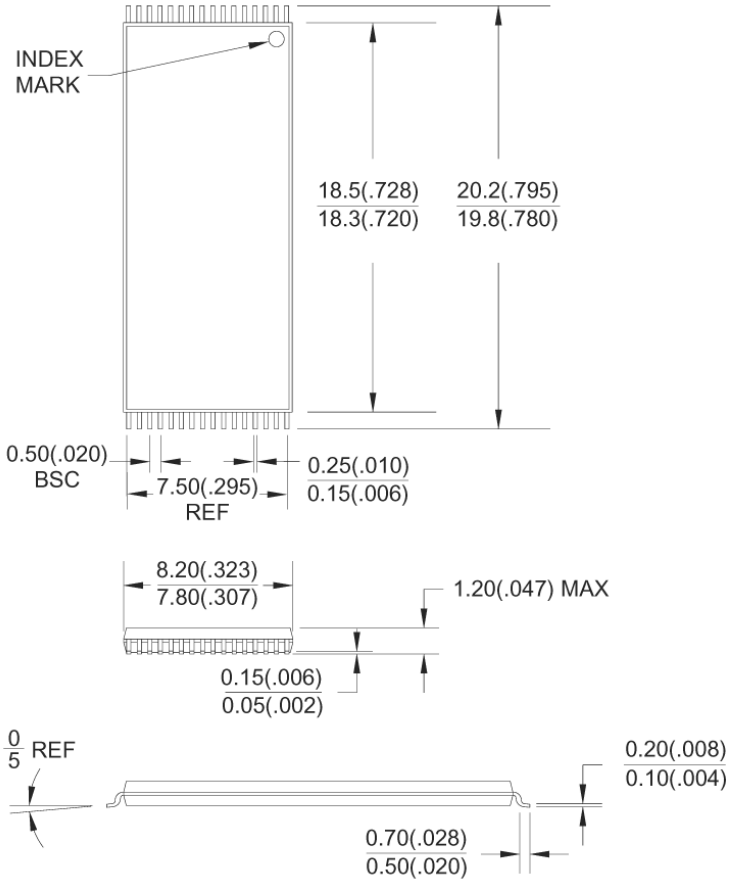
Unit: mm



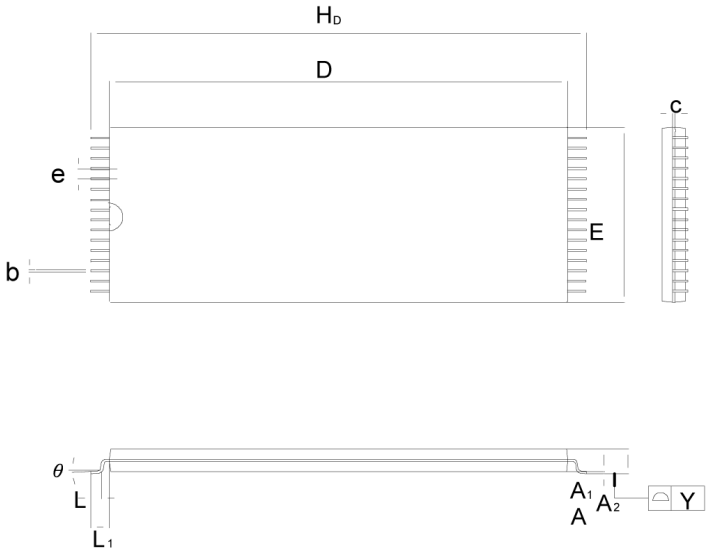
32 pin 600 mil P-DIP Package Outline Dimension



32 pin 8mm x 20mm TSOP-I Package Outline Dimension

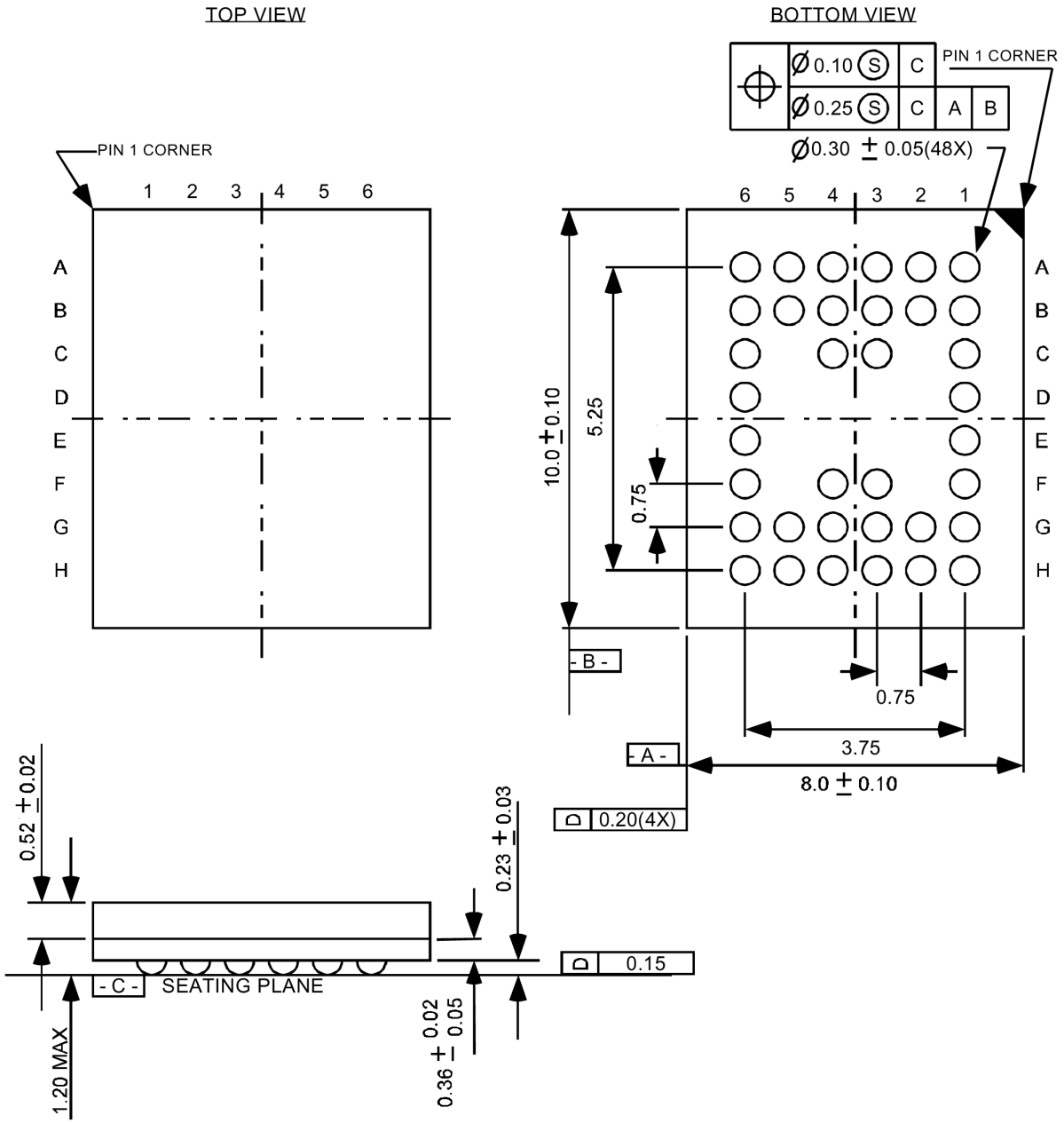


32 pin 8mm x 13.4mm STSOP Package Outline Dimension

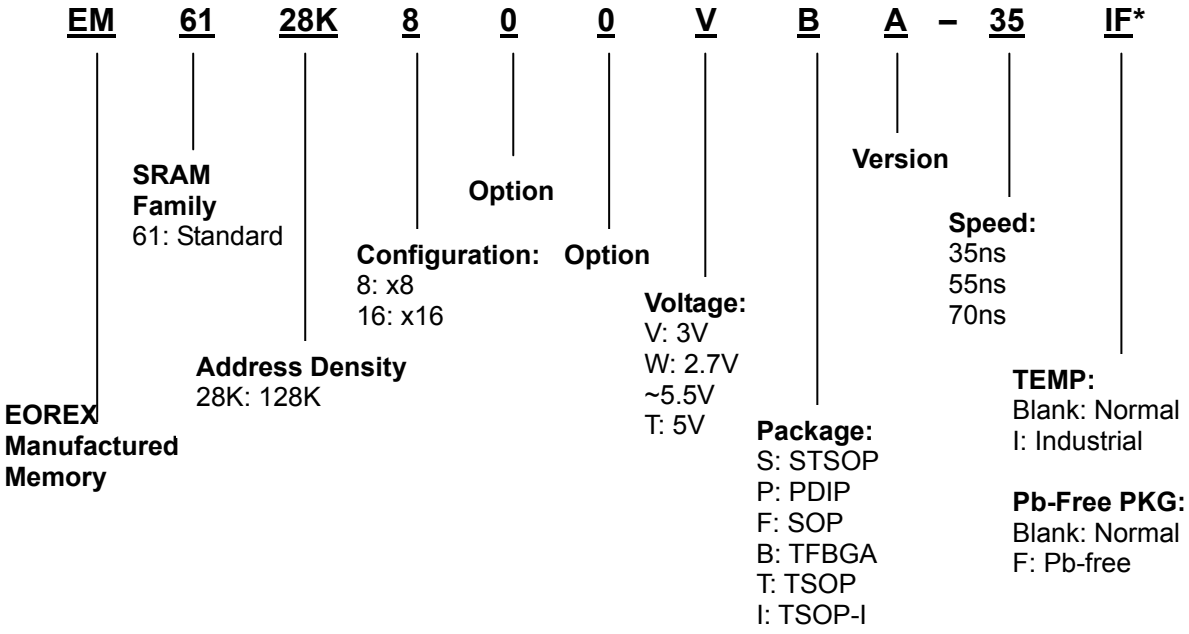


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

36-ball 6mm × 8mm TFBGA Package Outline Dimension



Product ID Information



* Product ID example

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