SECTION 20
ELECTRICAL CHARACTERISTICS

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC860.

NOTE

The MPC860 electrical specifications are preliminary and many specs are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

20.1 MAXIMUM RATINGS (GND = 0V)

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	VDDH	-0.3 to 4.0	V
	VDD	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input Voltage	VIN	GND-0.3 to 5.8	V
Junction Temperature	T_j	90@25 MHz or TBD @ 40 MHz	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

NOTE:
1. Functional operating conditions are given in **Section 20.3 Power Considerations**. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. **CAUTION**: All "5 Volt Friendly" Input voltages cannot be more than 2.5 V greater than supply voltage, this restriction applies also on "power-on" as well as on normal operation.
3. "5 Volt Friendly" inputs are inputs that tolerate 5 volts.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

20.2 THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Thermal Resistance for BGA	θ_{JA}	47[1]	°C/W
	θ_{JA}	30[2]	°C/W
	θ_{JA}	15[3]	°C/W

NOTE:
1. Assumes natural convection and a single layer board (no thermal vias).
2. Assumes natural convection, a mult ilayer board with thermal vias[4], 1 watt MPC860 dissipation, and a board temperature rise of 20°C above ambient.
3. Assumes natural convection, a multilayer board with thermal vias[4],1 watt MPC860 dissipation, and a board temperature rise of 10°C above ambient.
4. For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, *Plastic Ball Grid Array Application Note* available from your local Motorola sales office.

$$T_J = T_A + (P_D \bullet \theta_{JA})$$
$$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$$

where:

$P_{I/O}$ is the power dissipation on pins.

20.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from

$$T_J = T_A + (P_D \bullet q_{JA}) \qquad (1)$$

where

T_A = Ambient Temperature, ∞C

q_{JA} = Package Thermal Resistance, Junction to Ambient, ∞C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = I_{DD} x V_{DD}, Watts—Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \prod (T_J + 273\infty C) \qquad (2)$$

Solving equations (1) and (2) for K gives

$$K = P_D \bullet (T_A + 273\infty C) + q_{JA} \bullet P_D^{\,2} \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

20.3.1 Layout Practices

Each V_{CC} pin on the MPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs

during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

20.4 DC ELECTRICAL CHARACTERISTICS

(T_A = 0 °C to 70 °C; V_{CC} = 3.0 - 3.6 Vdc ±5%; GND = 0 Vdc; unless otherwise noted)

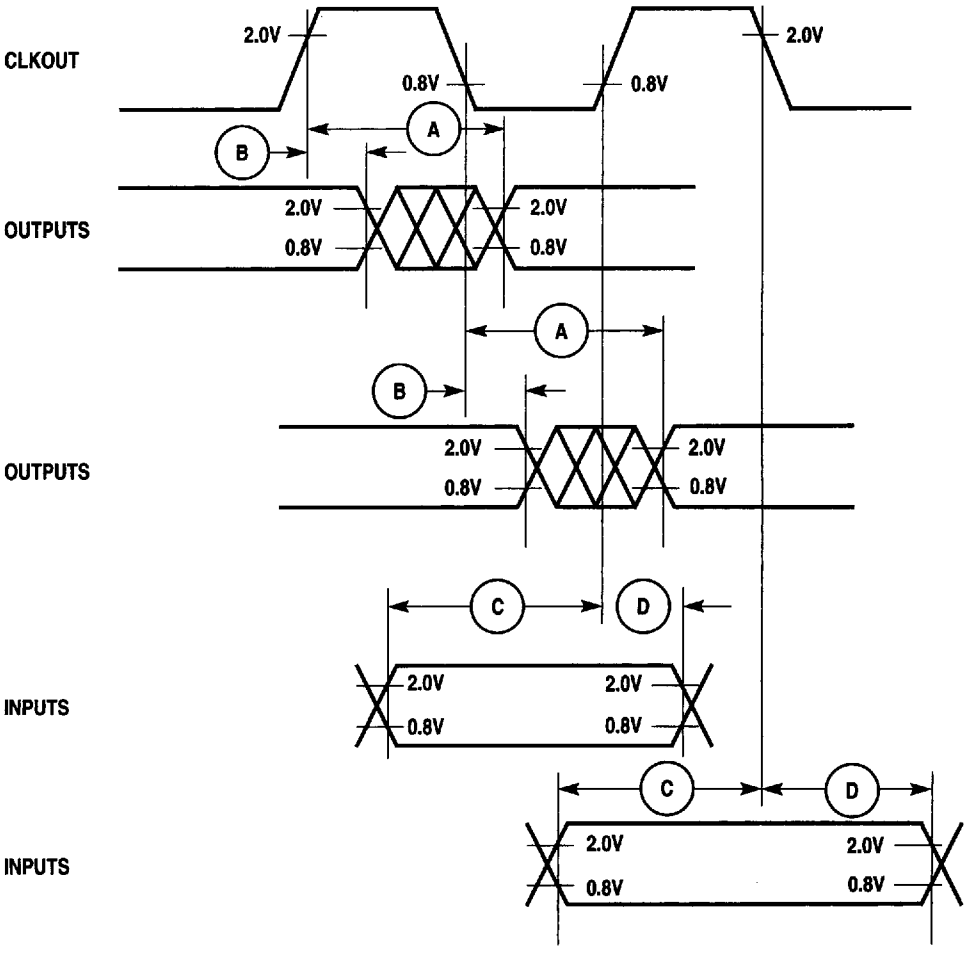
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage, all inputs except EXTAL and CLK4IN *	V_{IH}	2.0	5.5	V
Input Low Voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	V_{IHC}	0.7*(V_{CC})	V_{CC}+0.3	V
Input Leakage Current, V_{IN} = 5.5 V	I_{IN}	—	TBD	mA
Hi-Z (Off State) Leakage Current, V_{IN} = TBD V	I_{OZ}	—	TBD	mA
Signal Low Input Current, V_{IL} = 0.8 V	I_L	TBD	TBD	mA
Signal High Input Current, V_{IH} = 2.0 V	I_H	TBD	TBD	mA
Output High Voltage, I_{OH} = –20 mA, V_{DDH} = 3.0 V Except XTAL, XFC, and Open Drain Pins	V_{OH}	2.4	—	V
Output Low Voltage, I_{OL} = 2.0 mA CLKOUT I_{OL} = 3.2 mA A(0:31), TSIZ0 / $\overline{REG}$, TSIZ1, D(0:31), DP(0:3) / $\overline{IRQ}$(3:6), RD / $\overline{WR}$, $\overline{BURST}$, RSV / $\overline{IRQ2}$, IP_B(0:1) / IWP(0:1) / VFLS(0:1), IP_B2 / $\overline{IOIS16\_B}$ / AT2, IP_B3 / IWP2 / VF2, IP_B4 / LWP0 / VF0, IP_B5 / LWP1 / VF1, IP_B6 / DSDI / AT0, IP_B7 / PTR / AT3, RXD1 / PA15, RXD2 / PA13, L1TXDB / PA11, L1RXDB / PA10, L1TXDA / PA9, L1RXDA / PA8, TIN1 / L1RCLKA / BRGO1 / CLK1 / PA7, BRGCLK1 / $\overline{TOUT1}$ / CLK2 / PA6, TIN2 / L1TCLKA / BRGO2 / CLK3 / PA5, $\overline{TOUT2}$ / CLK4 / PA4, TIN3 / BRGO3 / CLK5 / PA3, BRGCLK2 / L1RCLKB / $\overline{TOUT3}$ / CLK6 / PA2, TIN4 / BRGO4 / CLK7 / PA1, L1TCLKB / $\overline{TOUT4}$ / CLK8 / PA0, REJECT1 / $\overline{SPISEL}$ / PB31, SPICLK / PB30, SPIMOSI / PB29,	V_{OL}	—	0.5	V

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Output Low Voltage (continued),	V_{OL}	—	0.5	V
I_{OL} = 3.2 mA BRGO4 / SPIMISO / PB28, BRGO1 / I2CSDA / PB27, BRGO2 / I2CSCL / PB26, SMTXD1 / PB25, SMRXD1 / PB24, $\overline{\text{SMSYN1}}$ / SDACK1 / PB23, $\overline{\text{SMSYN2}}$ / SDACK2 / PB22, SMTXD2 / L1CLKOB / PB21, SMRXD2 / L1CLKOA / PB20, L1ST1 / $\overline{\text{RTS1}}$ / PB19, L1ST2 / $\overline{\text{RTS2}}$ / PB18, L1ST3 / L1RQB / PB17, L1ST4 / L1RQA / PB16, BRGO3 / PB15, $\overline{\text{RSTRT1}}$ / PB14, L1ST1 / $\overline{\text{RTS1}}$ / DREQ0 / PC15, L1ST2 / $\overline{\text{RTS2}}$ / DREQ1 / PC14, L1ST3 / L1RQB / PC13, L1ST4 / L1RQA / PC12, $\overline{\text{CTS1}}$ / PC11, $\overline{\text{TGATE1}}$ / CD1 / PC10, $\overline{\text{CTS2}}$ / PC9, $\overline{\text{TGATE2}}$ / CD2 / PC8, SDACK2 / L1TSYNCB / PC7, L1RSYNCB / PC6, SDACK1 / L1TSYNCA / PC5, L1RSYNCA / PC4, LD8, RXD3, TXD3, RTS3, CD3, RXD4, TXD4, RTS4, CD4,				
I_{OL} = 5.3 mA $\overline{\text{BDIP}}$ / $\overline{\text{GPL_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ / $\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:5), $\overline{\text{CS}}$(6) / $\overline{\text{CE}}$(1)_B, $\overline{\text{CS}}$(7) / $\overline{\text{CE}}$(2)_B, $\overline{\text{WE0}}$ / $\overline{\text{BS_B0}}$ / $\overline{\text{IORD}}$, $\overline{\text{WE1}}$ / $\overline{\text{BS_B1}}$ / $\overline{\text{IOWR}}$, $\overline{\text{WE2}}$ / $\overline{\text{BS_B2}}$ / $\overline{\text{PCOE}}$, $\overline{\text{WE3}}$ / $\overline{\text{BS_B3}}$ / $\overline{\text{PCWE}}$, $\overline{\text{BS_A}}$(0:3), $\overline{\text{GPL_A0}}$ / $\overline{\text{GPL_B0}}$, $\overline{\text{OE}}$ / $\overline{\text{GPL_A1}}$ / $\overline{\text{GPL_B1}}$, $\overline{\text{GPL_A}}$(2:3) / $\overline{\text{GPL_B}}$(2:3) / $\overline{\text{CS}}$(2:3), $\overline{\text{UPWAITA}}$ / $\overline{\text{GPL_A4}}$, $\overline{\text{UPWAITB}}$ / $\overline{\text{GPL_B4}}$, $\overline{\text{GPL_A5}}$, ALE_A, $\overline{\text{CE1_A}}$, $\overline{\text{CE2_A}}$, ALE_B / DSCK / AT1, OP(0:1), OP2 / MODCK0 / $\overline{\text{STS}}$, OP3 / MODCK1 / DSDO				
I_{OL} = 7.0 mA TXD1 / PA14, TXD2 / PA12				
I_{OL} = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$				

NOTE: 1. Input pin voltage specifications are V_{CC} = +4 V or 5.8 V, whichever is less.

2. AC timings are based on a 50 pf load.

20.5 MPC860 AC ELECTRICAL SPECIFICATIONS



A = MAXIMUM OUTPUT DELAY SPECIFICATION

B = MINIMUM OUTPUT HOLD TIME

C = MINIMUM INPUT SETUP TIME SPECIFICATION

D = MINIMUM INPUT HOLD TIME SPECIFICATION

Figure 20-1. AC Electrical Specifications Control Timing Diagram

Table 20-1. Bus Operation Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
B1	CLKOUT Period	TC	—	—	—	—	ns
B2	Clock Pulse Width Low		—	—	—	—	ns
B3	Clock Pulse Width High		—	—	—	—	ns
B4	CLKOUT Rise Time		—	—	—	—	ns
B5	CLKOUT Fall Time		—	—	—	—	ns
B6	Circuit Parameter TCC		9	—	6	—	—
B7	CLKOUT to A(0:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) Invalid	0.25TC + 1	10	—	5	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR Invalid	0.25TC + 1	10	—	5	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), $\overline{STS}$ Invalid [1]	0.25TC + 1	10	—	5	—	ns
B8	CLKOUT to A(0:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) Valid	0.25TC + TCC	10	19	—	13	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR Valid	0.25TC + TCC	10	19	—	13	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid. [1]	0.25TC + TCC	10	19	—	13	ns
B9	CLKOUT to A(0:31), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z	0.25TC + TCC	10	19	5	13	ns
B10			—	—	—	—	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ Assertion	0.25TC + TCC	10	19	5	13	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Assertion (When Driven by the Memory Controller or PCMCIA Interface)		—	11	—	10	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ Negation	0.25TC + TCC	10	19	5	13	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ Negation (When Driven by the Memory Controller or PCMCIA Interface)		—	11	—	11	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z	0.25TC +14	10	24	5	21	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (When Driven by the Memory Controller or PCMCIA Interface)		—	15	—	15	ns
B14	CLKOUT to $\overline{TEA}$ Assertion		—	11	—	11	ns
B15	CLKOUT to $\overline{TEA}$ High-Z		—	15	—	15	ns

Table 20-1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
B16	$\overline{TA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ Valid to CLKOUT (Setup Time) [2 3]		9	—	7	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ Valid to CLKOUT (Setup Time)		11	—	10	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ Valid (Hold Time) [2]		2	—	2	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ Valid (Hold Time)		2	—	2	—	ns
B18	D(0:31), DP(0:3) Valid to CLKOUT Rising Edge (Setup Time) [4]		6	—	6	—	ns
B19	CLKOUT Rising Edge to D(0:31), DP(0:3) Valid (Hold Time) [4]		2	—	1	—	ns
B20	D(0:31), DP(0:3) Valid to CLKOUT Falling Edge (Setup Time) [5]		4	—	4	—	ns
B21	CLKOUT Falling Edge to D(0:31), DP(0:3) Valid (Hold Time) [5]		2	—	2	—	ns
B22	CLKOUT Rising Edge to $\overline{CS}$ Asserted -GPCM- ACS = 00	0.25TC+TCC+1	10	20	5	13	ns
B22a	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0	TCC + 1	—	10	—	8	ns
B22b	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0	0.25TC+TCC+1	10	20	5	13	ns
B23	CLKOUT Rising Edge to $\overline{CS}$ Negated -GPCM- Read Access	TCC + 1	3	10	2	8	ns
B24	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0		8	—	3	—	ns
B24a	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0		18	—	8	—	ns
B25	CLKOUT Rising Edge to $\overline{OE}$, $\overline{WE}$(0:3) Asserted		—	11	—	9	ns
B26	CLKOUT Rising Edge to $\overline{OE}$ Negated		3	11	2	9	ns
B27	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 1		48	—	23	—	ns
B27a	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 1		58	—	28	—	ns
B28	CLKOUT Rising Edge to $\overline{WE}$(0:3) Negated -GPCM- Write Access, CSNT = '0'		—	11	—	9	ns

Table 20-1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
B28a	CLKOUT Falling Edge to $\overline{WE}$(0:3) Negated -GPCM- Write Access, TRLX = '0', CSNT = '1'	0.25TC + TCC + 1	10	20	5	13	ns
B28b	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10', or ACS='11'	0.25TC + TCC + 1	—	20	—	13	ns
B29	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, CSNT = '0'		8	—	3	—	ns
B29a	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, TRLX = '0', CSNT = '1'		18	—	8	—	ns
B29b	$\overline{CS}$ Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, ACS = '00', TRLX = '0', and CSNT = '0'		8	—	3	—	ns
B29c	$\overline{CS}$ Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10', or ACS='11'		18	—	8	—	ns
B29d	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, TRLX = '1', CSNT = '1'		58	—	28	—	ns
B29e	$\overline{CS}$ Negated to D(0:31), DP(0:3) High-Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10', or ACS='11'		58	—	28	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) Negated to A(0:31) Invalid -GPCM- Write Access [6]		8	—	3	—	—
B30a	$\overline{WE}$(0:3) Negated to A(0:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1' $\overline{CS}$ negated to A(0:31) Invalid -GPCM- Write Access, TRLX='0', CSNT = '1', ACS = '10', ACS = ='11'		18	—	8	—	ns
B30b	$\overline{WE}$(0:3) Negated to A(0:31) Invalid -GPCM- Write Access, TRLX='1', CSNT = '1' $\overline{CS}$ Negated to A(0:31) Invalid -GPCM- Write Access, TRLX='1', CSNT = '1', ACS = '10', ACS = ='11'		58	—	28	—	ns
B31	CLKOUT Falling Edge to $\overline{CS}$ Valid - As Requested by Control Bit CST4 in the Corresponding Word in the UPM	TCC + 1	1.5	10	1.5	8	ns
B31a	CLKOUT Falling Edge to $\overline{CS}$ Valid - As Requested by Control Bit CST1 in the Corresponding Word in the UPM	0.25TC + TCC + 1	10	20	5	13	ns
B31b	CLKOUT Rising Edge to $\overline{CS}$ Valid - As Requested by Control Bit CST2 in the Corresponding Word in the UPM	TCC + 1	1.5	10	1.5	8	ns

Table 20-1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
B31c	CLKOUT Rising Edge to $\overline{CS}$ Valid - As Requested by Control Bit CST3 in the Corresponding Word in the UPM	0.25TC + TCC + 1	10	20	5	13	ns
B32	CLKOUT Falling Edge to $\overline{BS}$ Valid - As Requested by Control Bit BST4 in the Corresponding Word in the UPM	TCC + 1	1.5	10	1.5	8	ns
B32a	CLKOUT Falling Edge to $\overline{BS}$ Valid - As Requested by Control Bit BST1 in the Corresponding Word in the UPM	0.25TC + TCC + 1	10	20	5	13	ns
B32b	CLKOUT Rising Edge to $\overline{BS}$ Valid - As Requested by Control Bit BST2 in the Corresponding Word in the UPM	TCC + 1	1.5	10	1.5	8	ns
B32c	CLKOUT Rising Edge to $\overline{BS}$ Valid - As Requested by Control Bit BST3 in the Corresponding Word in the UPM	0.25TC + TCC + 1	10	20	5	13	ns
B33	CLKOUT Falling Edge to $\overline{GPL}$ Valid - As Requested by Control Bit GxT4 in the Corresponding Word in the UPM	TCC + 1	—	10	—	8	ns
B33a	CLKOUT Rising Edge to $\overline{GPL}$ Valid - As Requested by Control Bit GxT3 in the Corresponding Word in the UPM	0.25TC + TCC + 1	10	20	5	13	ns
B34	A(0:31) to $\overline{CS}$ Valid - As Requested by Control Bit $\overline{CST4}$ in the Corresponding Word in the UPM		8	—	3	—	ns
B34a	A(0:31) to $\overline{CS}$ Valid - As Requested by Control Bit $\overline{CST1}$ in the Corresponding Word in the UPM		18	—	8	—	ns
B34b	A(0:31) to $\overline{CS}$ Valid - As Requested by Control Bit $\overline{CST2}$ in the Corresponding Word in the UPM		28	—	13	—	ns
B35	A(0:31) to $\overline{BS}$ Valid - As Requested by Control Bit BST4 in the Corresponding Word in the UPM		8	—	3	—	ns
B35a	A(0:31) to $\overline{BS}$ Valid - As Requested by Control Bit BST1 in the Corresponding Word in the UPM		18	—	8	—	ns
B35b	A(0:31) to $\overline{BS}$ Valid - As Requested by Control Bit BST2 in the Corresponding Word in the UPM		28	—	13	—	ns
B36	A(0:31) to $\overline{GPL}$ Valid - As Requested by Control Bit GxT4 in the Corresponding Word in the UPM		8	—	3	—	ns
B37	UPWAIT Valid to CLKOUT Falling Edge [7]		6	—	—	—	ns
B38	CLKOUT Falling Edge to UPWAIT Valid [7]		1	—	—	—	ns
B39	$\overline{AS}$ Valid to CLKOUT Rising Edge [8]		9	—	7	—	ns

Table 20-1. Bus Operation Timing (Continued)

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, Valid to CLKOUT Rising Edge		9	—	7	—	ns
B41	$\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)		9	—	7	—	ns
B42	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time)		2	—	2	—	ns
B43	$\overline{AS}$ Negation to Memory Controller Signals Negation		—	TBD	—	TBD	ns

NOTES:
1. The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.
2. The setup times required for $\overline{TA}$, $\overline{TEA}$ and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drive them).
3. The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.
4. The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.
5. The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only under control of the UPM in the memory controller.
6. The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE}$(0:3) when CSNT = '0'.
7. The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20-15.
8. The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified to allow the behavior specified in Figure 20-18.

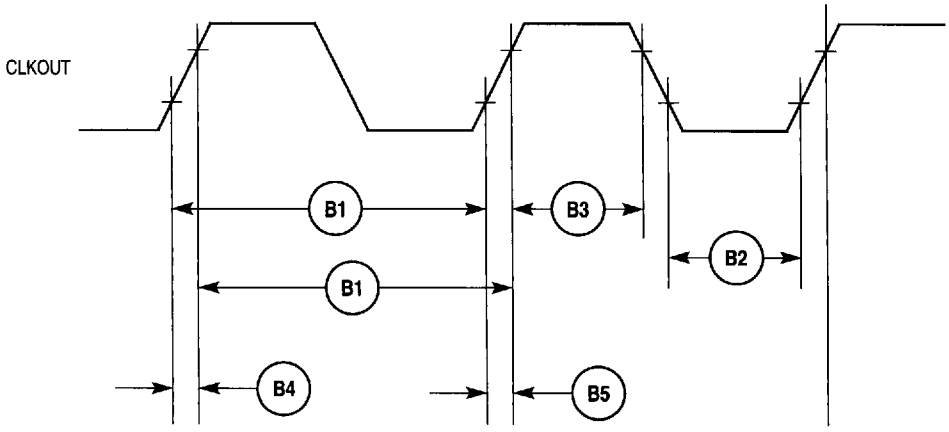


Figure 20-2. External Clock Timing Diagram

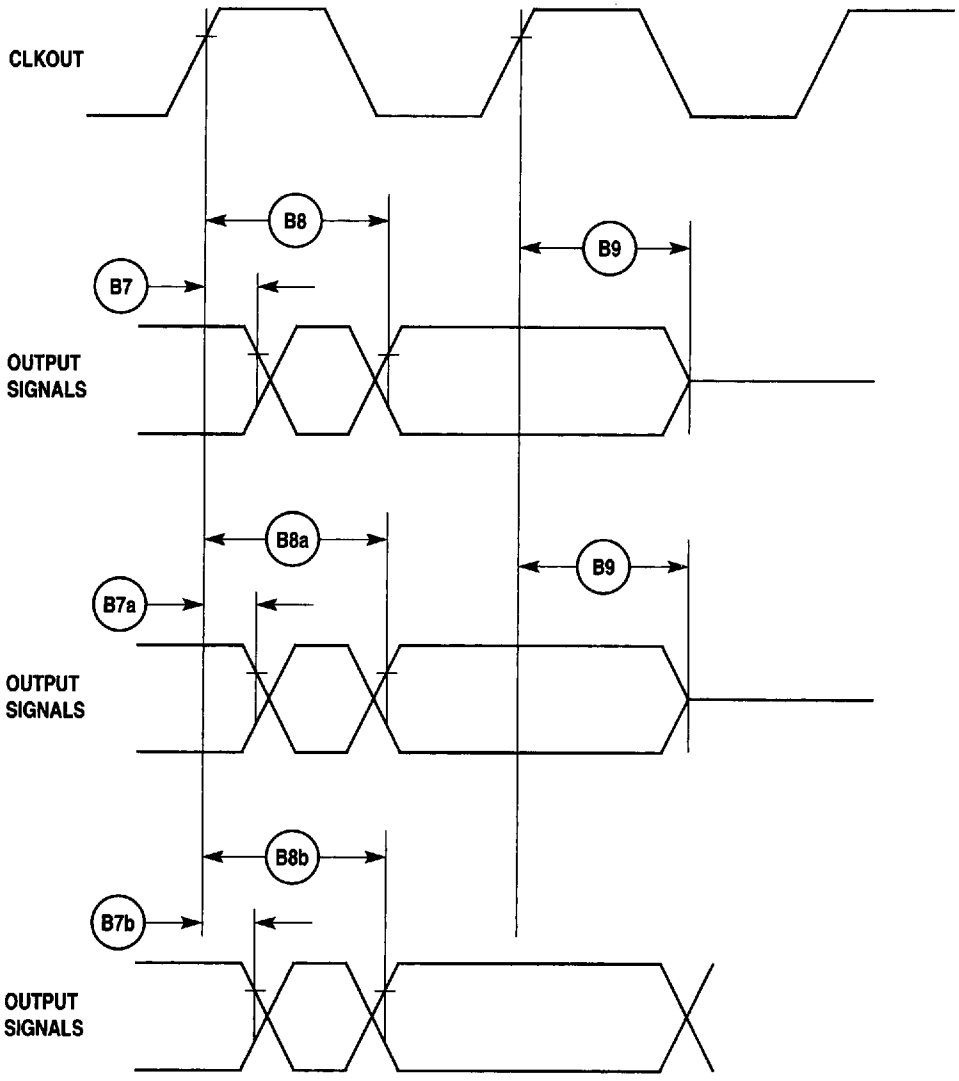


Figure 20-3. Synchronous Output Signals Timing Diagram

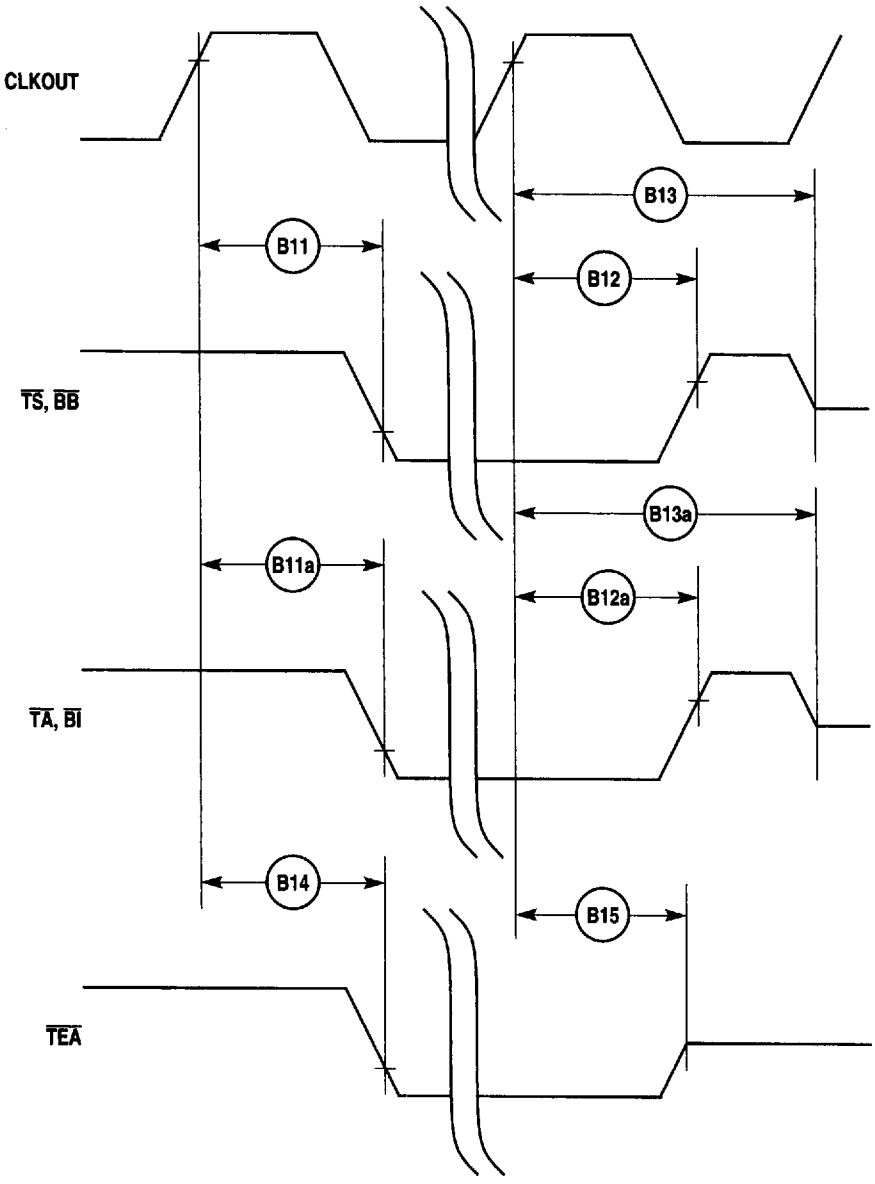


Figure 20-4. Synchronous Active Pull-Up and Open Drain Outputs Signals Timing Diagram

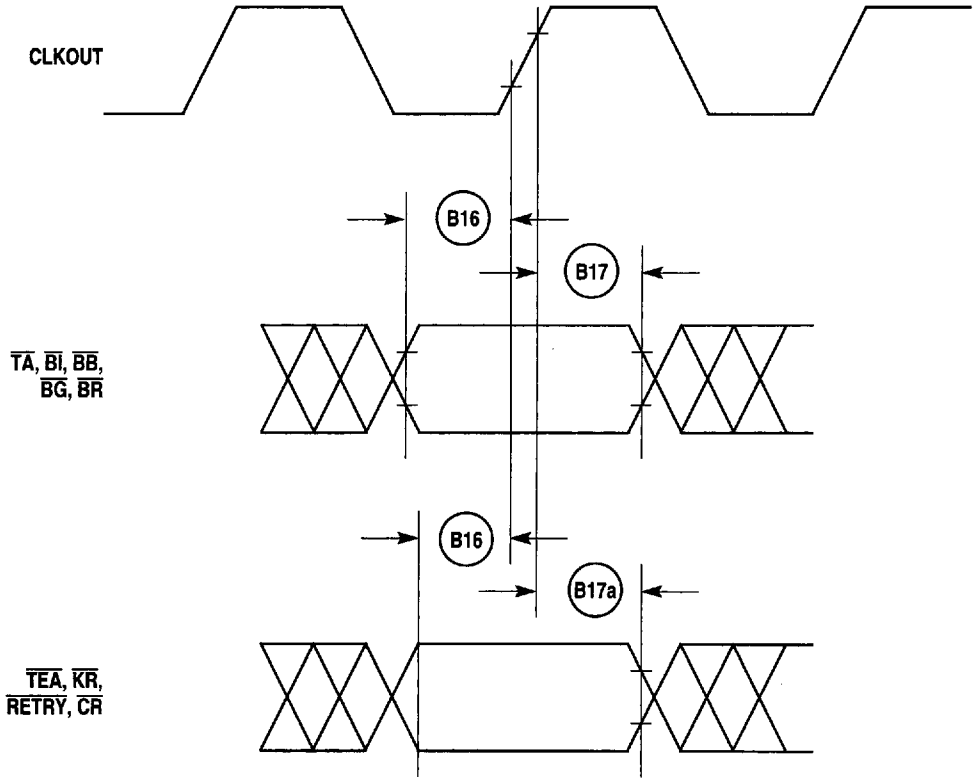


Figure 20-5. Synchronous Input Signals Timing Diagram

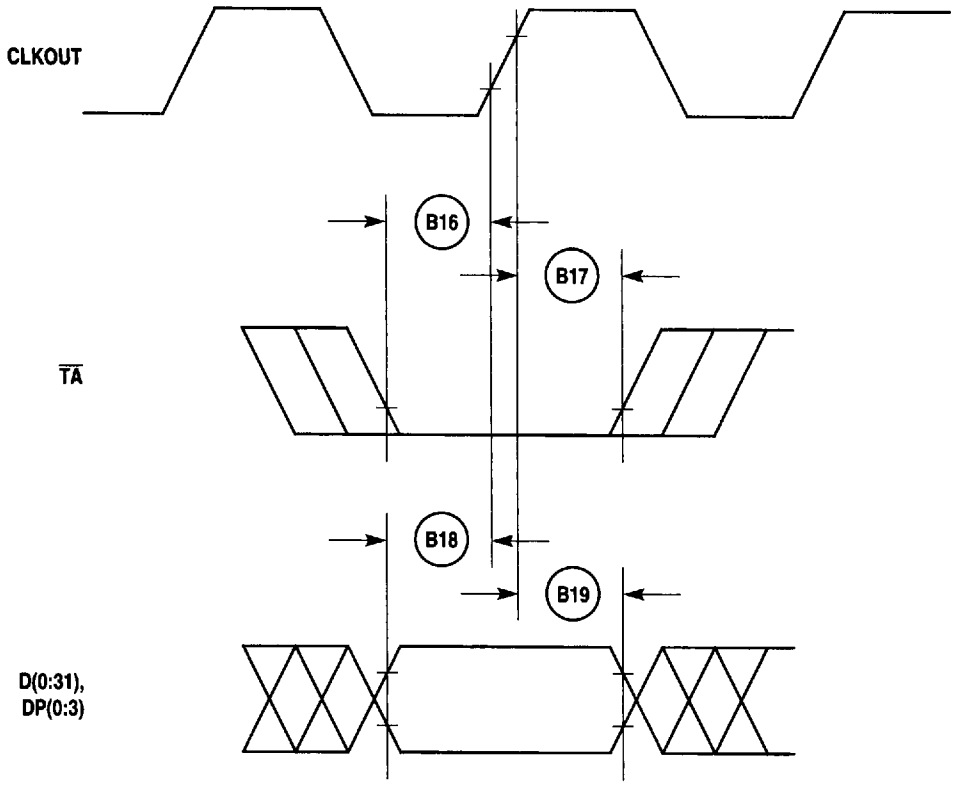


Figure 20-6. Input Data In Normal Case Timing Diagram

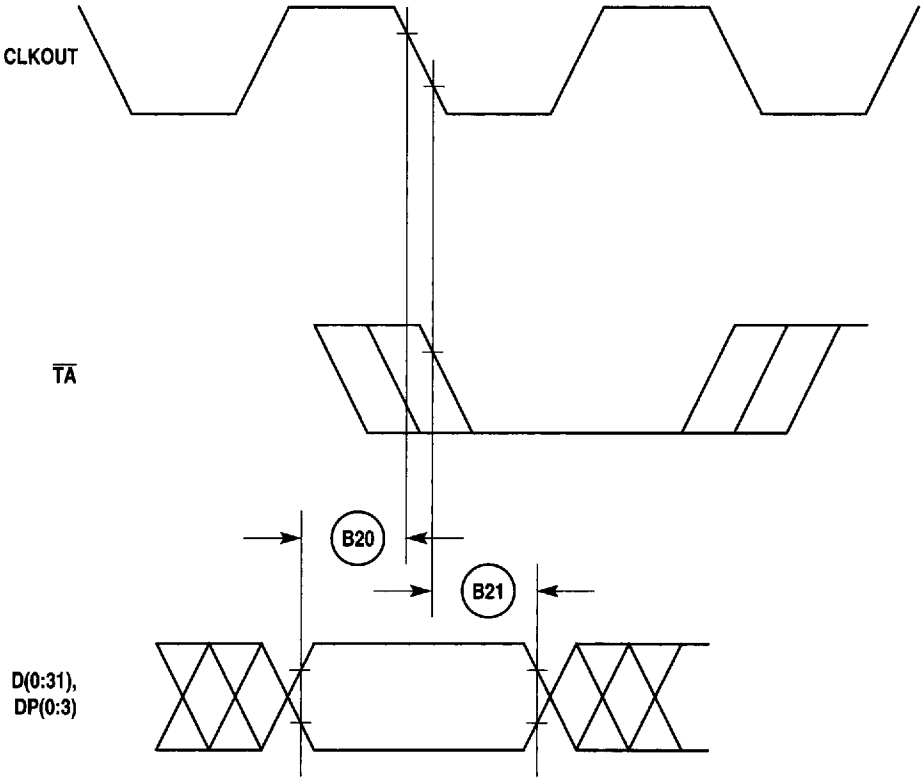


Figure 20-7. Input Data When Controlled by the UPM in the Memory Controller Timing Diagram

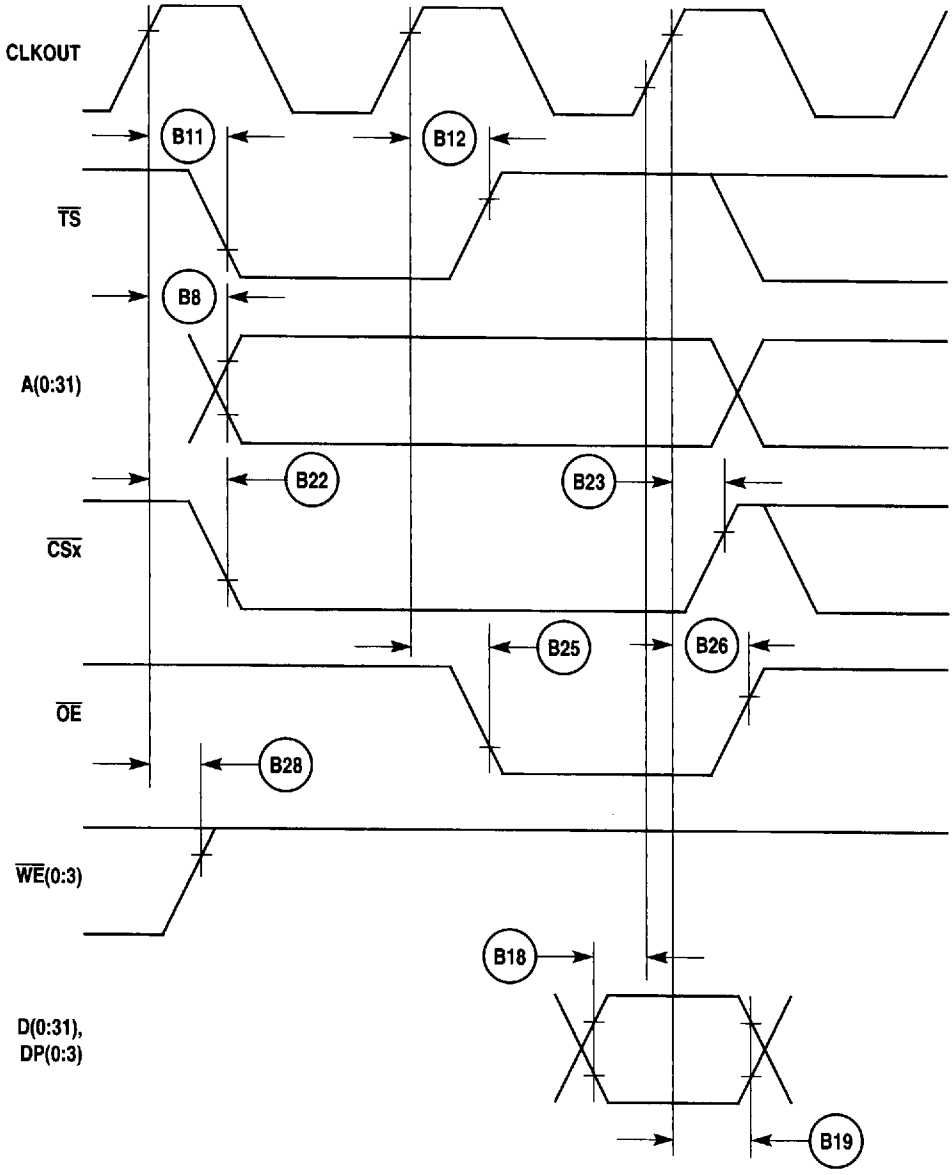


Figure 20-8. External Bus Read Timing Diagram (GPCM Controlled–ACS = '00')

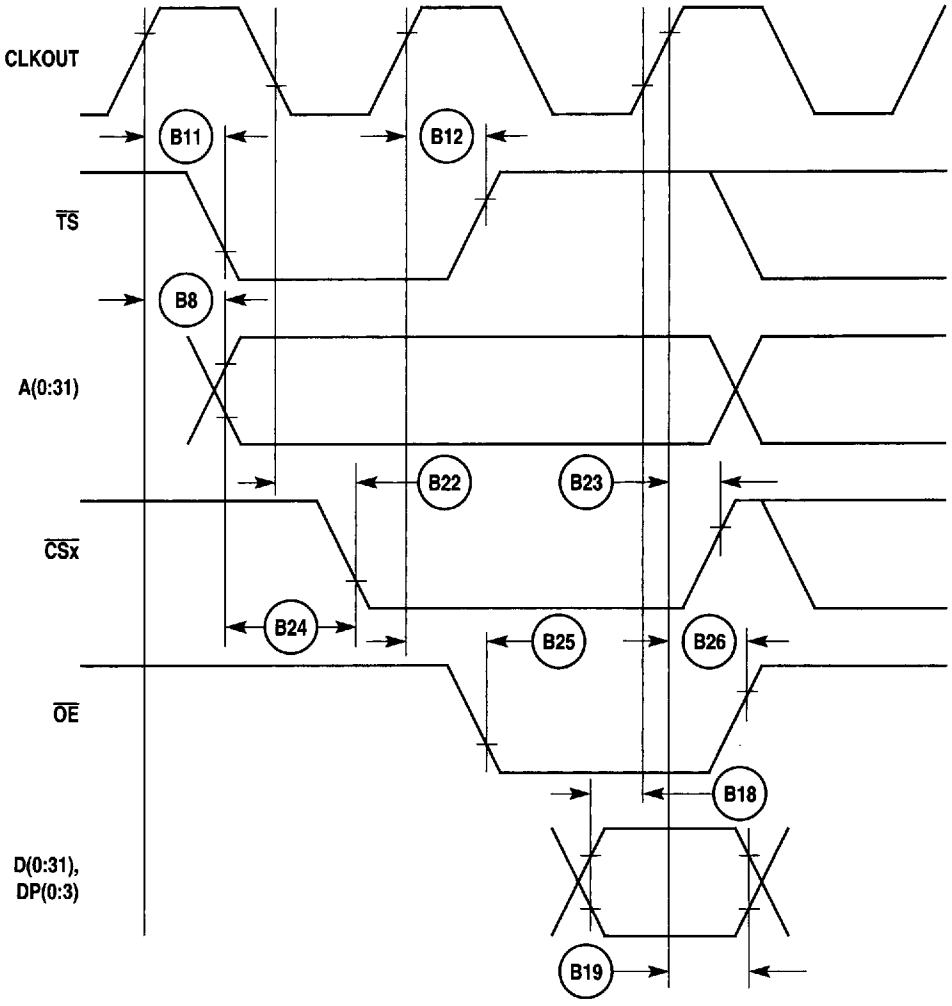


Figure 20-9. External Bus Read Timing Diagram (GPCM Controlled–TRLX = '0', ACS = '10')

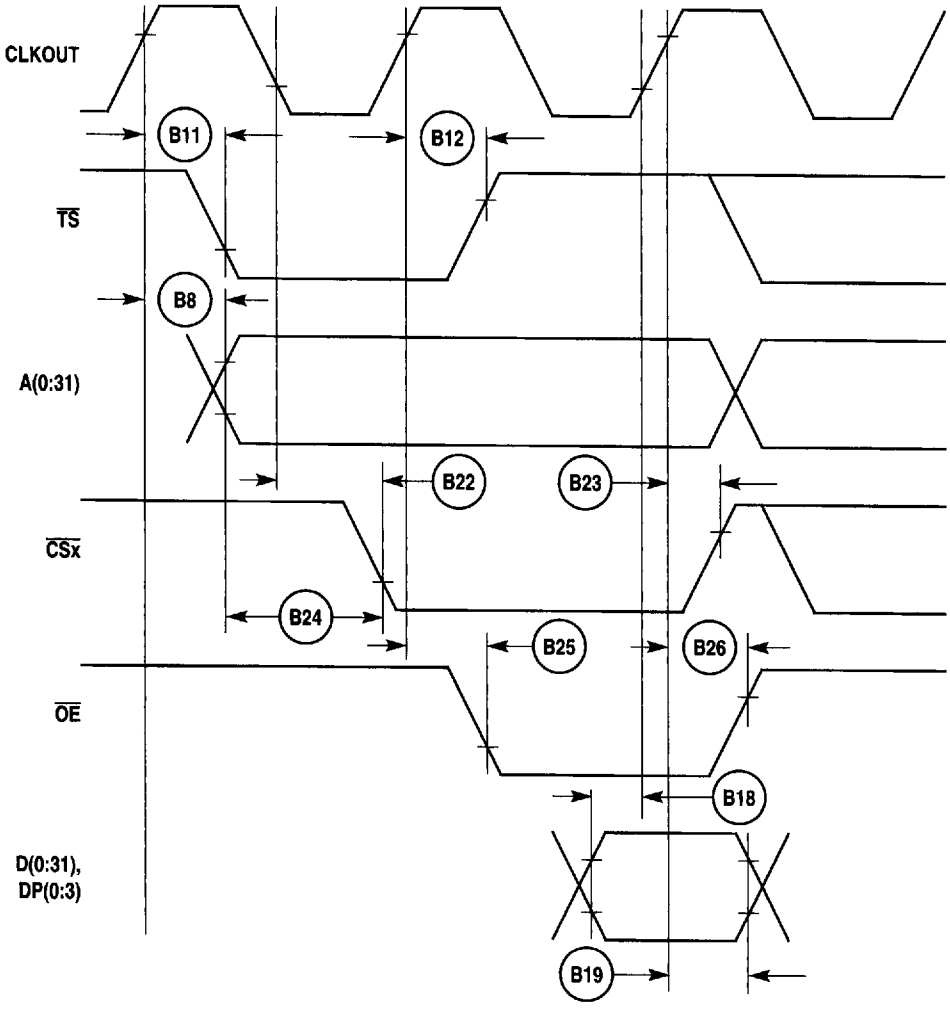


Figure 20-10. External Bus Read Timing Diagram (GPCM Controlled–TRLX = '0', ACS = '11')

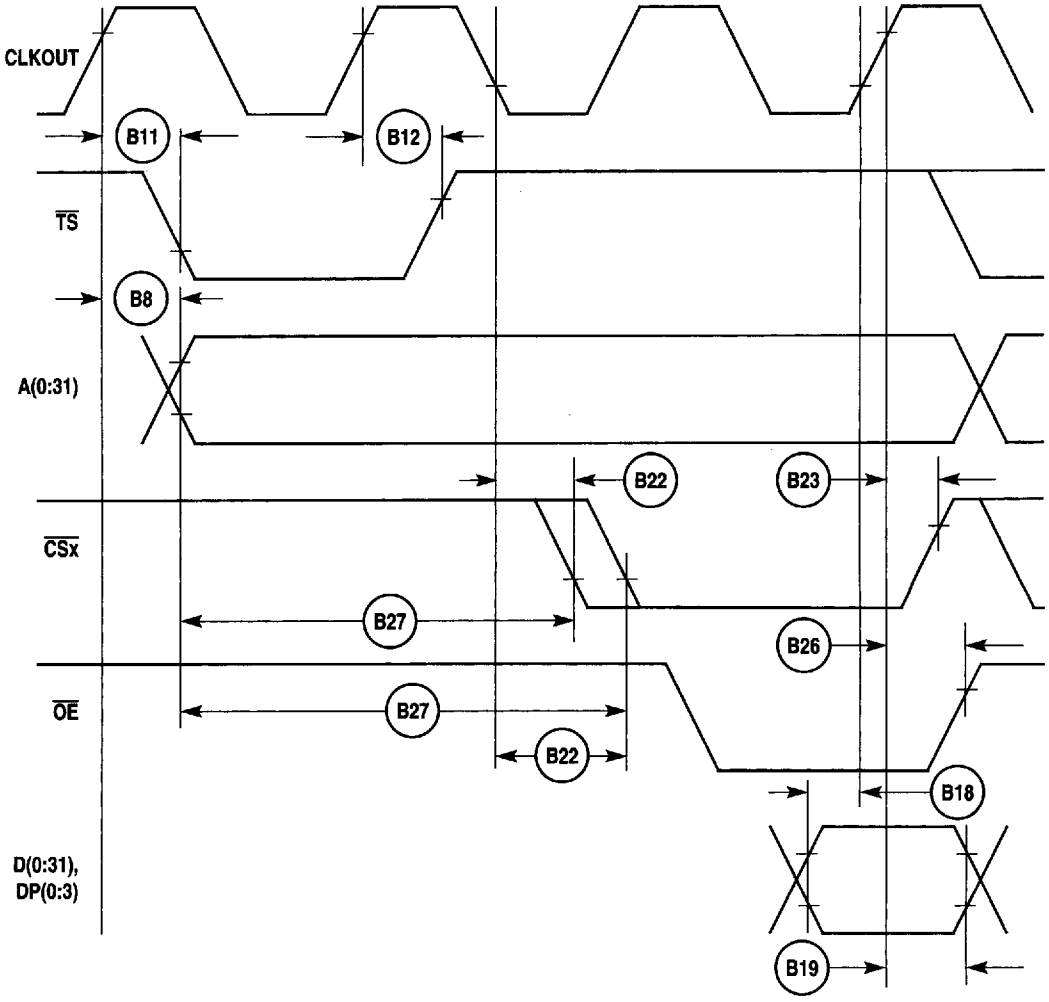


Figure 20-11. External Bus Read Timing Diagram (GPCM Controlled–TRLX = '1', ACS = '10', ACS = '11')

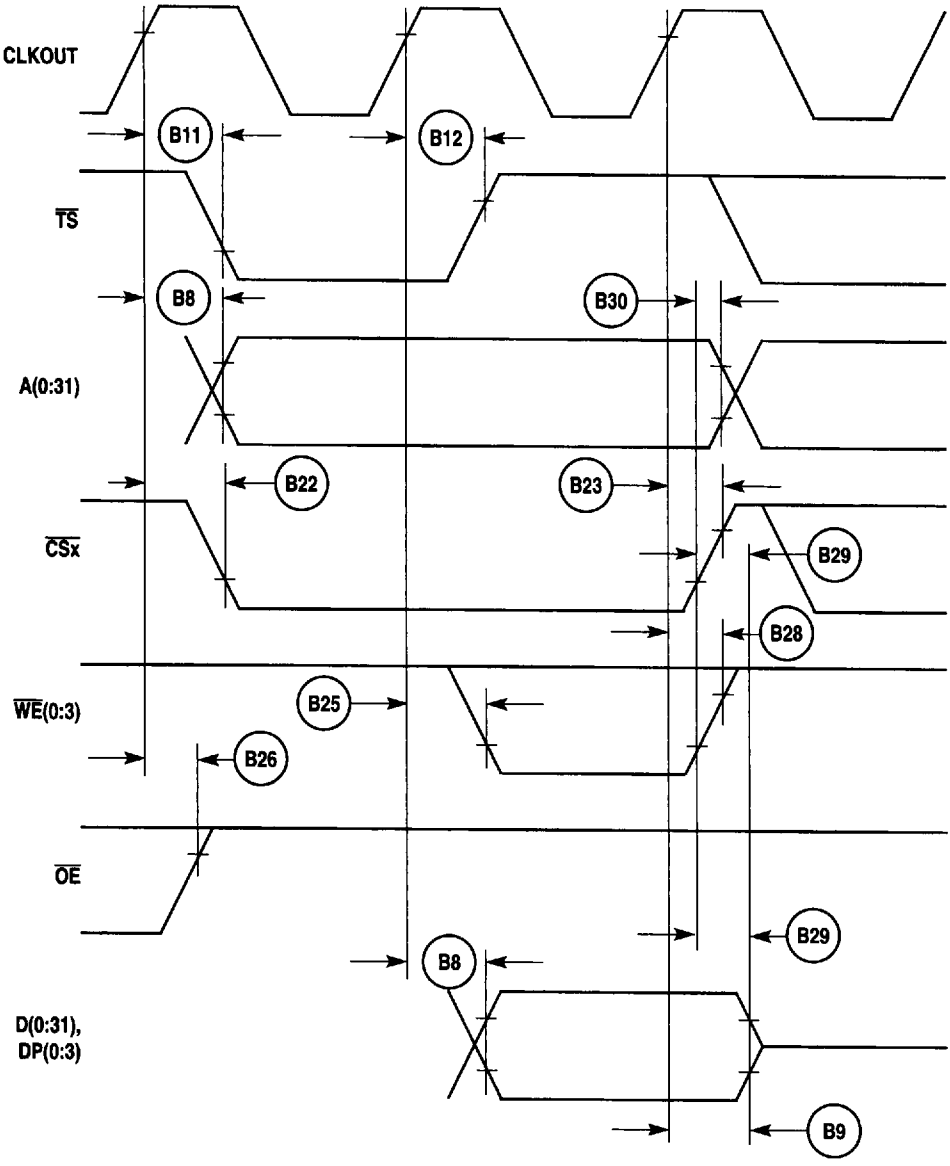


Figure 20-12. External Bus Write Timing Diagram (GPCM Controlled–TRLX = '0', CSNT = '0')

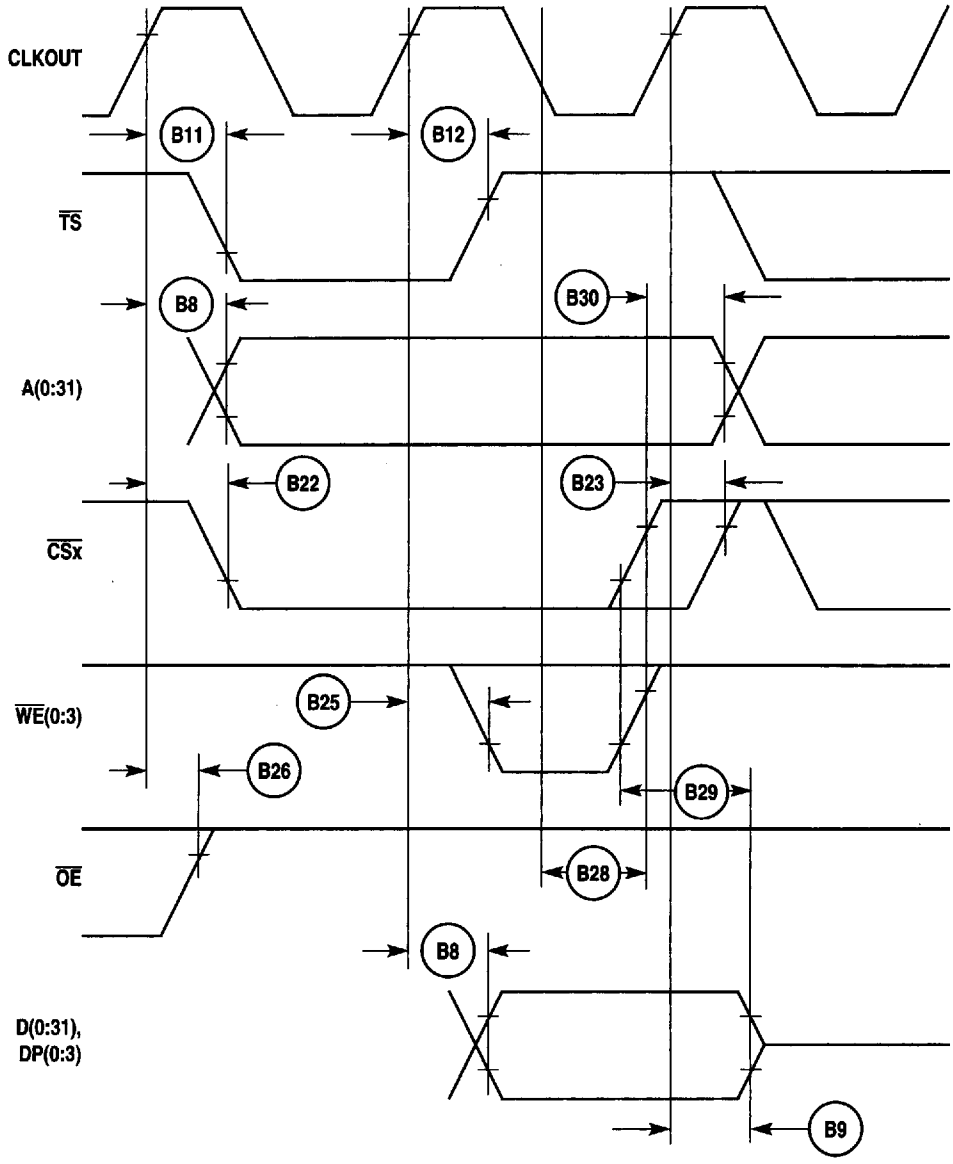


Figure 20-13. External Bus Write Timing Diagram (GPCM Controlled–TRLX = '0', CSNT = '1')

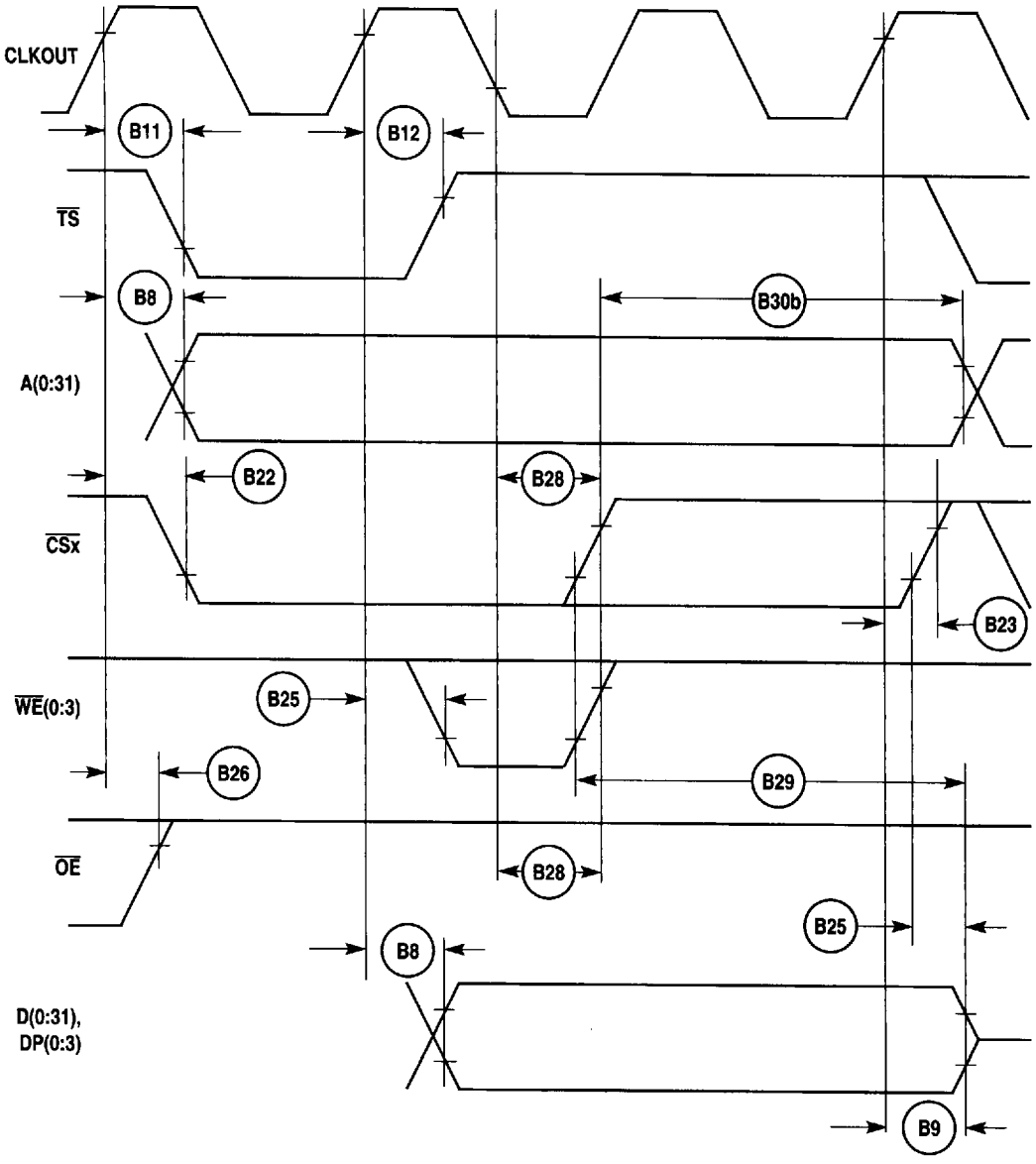


Figure 20-14. External Bus Write Timing Diagram (GPCM Controlled–TRLX = '1', CSNT = '1')

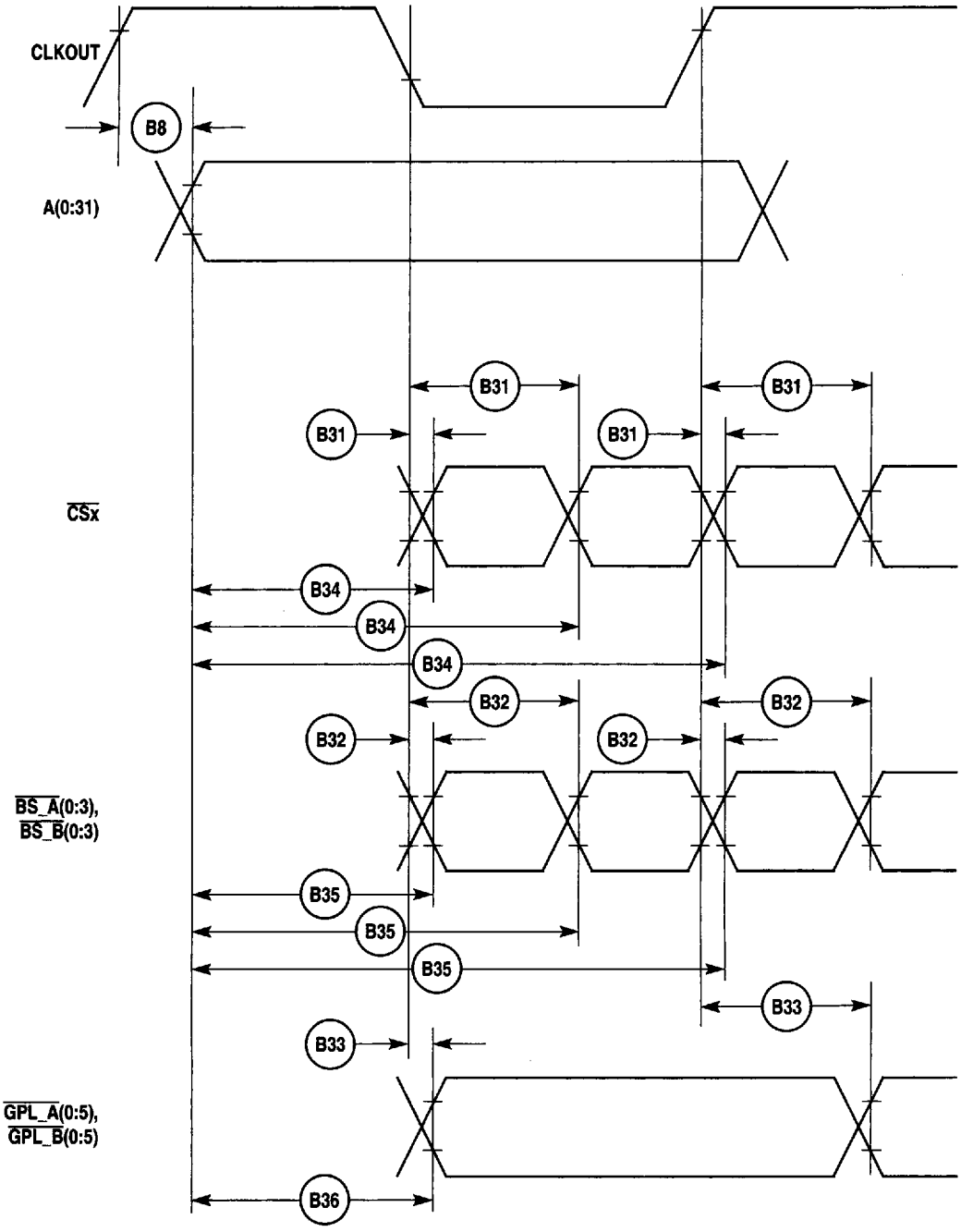


Figure 20-15. External Bus Timing Diagram (UPM Controlled Signals)

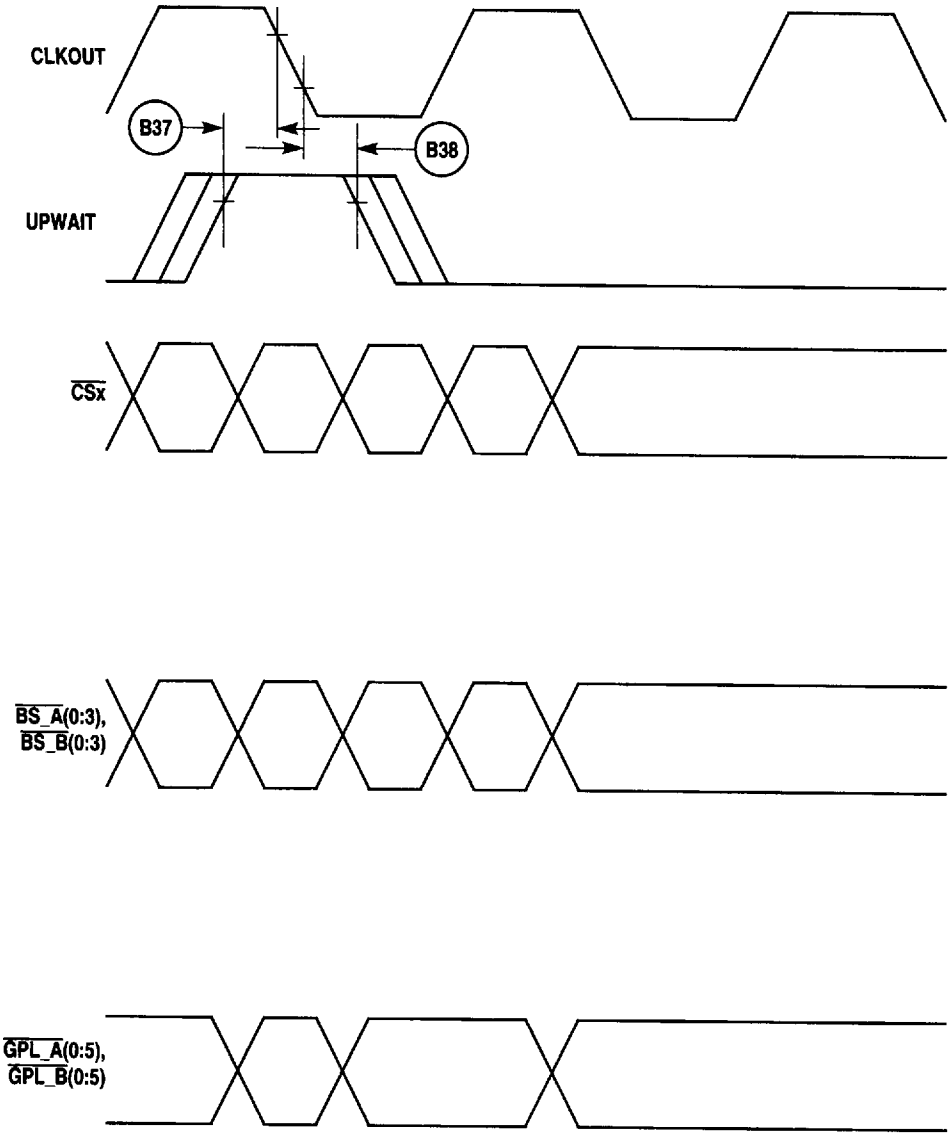


Figure 20-16. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing Diagram

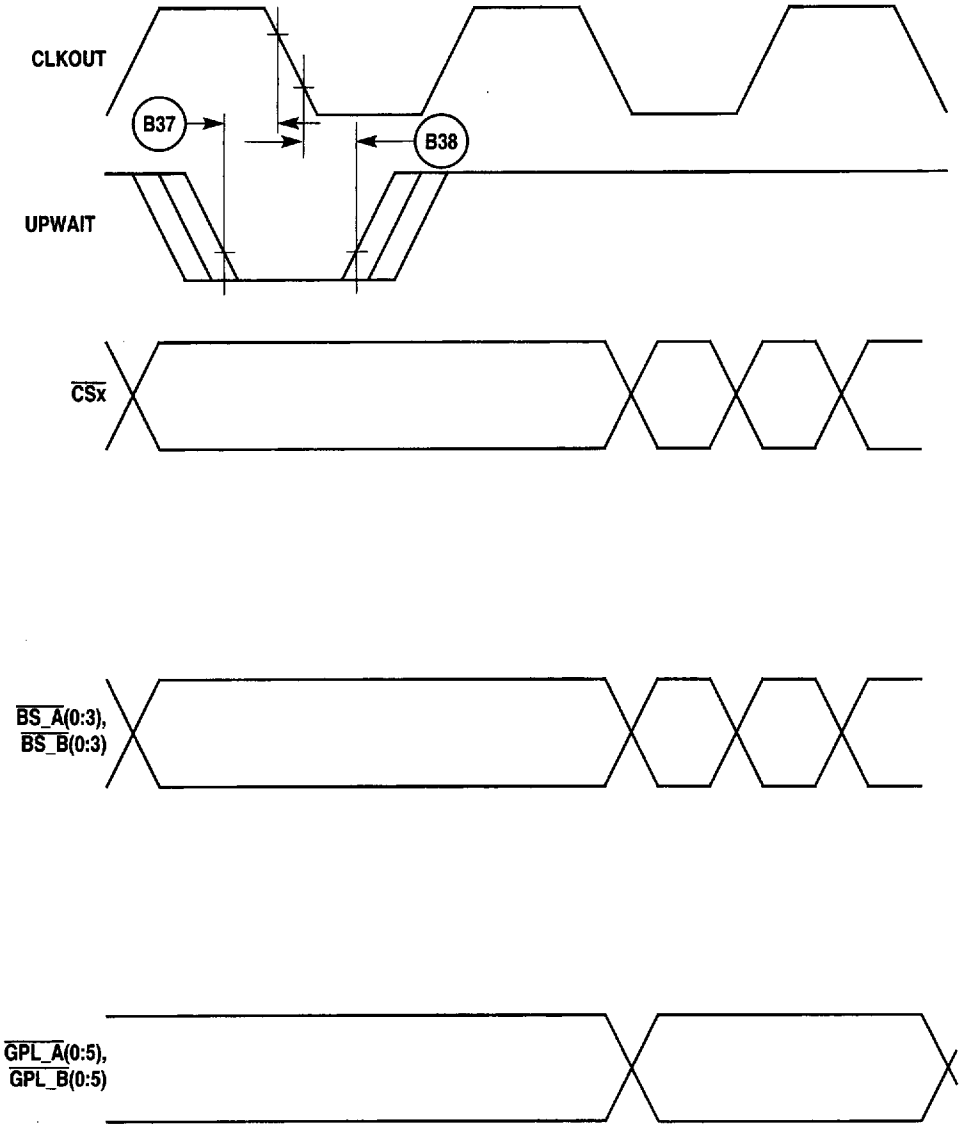


Figure 20-17. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing Diagram

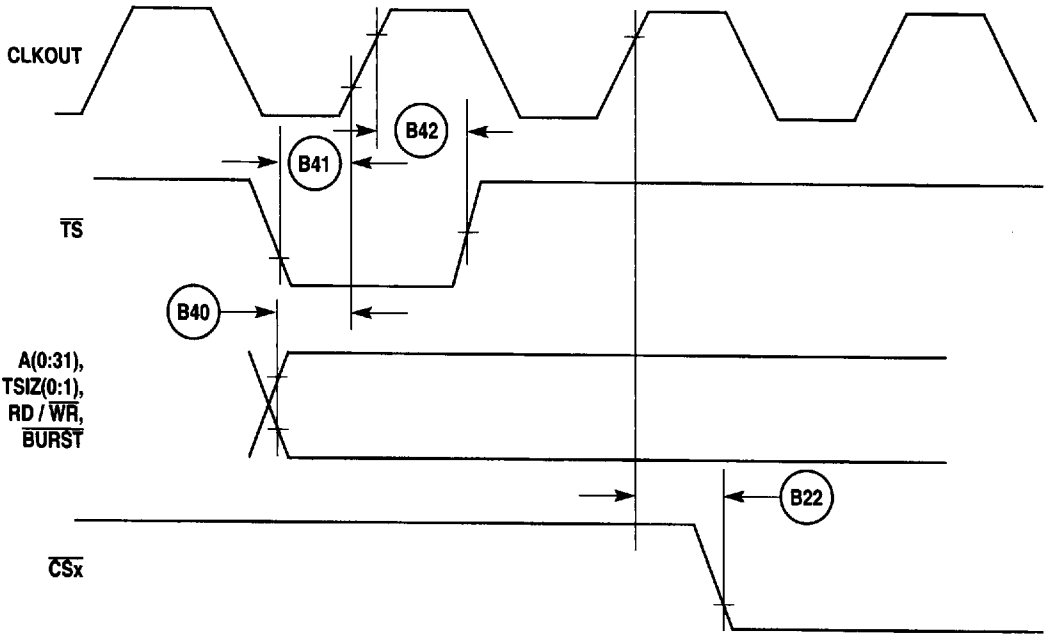


Figure 20-18. Synchronous External Master Access Timing Diagram (GPCM Handled–ACS = '00')

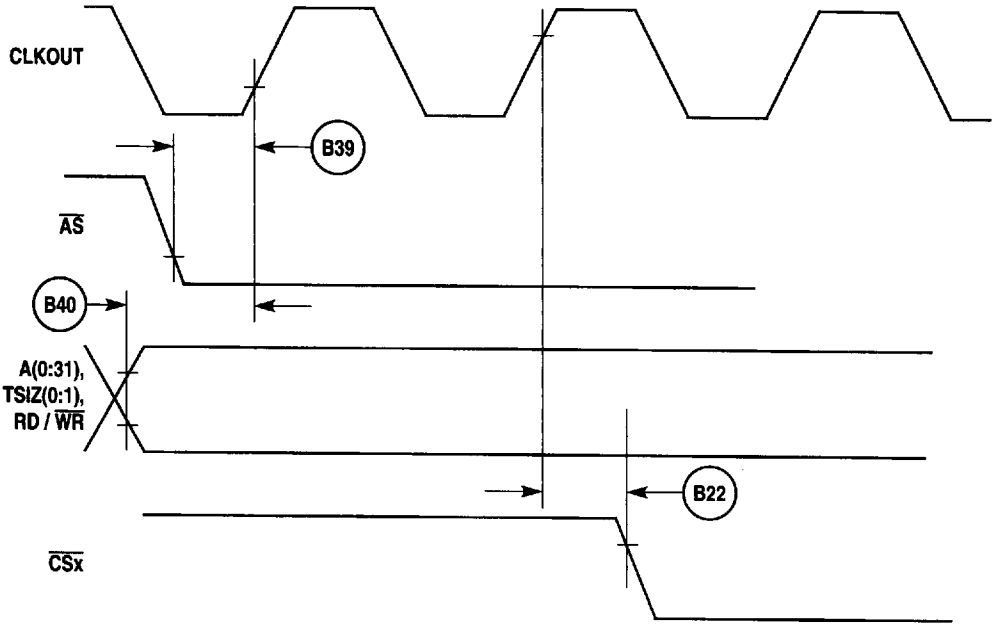


Figure 20-19. Asynchronous External Master Memory Access Timing Diagram (GPCM Controlled–ACS = '00')

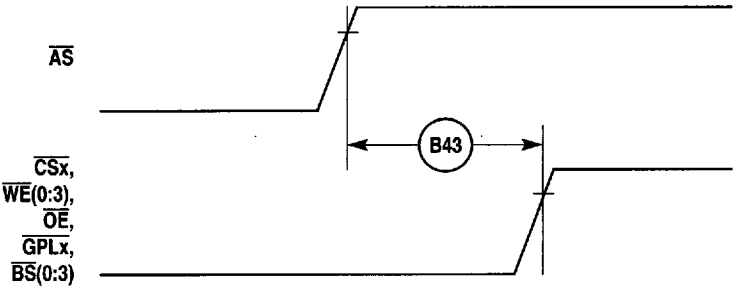


Figure 20-20. Asynchronous External Master Timing Diagram (Control Signals Negation Time)

Table 20-2. Interrupt Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
I39	$\overline{IRQx}$ Valid to CLKOUT Rising Edge (Setup Time) [1]		6	—	6	—	ns
I40	$\overline{IRQx}$ Hold Time After CLKOUT [1]		2	—	2	—	ns
I41	$\overline{IRQx}$ Pulse Width Low		3	—	3	—	ns
I42	$\overline{IRQx}$ Pulse Width High		3	—	3	—	ns
I43	$\overline{IRQx}$ Edge to Edge Time	4*TC	160	—	80	—	ns

NOTES:
1. The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
2. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC860 is able to support.

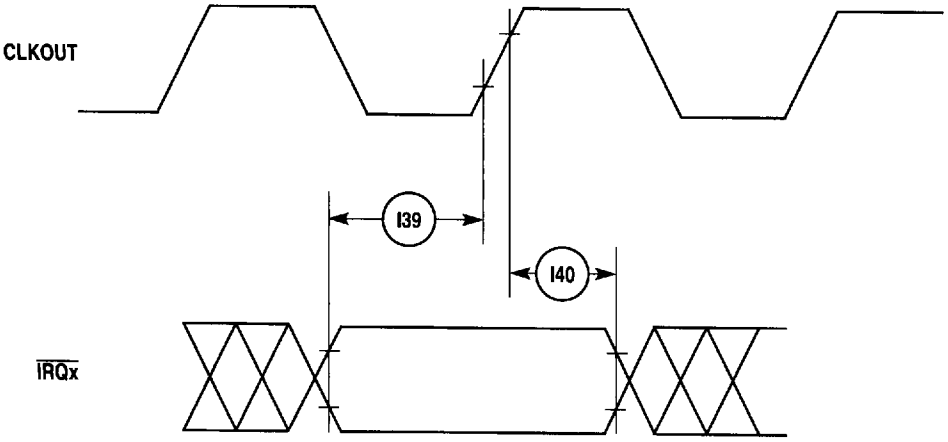


Figure 20-21. Interrupt Detection Timing Diagram for External Level-Sensitive Lines

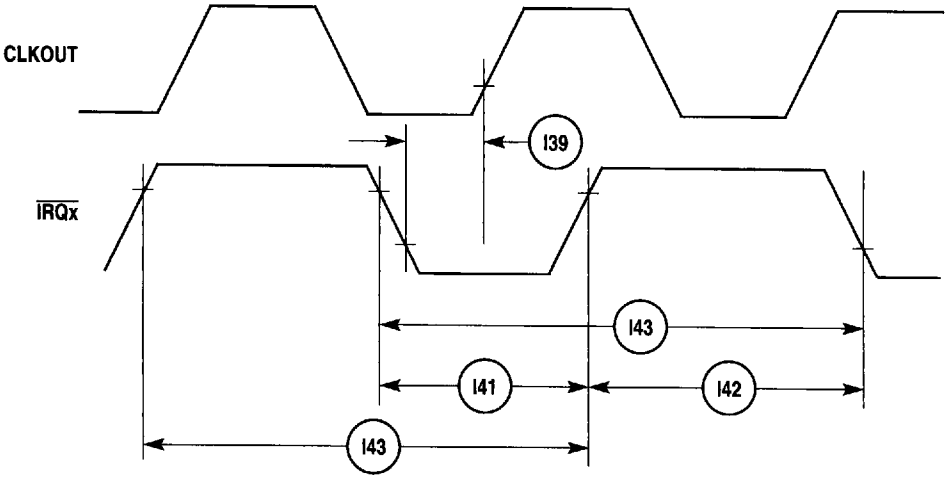


Figure 20-22. Interrupt Detection Timing Diagram for External Edge-Sensitive Lines

Table 20-3. PCMCIA Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
P44	A(0:31), $\overline{REG}$ Valid to PCMCIA Strobe Asserted [1]		28	—	13	—	ns
P45	A(0:31), $\overline{REG}$ Valid to ALE Negation [1]		38	—	18	—	ns
P46	CLKOUT to $\overline{REG}$ Valid		—	19	5	13	ns
P47	CLKOUT to $\overline{REG}$ Invalid		11	—	6	—	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ Asserted		10	19	5	13	—
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ Negated		10	19	5	13	ns
P50	CLKOUT to $\overline{PCOE}$, $\overline{IORD}$, $\overline{PCWE}$, $\overline{IOWR}$ Assert Time		—	12	—	11	ns
P51	CLKOUT to $\overline{PCOE}$, $\overline{IORD}$, $\overline{PCWE}$, $\overline{IOWR}$ Negate Time		3	12	2	11	ns
P52	CLKOUT to ALE Assert Time		10	19	5	13	ns
P53	CLKOUT to ALE Negate Time		—	19	—	13	ns
P54	$\overline{PCWE}$, $\overline{IOWR}$ Negated to D(0:31)Invalid [2]		8	—	3	—	ns
P55	$\overline{WAITA}$ and $\overline{WAITB}$ Valid to CLKOUT Rising Edge [3]		8	—	8	—	ns
P56	CLKOUT Rising Edge to $\overline{WAITA}$ and $\overline{WAITB}$ Invalid [3]		2	—	2	—	ns

NOTES:
1. PSST = 1. Otherwise add PSST times cycle time.
2. PSHT = 0. Otherwise add PSHT times cycle time.
3. These synchronous timings define when the $\overline{WAITx}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{WAITx}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. Refer to **Section 12 PCMCIA Interface.**

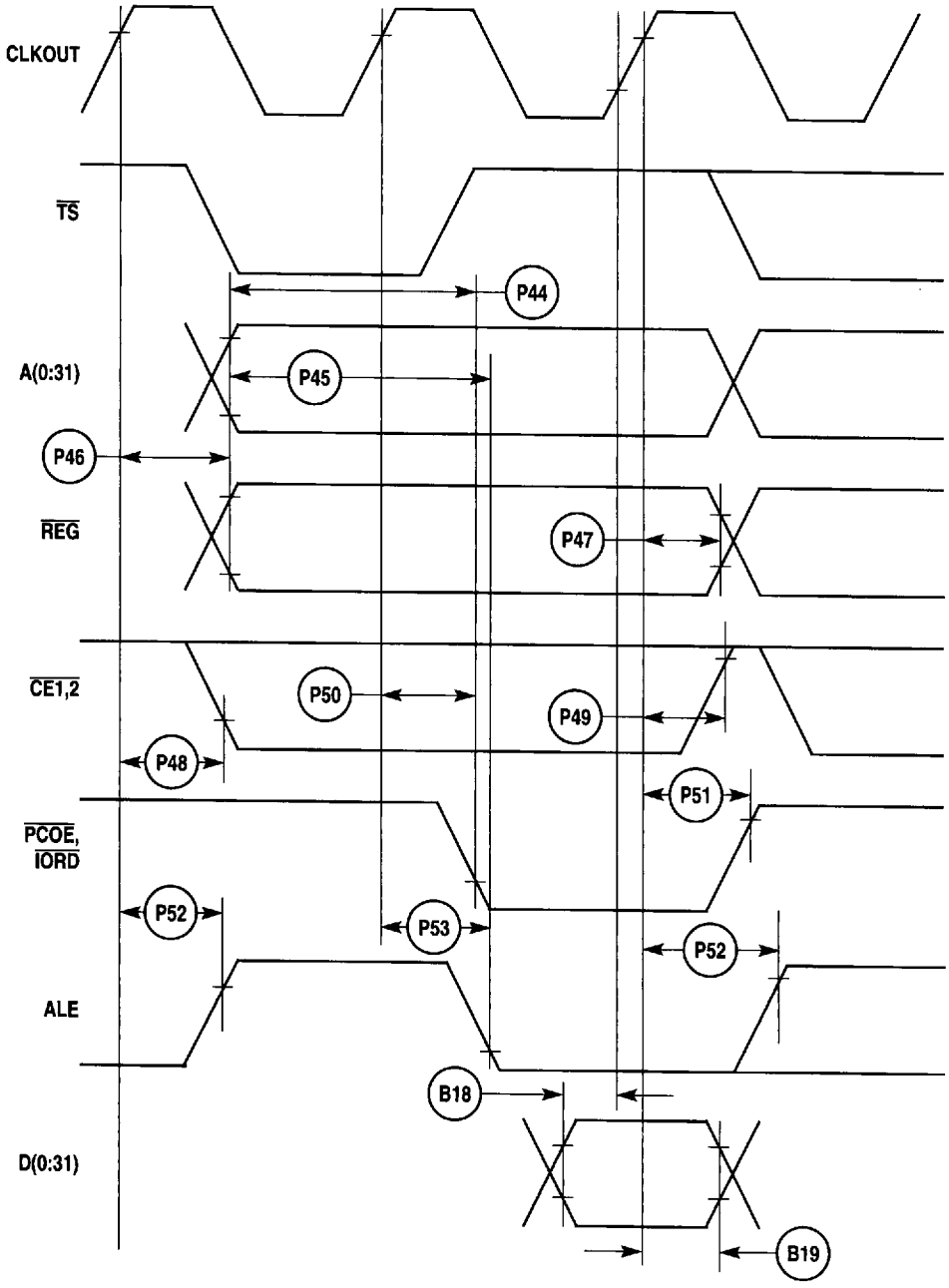


Figure 20-23. PCMCIA Access Cycles Timing Diagram (External Bus Read)

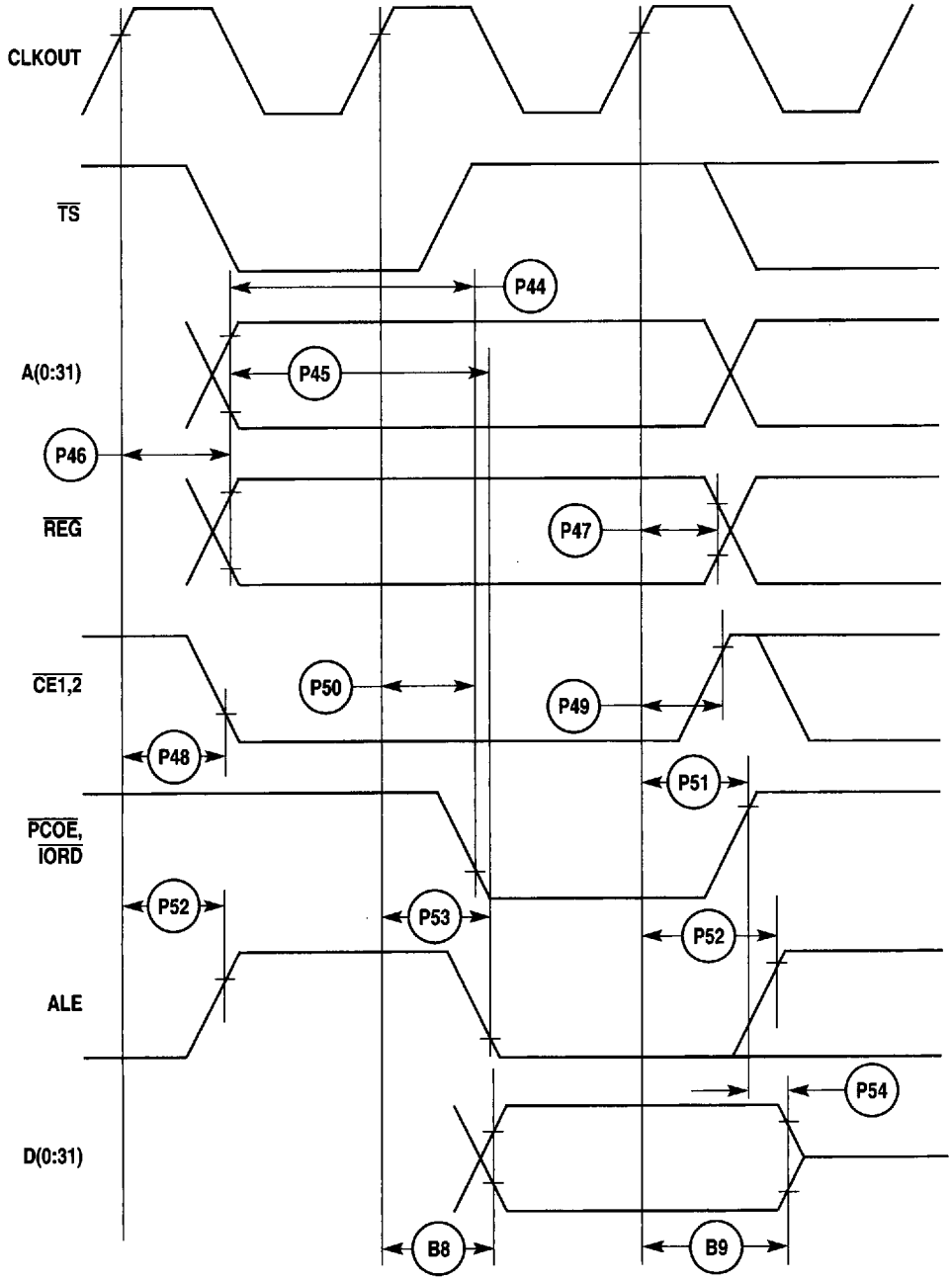


Figure 20-24. PCMCIA Access Cycles Timing Diagram (External Bus Write)

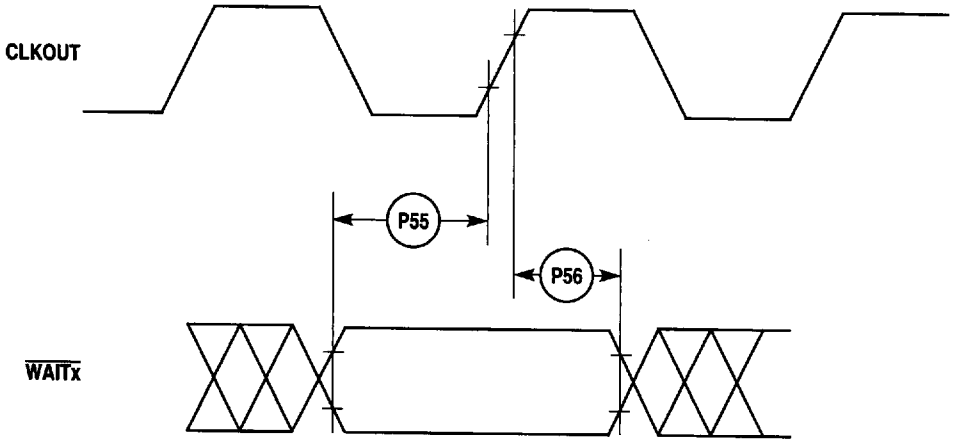


Figure 20-25. PCMCIA Wait Signals Detection Timing Diagram

Table 20-4. PCMCIA Port Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
P57	CLKOUT to OPx Valid		—	25	—	19	ns
P58	$\overline{\text{HRESET}}$ Negated to OPx Drive *		30	—	18	—	ns
P59	IP_Xx Valid to CLKOUT Rising Edge		6	—	5	—	ns
P60	CLKOUT Rising Edge to IP_Xx Invalid		2	—	1	—	ns

NOTE: * OP2 and OP3 only.

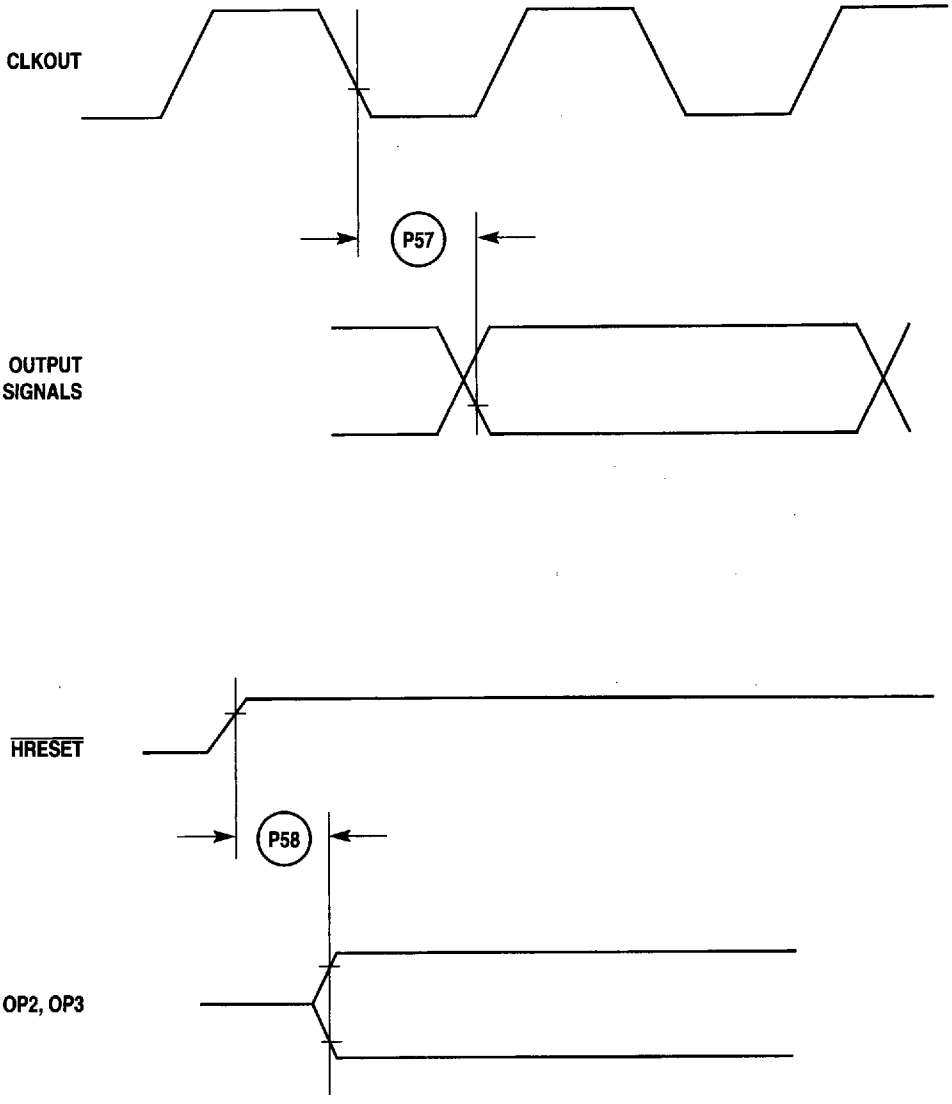


Figure 20-26. PCMCIA Output Port Timing Diagram

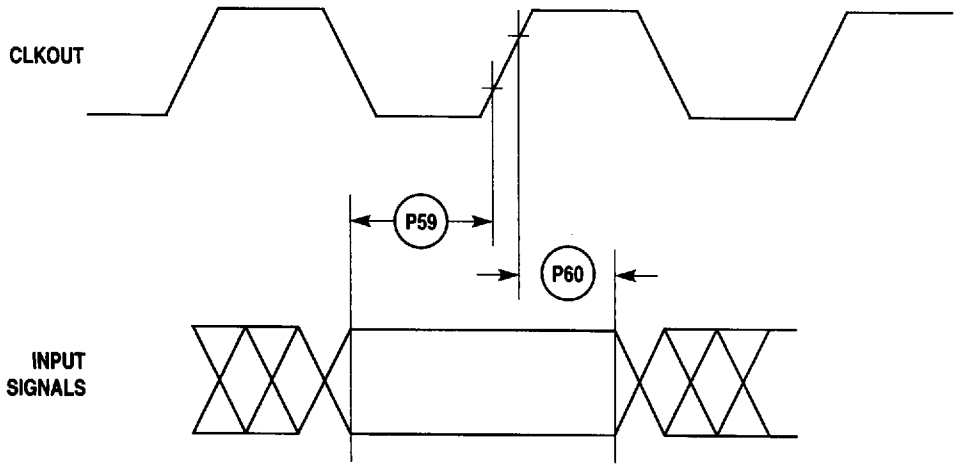


Figure 20-27. PCMCIA Input Port Timing Diagram

Table 20-5. Debug Port Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
D61	DSCK Cycle Time		120	—	60	—	ns
D62	DSCK Clock Pulse Width		50	—	25	—	ns
D63	DSCK Rise and Fall Times		0	3	0	3	ns
D64	DSDI Input Data Setup Time		TBD	—	TBD	—	ns
D65	DSDI Data Hold Time		TBD	—	TBD	—	ns
D66	DSCK High to DSDO Data Valid		0	TBD	0	TBD	ns
D67	DSCK High to DSDO Invalid		0	TBD	0	TBD	ns

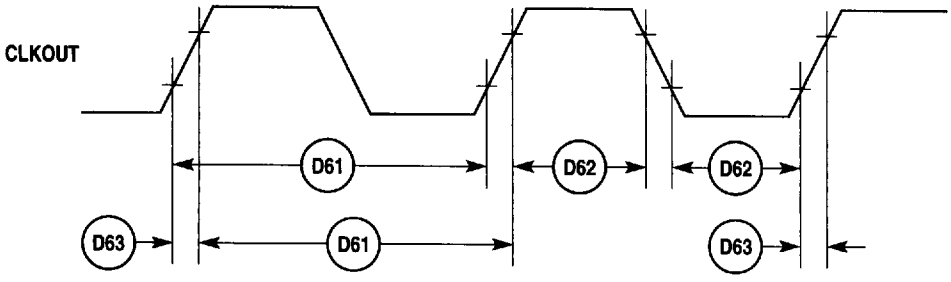


Figure 20-28. Debug Port Clock Input Timing Diagram

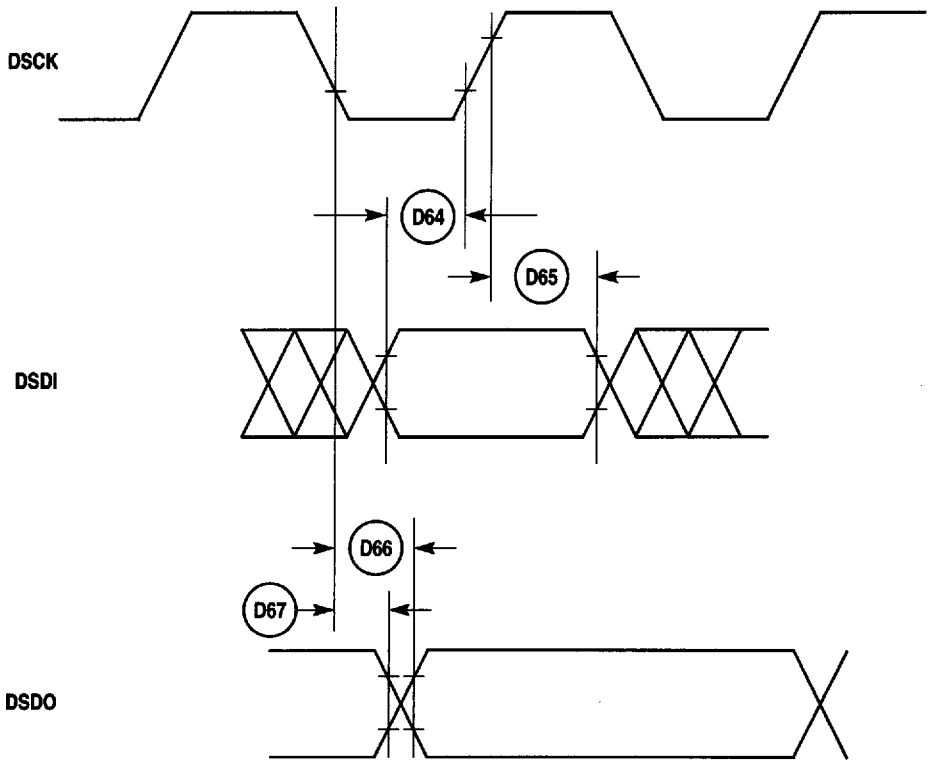


Figure 20-29. Debug Port Timing Diagram

Table 20-6. RESET Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
R68	$\overline{\text{HRESET}}$ Setup Time		TBD	—	TBD	—	ns
R69	CLKOUT to $\overline{\text{HRESET}}$ High Impedance		—	20	—	20	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ High Impedance		—	20	—	20	ns
R71	$\overline{\text{RSTCONF}}$ Pulse Width	17*TC	680	—	425	—	ns
R72	$\overline{\text{RSTCONF}}$ Setup Time		TBD	—	TBD	—	ns
R73	Configuration Data to $\overline{\text{HRESET}}$ Rising Edge Setup Time	15*TC+TCC	650	—	425	—	ns
R74	Configuration Data to $\overline{\text{RSTCONF}}$ Rising Edge Setup Time		650	—	425	—	ns
R75	Configuration Data Hold Time After $\overline{\text{RSTCONF}}$ Negation		0	—	0	—	ns
R76	Configuration Data Hold Time After $\overline{\text{HRESET}}$ Negation		0	—	0	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ Asserted to Data Out Drive		—	25	—	25	ns
R78	$\overline{\text{RSTCONF}}$ Negated to Data Out High Impedance		—	25	—	25	ns
R79	CLKOUT of Last Rising Edge Before Chip Three-States $\overline{\text{HRESET}}$ to Data Out High Impedance		—	25	—	25	ns
R80	DSDI, DSCK Setup	3 TCC	120	—	75	—	ns
R81	DSDI, DSCK Hold Time		0	—	0	—	ns
R82	$\overline{\text{SRESET}}$ Negated to CLKOUT Rising Edge for DSDI and DSCK Sample	8TCC	320	—	200	—	ns

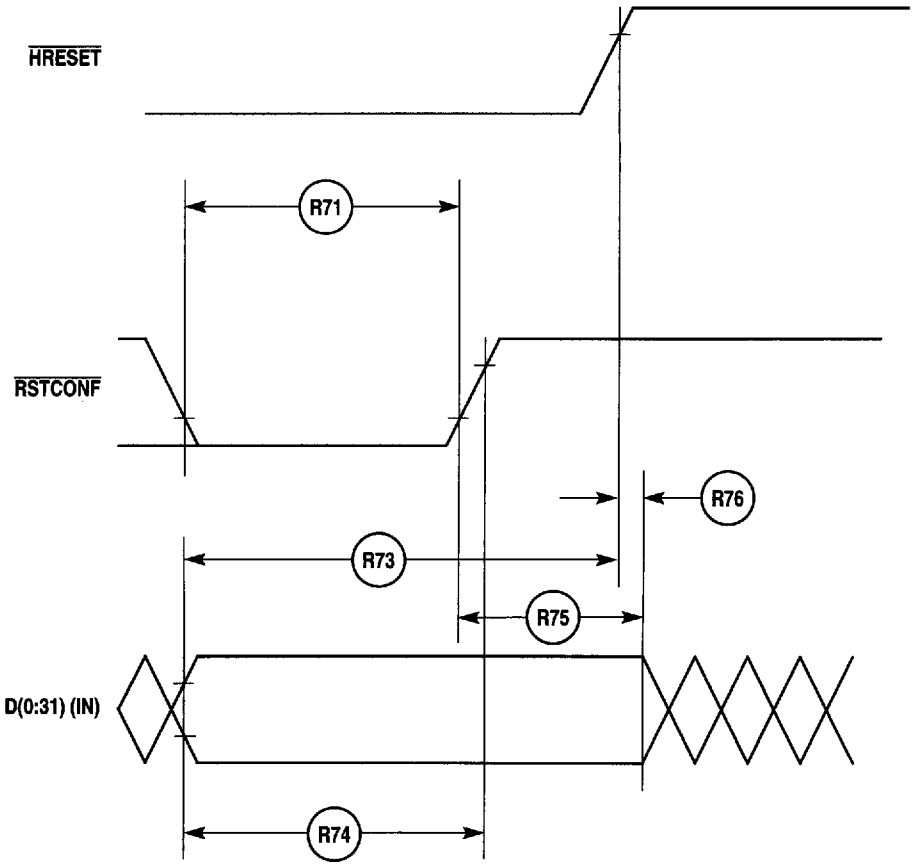


Figure 20-30. Reset Timing Diagram (Configuration from Data Bus)

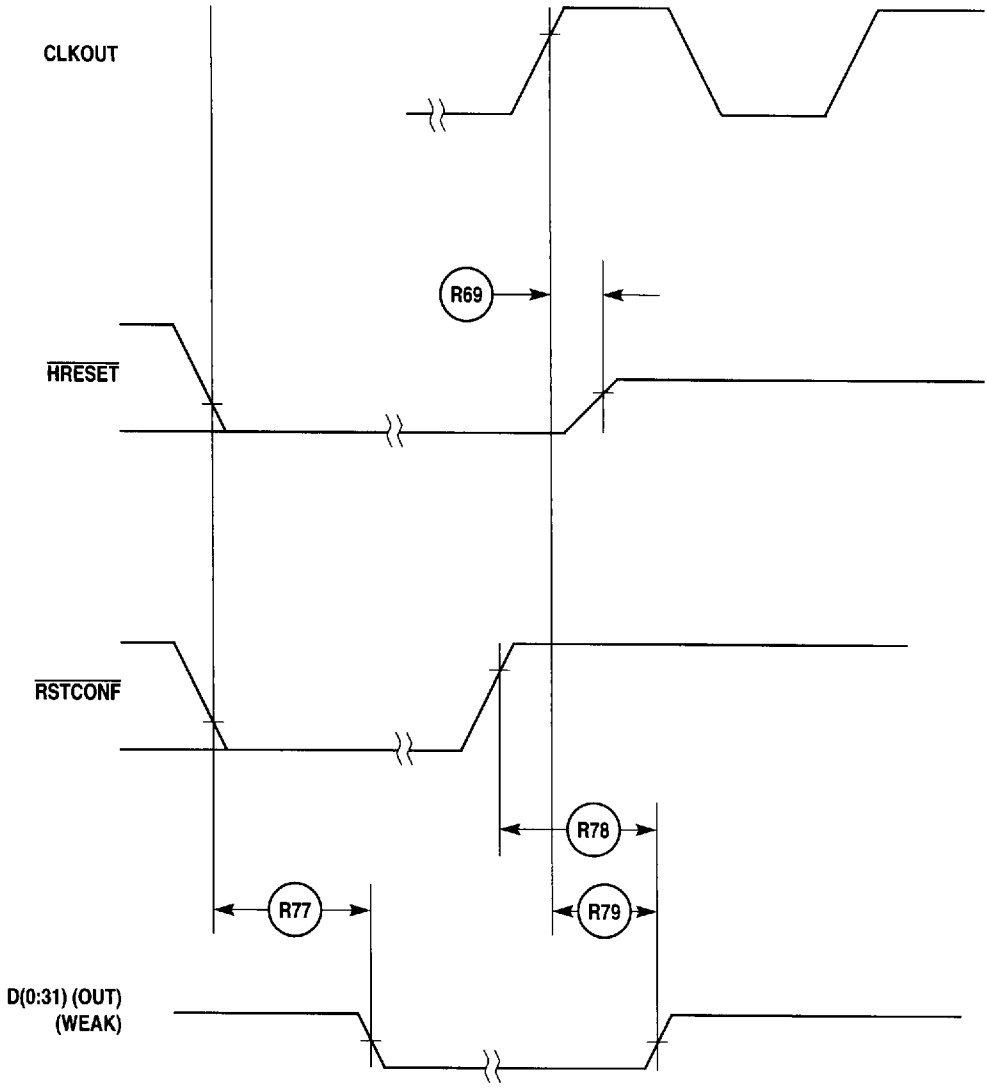


Figure 20-31. Reset Timing Diagram–MPC860 Data Bus Weak Drive During Configuration

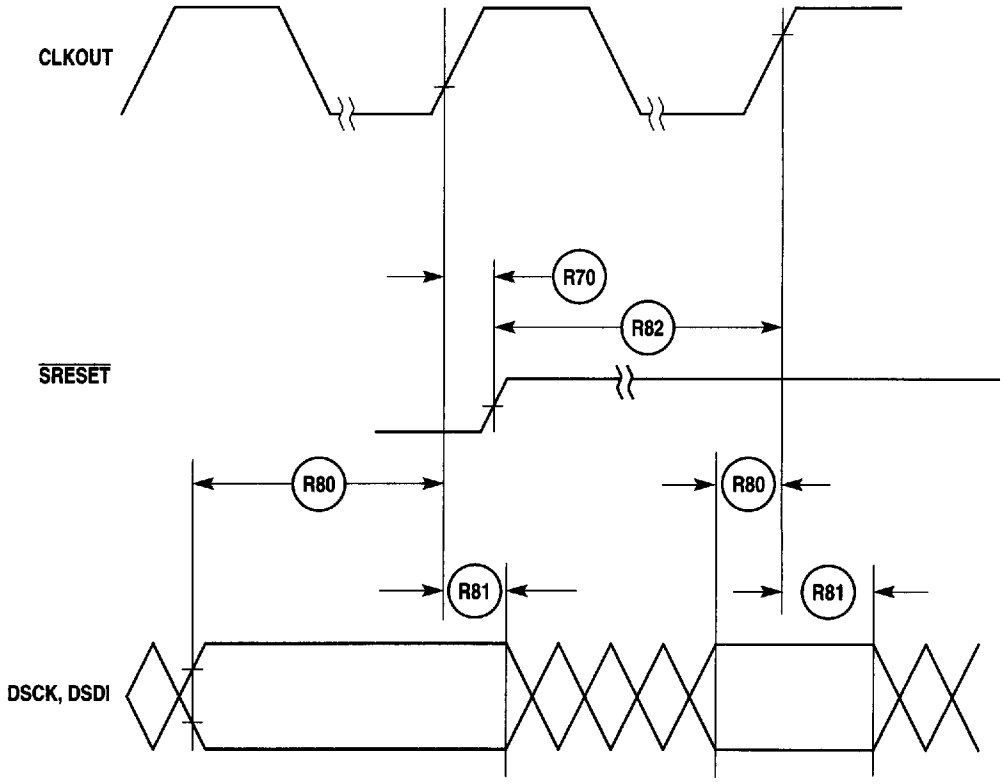


Figure 20-32. Reset Timing Diagram–Debug Port Configuration

20.6 IEEE 1149.1 ELECTRICAL SPECIFICATIONS

Table 20-7. JTAG Timing

NUM	CHARACTERISTIC	EXPRESSION	25 MHZ		40 MHZ		UNIT
			MIN	MAX	MIN	MAX	
J82	TCK Cycle Time		100	—	100	—	ns
J83	TCK Clock Pulse Width Measured at 1.5 V		40	—	40	—	ns
J84	TCK Rise and Fall Times		0	10	0	10	ns
J85	TMS, TDI Data Setup Time		5	—	5	—	ns
J86	TMS, TDI Data Hold Time		25	—	25	—	ns
J87	TCK Low to TDO Data Valid		—	20	—	20	ns
J88	TCK Low to TDO Data Invalid		0	—	0	—	ns
J89	TCK Low to TDO High Impedance		—	20	—	20	ns
J90	TRST Assert Time		100	—	100	—	ns
J91	TRST Setup Time to TCK Low		40	—	40	—	ns
J92	TCK Falling Edge to Output Valid		—	50	—	50	ns
J93	TCK Falling Edge to Output Valid Out of High Impedance		—	50	—	50	ns
J94	TCK Falling Edge to Output High Impedance		—	50	—	50	ns
J95	Boundary Scan Input Valid to TCK Rising Edge		50	—	50	—	ns
J96	TCK Rising Edge to Boundary Scan Input Invalid		50	—	50	—	ns

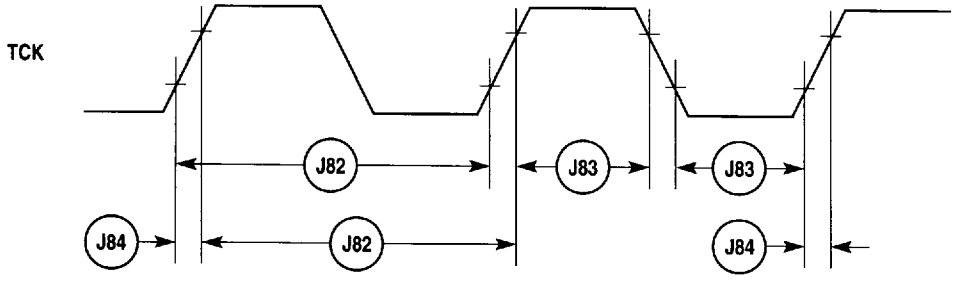


Figure 20-33. JTAG Test Clock Input Timing Diagram

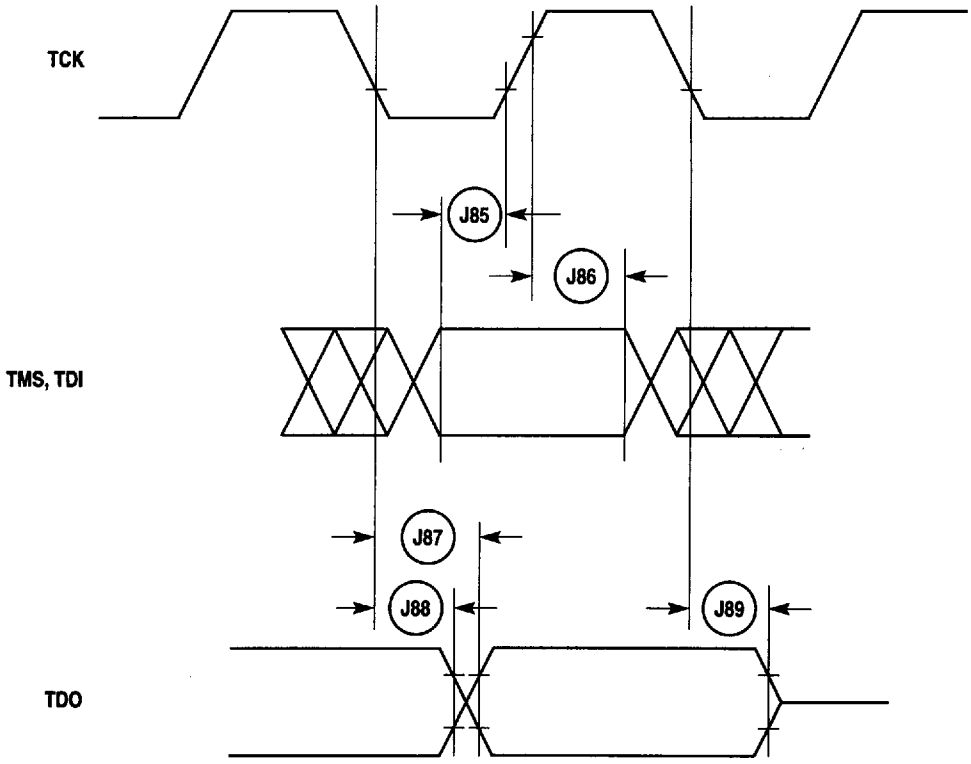


Figure 20-34. JTAG–Test Access Port Timing Diagram

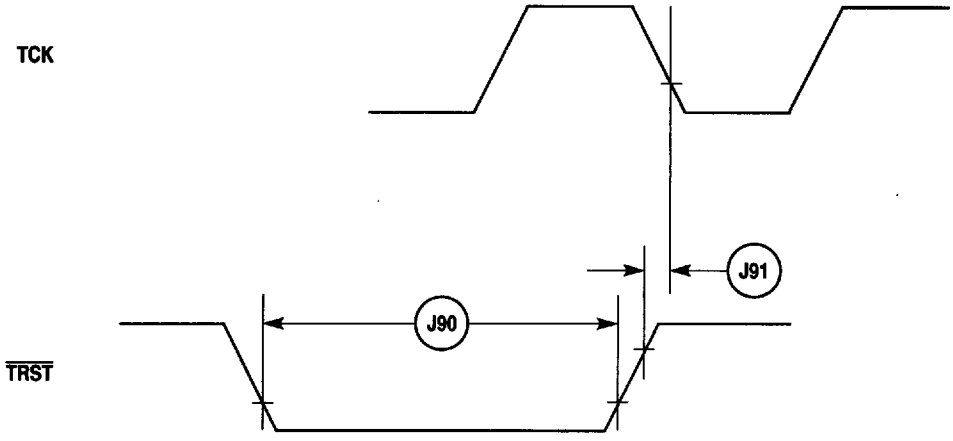


Figure 20-35. JTAG–$\overline{\text{TRST}}$ Timing Diagram

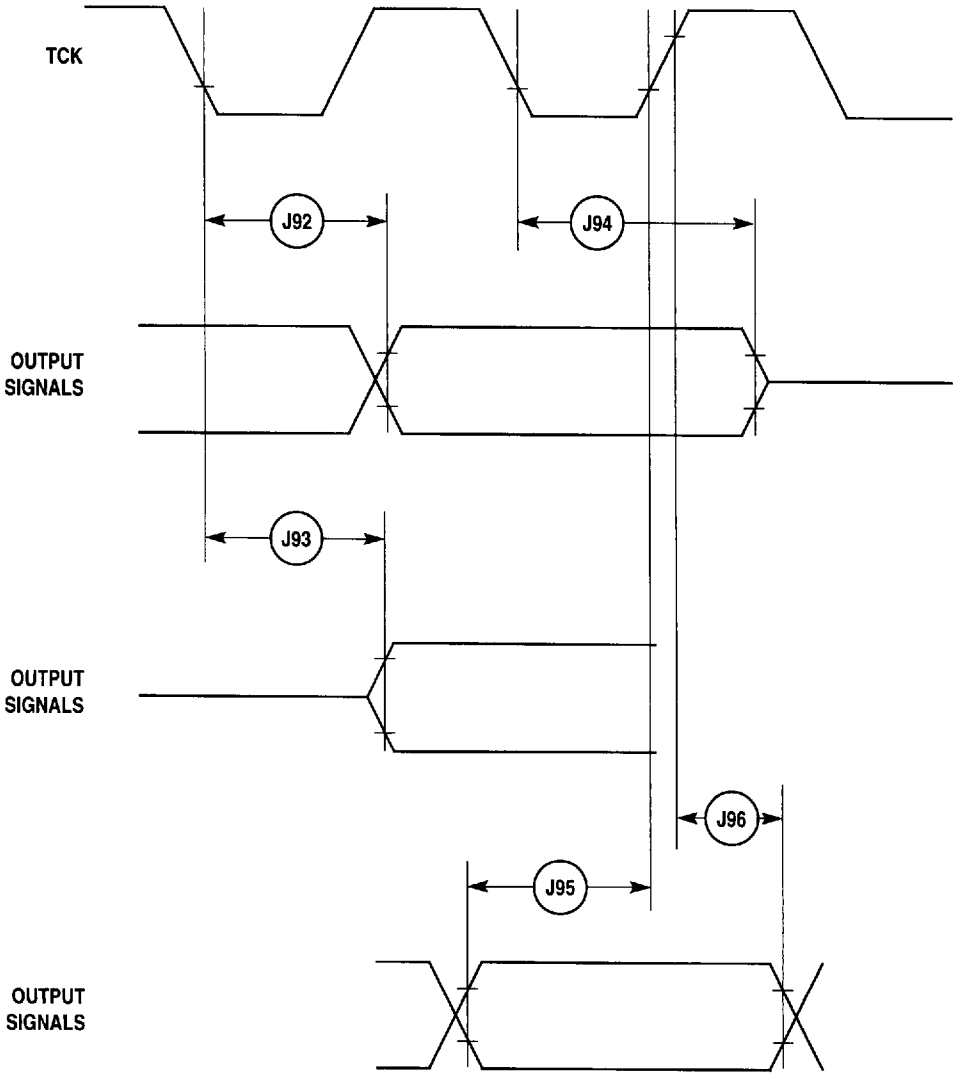


Figure 20-36. Boundary Scan (JTAG) Timing Diagram

SECTION 22
MECHANICAL DATA AND ORDERING INFORMATION

22.1 ORDERING INFORMATION

The following table identifies the packages and operating frequencies available for the MPC860.

Table 1. MPC860 Package/Frequency Availability

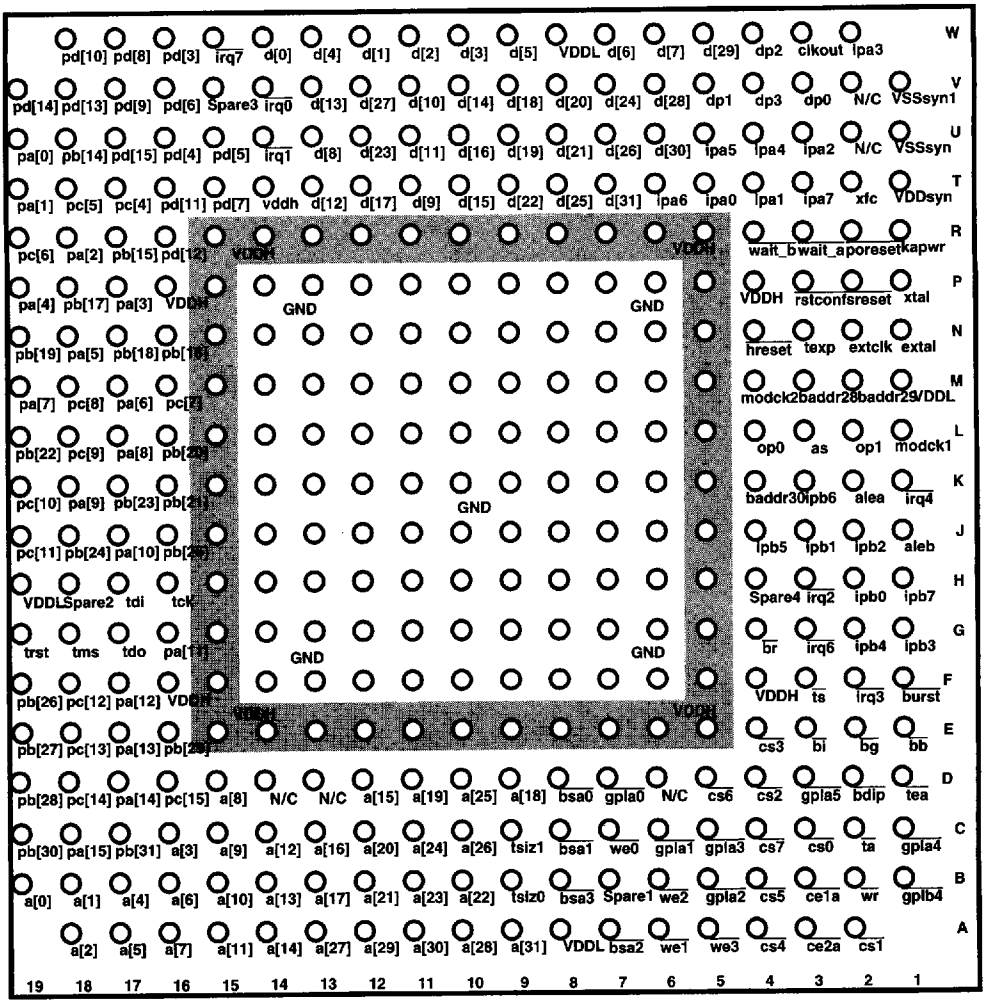
PACKAGE TYPE	FREQUENCY (MHZ)	TEMPERATURE	ORDER NUMBER
Ball Grid Array (ZP Suffix)	25	0°C to 70°C	XPC860ZP25
	25	0°C to 70°C	XPC860ENZP25
	25	0°C to 70°C	XPC860MHZP25
	25	0°C to 70°C	XPC860DCZP25
	25	0°C to 70°C	XPC860DEZP25
	40	0°C to 70°C	XPC860ZP40
	40	0°C to 70°C	XPC860ENZP40
	40	0°C to 70°C	XPC860MHZP40
	40	0°C to 70°C	XPC860DCZP40
	40	0°C to 70°C	XPC860DEZP40
Ball Grid Array (CZP Suffix)	TBD	-40°C to 85°C	TBD

Five different versions of the MPC860 PowerQUICC will be made available. The table below summarizes the different versions. Pricing and availability vary depending on the derivative.

Table 2. MPC860 Version Availability

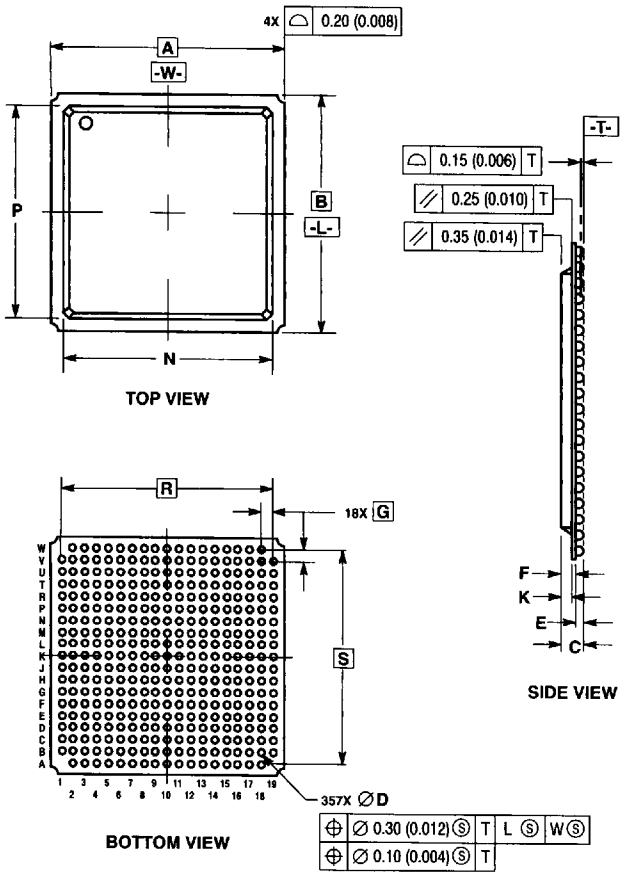
DEVICE	ETHERNET SUPPORT	NUMBER OF SCCS	32-CHANNEL HDLC SUPPORT
MPC860	N/A	Four	N/A
MPC860EN	Yes	Four	N/A
MPC860DC	N/A	Two	N/A
MPC860DE	Yes	Two	N/A
MPC860MH	Yes	Four	Yes

22.2 PIN ASSIGNMENTS – PBGA-TOP VIEW



22.3 PACKAGE DIMENSIONS–PLASTIC BALL GRID ARRAY (PBGA)

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, *Plastic Ball Grid Array Application Note* available from your local Motorola sales office.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	